Term Project: Design of 32-Bit ALU

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Part 1 – ALU 1 Bit:

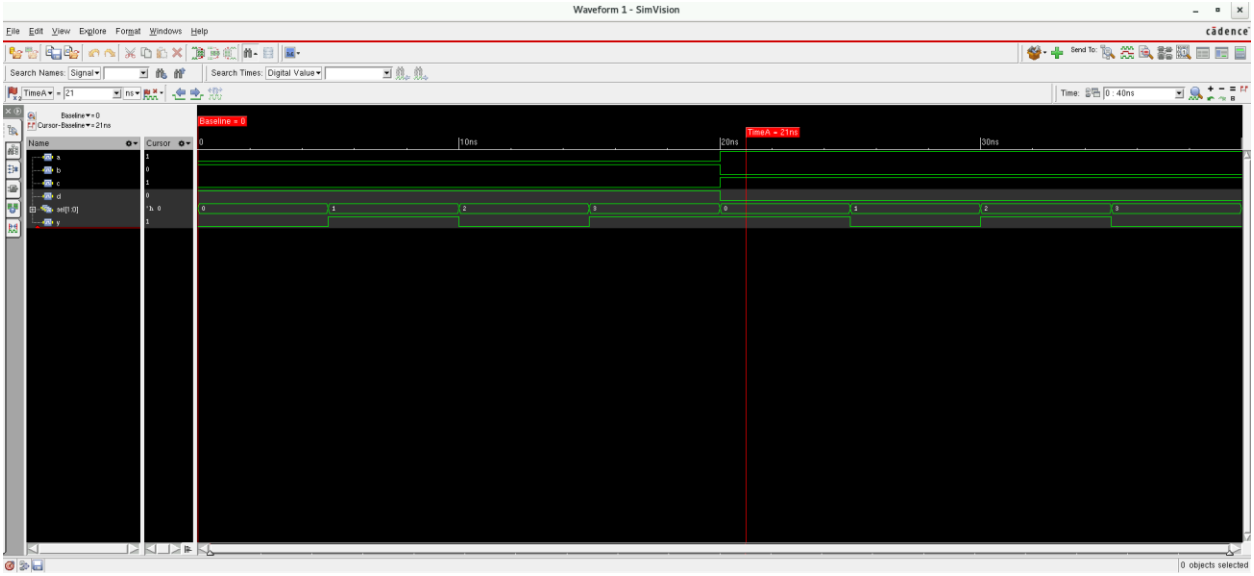


Figure 1: 4x1 Mux Testbench Simulation

Table 1: 4x1 Mux Truth Table

a	b	c	d	S1	S0	y
0	1	0	1	0	0	0
0	1	0	1	0	1	1
0	1	0	1	1	0	0
0	1	0	1	1	1	1
1	0	1	0	0	0	1
1	0	1	0	0	1	0
1	0	1	0	1	0	1
1	0	1	0	1	1	0

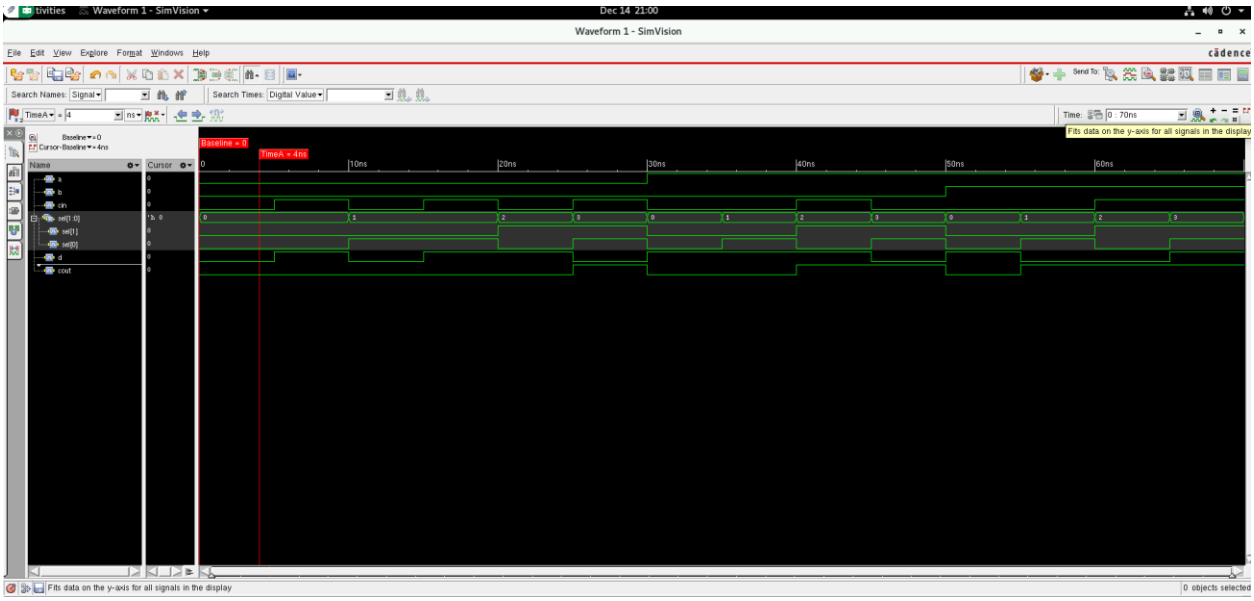


Figure 2: Arithmetic Circuit Testbench Simulation

Table 2: Arithmetic Circuit Truth Table

a	b	Cin	S1	S0	d	Cout
0	0	0	0	0	0	0
0	0	1	0	0	1	0
0	0	0	0	1	0	0
0	0	1	0	1	1	0
0	0	0	1	0	1	0
0	0	1	1	1	0	1
1	0	0	0	0	1	0
1	0	0	0	1	1	0
1	0	1	1	0	1	1
1	0	0	1	1	0	1
1	1	0	0	0	1	0
1	1	0	0	1	0	1
1	1	1	1	0	0	1
1	1	1	1	1	1	1

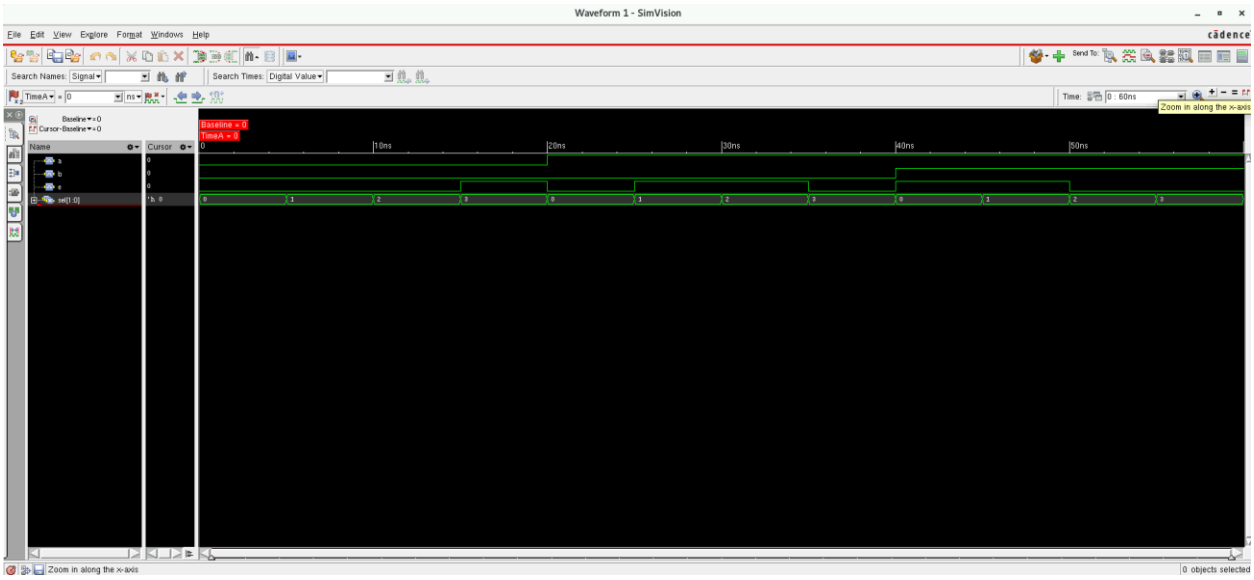


Figure 3: Logic Circuit Testbench Simulation

Table 3: Logic Circuit Truth Table

a	b	S1	S0	e
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

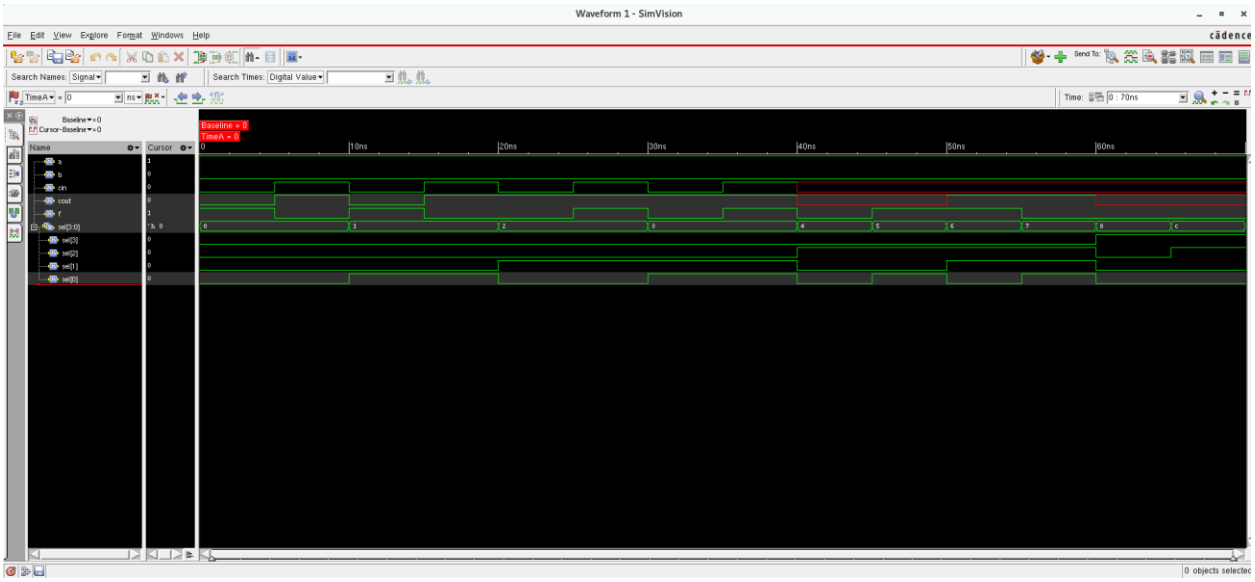


Figure 4: 1-bit ALU Testbench Simulation

Table 4: 1-bit ALU Truth Table

Operation	a	b	Cin	S3	S2	S1	S0	f	Cout
F = A	1	0	0	0	0	0	0	1	0
F = A + 1	1	0	1	0	0	0	0	0	1
F = A + B	1	0	0	0	0	0	1	1	0
F = A + B + 1	1	0	1	0	0	0	1	0	1
F = A + B'	1	0	0	0	0	1	0	0	1
F = A + B' + 1	1	0	1	0	0	1	0	1	1
F = A - 1	1	0	0	0	0	1	1	0	1
F = A	1	0	1	0	0	1	1	1	1
F = A & B	1	0	x	0	1	0	0	0	x
F = A | B	1	0	x	0	1	0	1	1	x
F = A ^ B	1	0	x	0	1	1	0	1	1
F = ~A	1	0	x	0	1	1	1	0	1
F = shr A	1	0	x	1	0	0	0	0	x
F = shl A	1	0	x	1	1	0	0	0	x

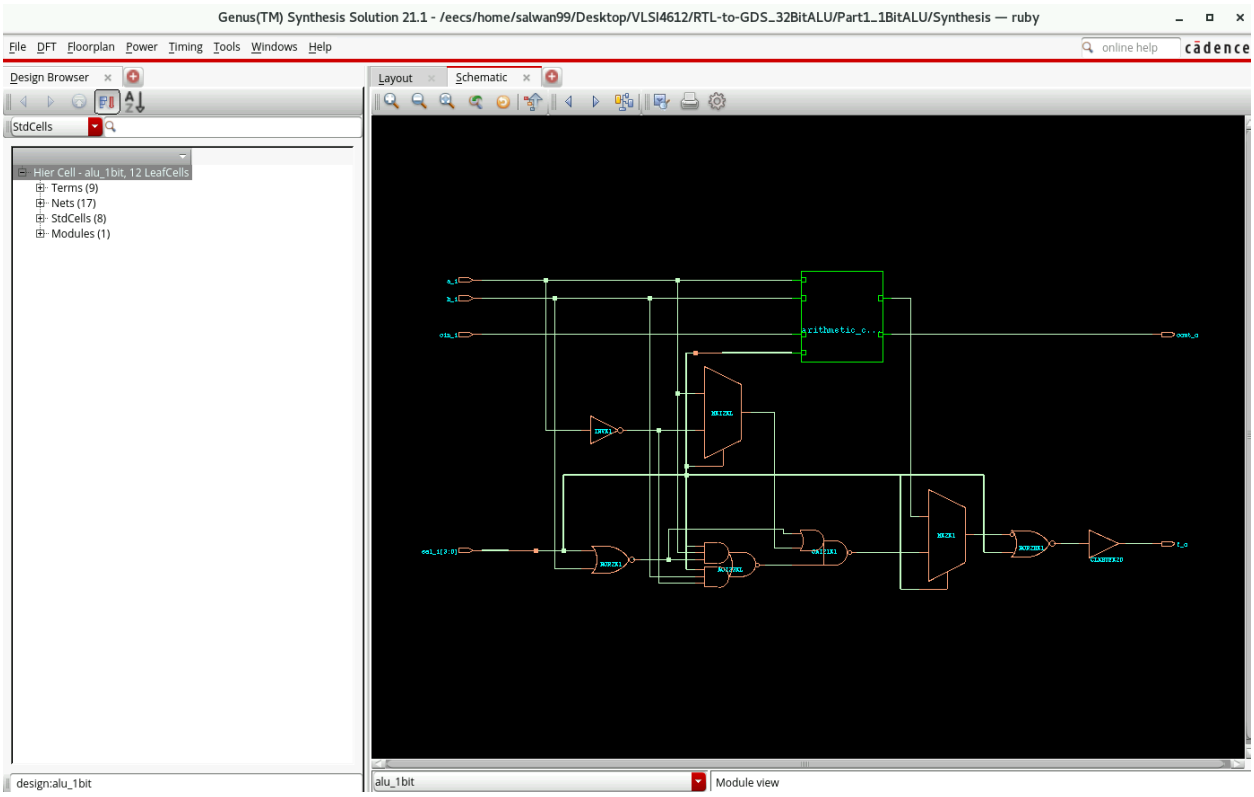


Figure 5: 1-bit ALU Synthesis

```
=============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.17-s066_1
  Generated on:           Dec 12 2025  02:51:35 am
  Module:                 alu_1bit
  Operating conditions:   PVT_0P9V_125C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
=============================================================


   Gate    Instances   Area      Library
-----------------------------------------
ADDFHXL            1   7.524    slow_vdd1v0
AOI33XL            1   2.394    slow_vdd1v0
CLKBUFX20          2  16.416    slow_vdd1v0
INVX1              1   0.684    slow_vdd1v0
MX2X1              1   2.394    slow_vdd1v0
MXI2XL             1   2.394    slow_vdd1v0
NAND2BX1           1   1.368    slow_vdd1v0
NOR2BX1            1   1.368    slow_vdd1v0
NOR2X1             1   1.026    slow_vdd1v0
OAI21X1            1   1.710    slow_vdd1v0
XNOR2X1            1   2.394    slow_vdd1v0
-----------------------------------------
total             12  39.672


     Type      Instances  Area  Area %
---------------------------------------
inverter               1  0.684    1.7
buffer                 2 16.416   41.4
logic                  9 22.572   56.9
physical_cells         0  0.000    0.0
---------------------------------------
total                 12 39.672  100.0
```

Figure 6: Area Report of 1-bit ALU

```
Instance: /alu_1bit
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  ------------------------------------------------------------------------------
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
    register     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       logic     1.69265e-09  1.19618e-08  9.83929e-07  9.97584e-07 100.00%
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       clock     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ------------------------------------------------------------------------------
    Subtotal     1.69265e-09  1.19618e-08  9.83929e-07  9.97584e-07 100.00%
  Percentage           0.17%       1.20%       98.63%      100.00% 100.00%
  ------------------------------------------------------------------------------
```

Figure 7: Power Report of 1-bit ALU

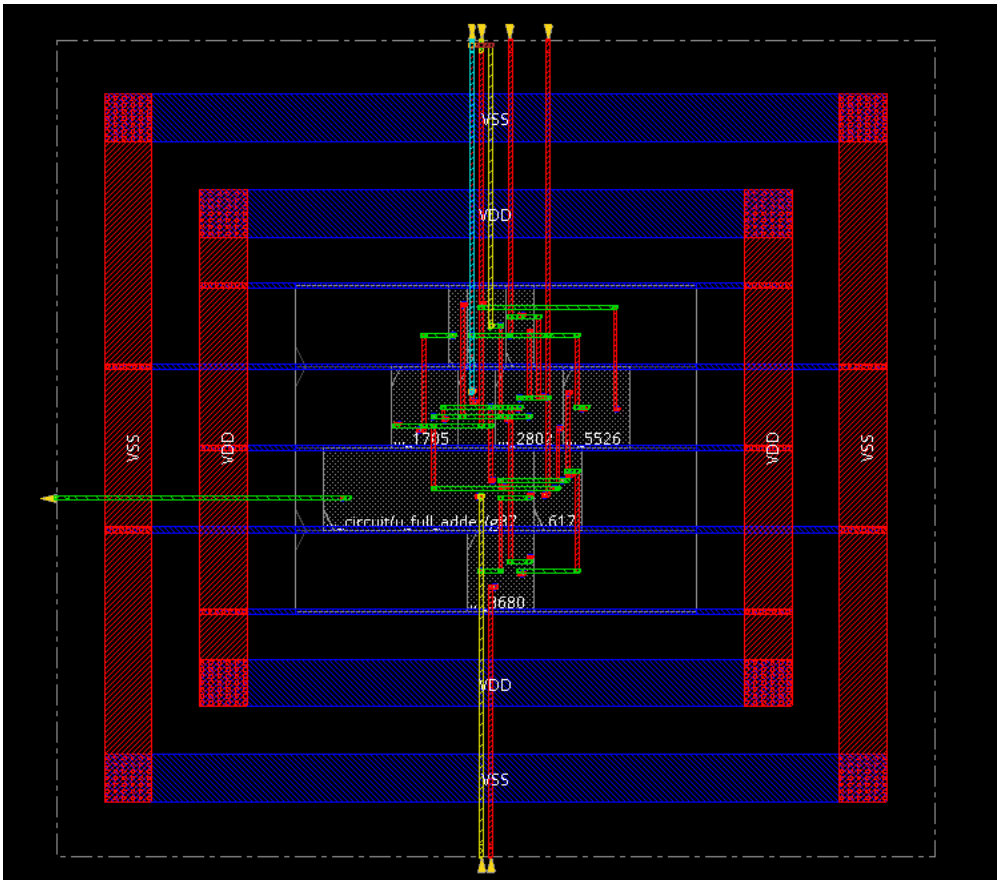


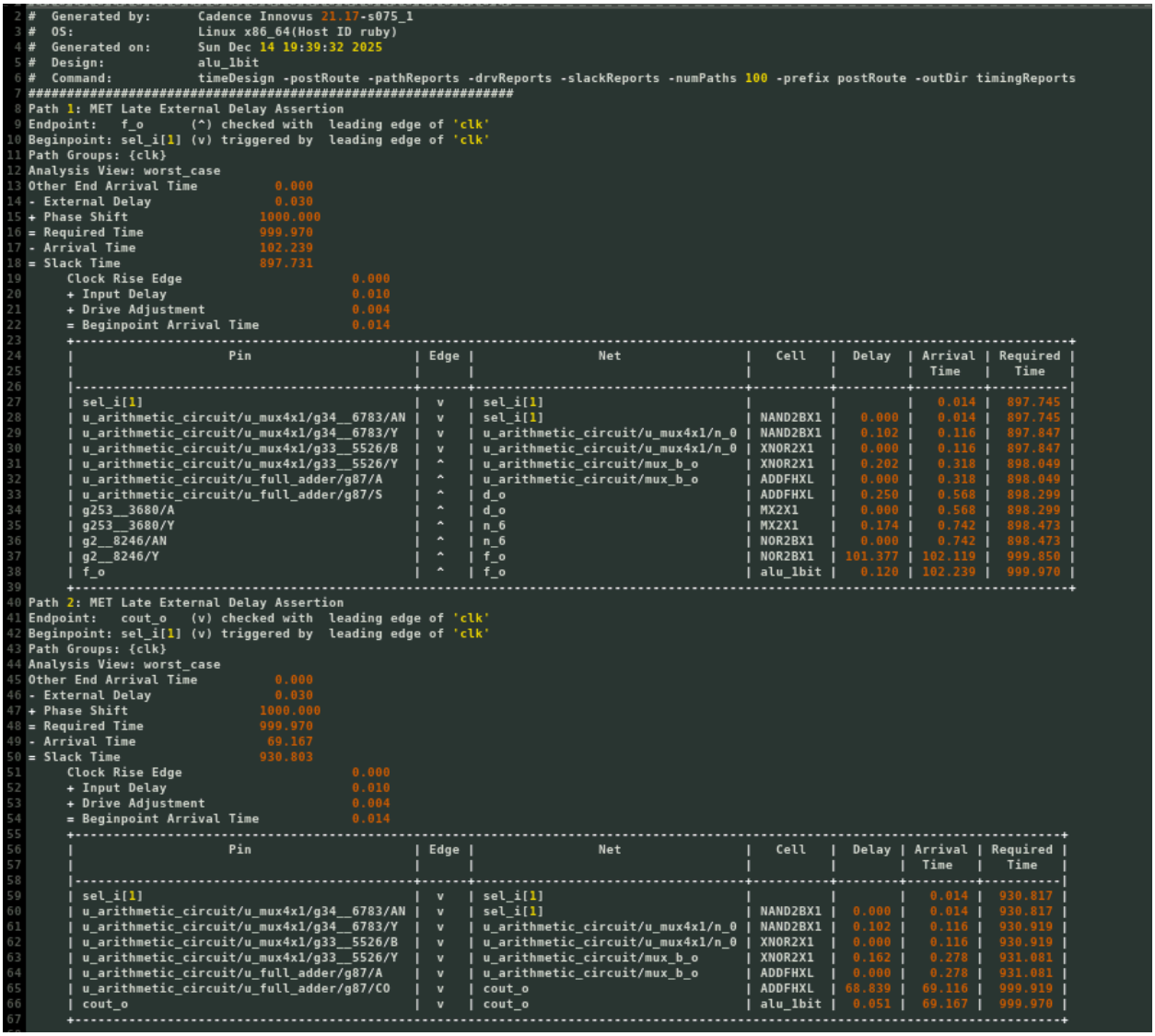
Figure 8: Layout Placement of 1-bit ALU

```
*** Starting Verify DRC (MEM: 2618.7) ***

 VERIFY DRC ..... Starting Verification
 VERIFY DRC ..... Initializing
 VERIFY DRC ..... Deleting Existing Violations
 VERIFY DRC ..... Creating Sub-Areas
 VERIFY DRC ..... Using new threading
 VERIFY DRC ..... Sub-Area: {0.000 0.000 18.400 17.100} 1 of 1
 VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

 Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.0  ELAPSED TIME: 0.00  MEM: 264.1M) ***
```

Figure 9: 1-bit ALU DRC Verification Results

```
******** Start: VERIFY CONNECTIVITY ********
Start Time: Fri Dec 12 12:10:42 2025

Design Name: alu_1bit
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (18.4000, 17.1000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Fri Dec 12 12:10:42 2025
Time Elapsed: 0:00:00.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.000M)
```

Figure 10: Connectivity Verification for 1-bit ALU



```
#  Generated by:      Cadence Innovus 21.17-s075_1
#  OS:                Linux x86_64(Host ID ruby)
#  Generated on:      Sun Dec 14 19:39:32 2025
#  Design:            alu_1bit
#  Command:           timeDesign -postRoute -pathReports -drvReports -slackReports -numPaths 100 -prefix postRoute -outDir timingReports
#############################################################
Path 1: MET Late External Delay Assertion
Endpoint:   f_o     (^) checked with  leading edge of 'clk'
Beginpoint: sel_i[1] (v) triggered by  leading edge of 'clk'
Path Groups: {clk}
Analysis View: worst_case
Other End Arrival Time          0.000
- External Delay               0.030
+ Phase Shift                1000.000
= Required Time               999.970
- Arrival Time                102.239
= Slack Time                  897.731
     Clock Rise Edge                      0.000
     + Input Delay                        0.010
     + Drive Adjustment                   0.004
     = Beginpoint Arrival Time            0.014
     +-------------------------------------------------------------------------------------------------------------------------------+
     |                   Pin                   | Edge |              Net               |   Cell   |  Delay  | Arrival | Required |
     |                                         |      |                                |          |         |  Time   |   Time   |
     |-----------------------------------------+------+--------------------------------+----------+---------+---------+----------|
     | sel_i[1]                                |  v   | sel_i[1]                       |          |         |   0.014 |  897.745 |
     | u_arithmetic_circuit/u_mux4x1/g34__6783/AN |  v   | sel_i[1]                       | NAND2BX1 |   0.000 |   0.014 |  897.745 |
     | u_arithmetic_circuit/u_mux4x1/g34__6783/Y |  v   | u_arithmetic_circuit/u_mux4x1/n_0 | NAND2BX1 |   0.102 |   0.116 |  897.847 |
     | u_arithmetic_circuit/u_mux4x1/g33__5526/B |  v   | u_arithmetic_circuit/u_mux4x1/n_0 | XNOR2X1  |   0.000 |   0.116 |  897.847 |
     | u_arithmetic_circuit/u_mux4x1/g33__5526/Y |  ^   | u_arithmetic_circuit/mux_b_o   | XNOR2X1  |   0.202 |   0.318 |  898.049 |
     | u_arithmetic_circuit/u_full_adder/g87/A |  ^   | u_arithmetic_circuit/mux_b_o   | ADDFHXL  |   0.000 |   0.318 |  898.049 |
     | u_arithmetic_circuit/u_full_adder/g87/S |  ^   | d_o                            | ADDFHXL  |   0.250 |   0.568 |  898.299 |
     | g253__3680/A                            |  ^   | d_o                            | MX2X1    |   0.000 |   0.568 |  898.299 |
     | g253__3680/Y                            |  ^   | n_6                            | MX2X1    |   0.174 |   0.742 |  898.473 |
     | g2__8246/AN                             |  ^   | n_6                            | NOR2BX1  |   0.000 |   0.742 |  898.473 |
     | g2__8246/Y                              |  ^   | f_o                            | NOR2BX1  | 101.377 | 102.119 |  999.850 |
     | f_o                                     |  ^   | f_o                            | alu_1bit |   0.120 | 102.239 |  999.970 |
     +-------------------------------------------------------------------------------------------------------------------------------+
Path 2: MET Late External Delay Assertion
Endpoint:   cout_o   (v) checked with  leading edge of 'clk'
Beginpoint: sel_i[1] (v) triggered by  leading edge of 'clk'
Path Groups: {clk}
Analysis View: worst_case
Other End Arrival Time          0.000
- External Delay               0.030
+ Phase Shift                1000.000
= Required Time               999.970
- Arrival Time                 69.167
= Slack Time                  930.803
     Clock Rise Edge                      0.000
     + Input Delay                        0.010
     + Drive Adjustment                   0.004
     = Beginpoint Arrival Time            0.014
     +-------------------------------------------------------------------------------------------------------------------------------+
     |                   Pin                   | Edge |              Net               |   Cell   |  Delay  | Arrival | Required |
     |                                         |      |                                |          |         |  Time   |   Time   |
     |-----------------------------------------+------+--------------------------------+----------+---------+---------+----------|
     | sel_i[1]                                |  v   | sel_i[1]                       |          |         |   0.014 |  930.817 |
     | u_arithmetic_circuit/u_mux4x1/g34__6783/AN |  v   | sel_i[1]                       | NAND2BX1 |   0.000 |   0.014 |  930.817 |
     | u_arithmetic_circuit/u_mux4x1/g34__6783/Y |  v   | u_arithmetic_circuit/u_mux4x1/n_0 | NAND2BX1 |   0.102 |   0.116 |  930.919 |
     | u_arithmetic_circuit/u_mux4x1/g33__5526/B |  v   | u_arithmetic_circuit/u_mux4x1/n_0 | XNOR2X1  |   0.000 |   0.116 |  930.919 |
     | u_arithmetic_circuit/u_mux4x1/g33__5526/Y |  v   | u_arithmetic_circuit/mux_b_o   | XNOR2X1  |   0.162 |   0.278 |  931.081 |
     | u_arithmetic_circuit/u_full_adder/g87/A |  v   | u_arithmetic_circuit/mux_b_o   | ADDFHXL  |   0.000 |   0.278 |  931.081 |
     | u_arithmetic_circuit/u_full_adder/g87/CO |  v   | cout_o                         | ADDFHXL  |  68.839 |  69.116 |  999.919 |
     | cout_o                                  |  v   | cout_o                         | alu_1bit |   0.051 |  69.167 |  999.970 |
     +-------------------------------------------------------------------------------------------------------------------------------+
```

Figure 11: Timing Report for 1-Bit ALU

Part 2 a – Hierarchical ALU 32 Bit:

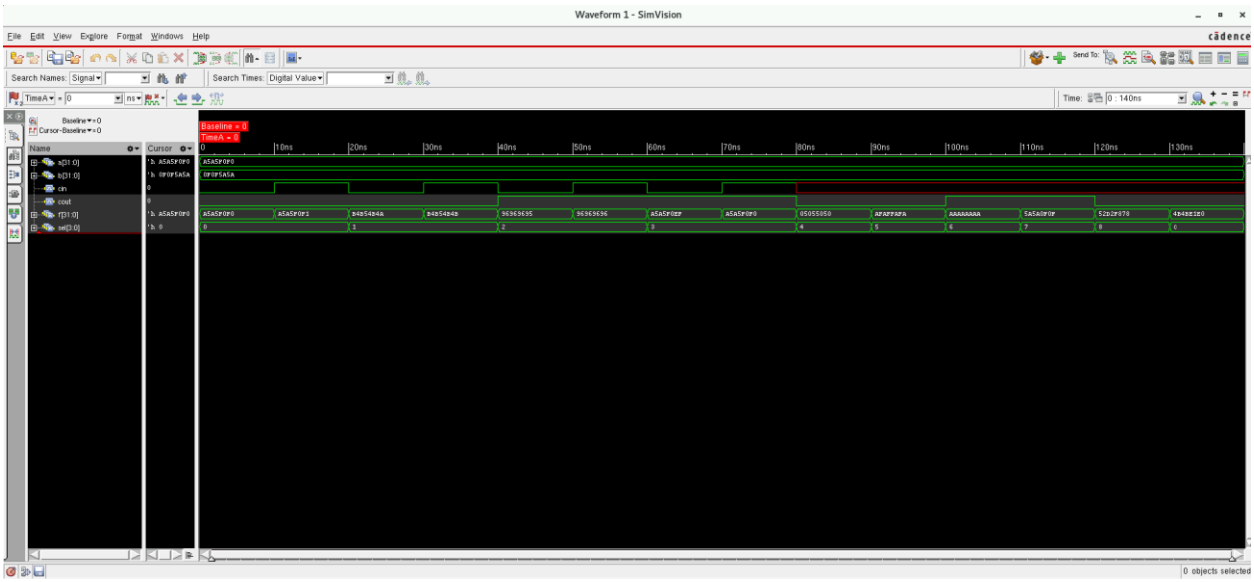


Figure 12: 32-bit ALU Simulation Results Using 32 Modules of the 1-bit ALU

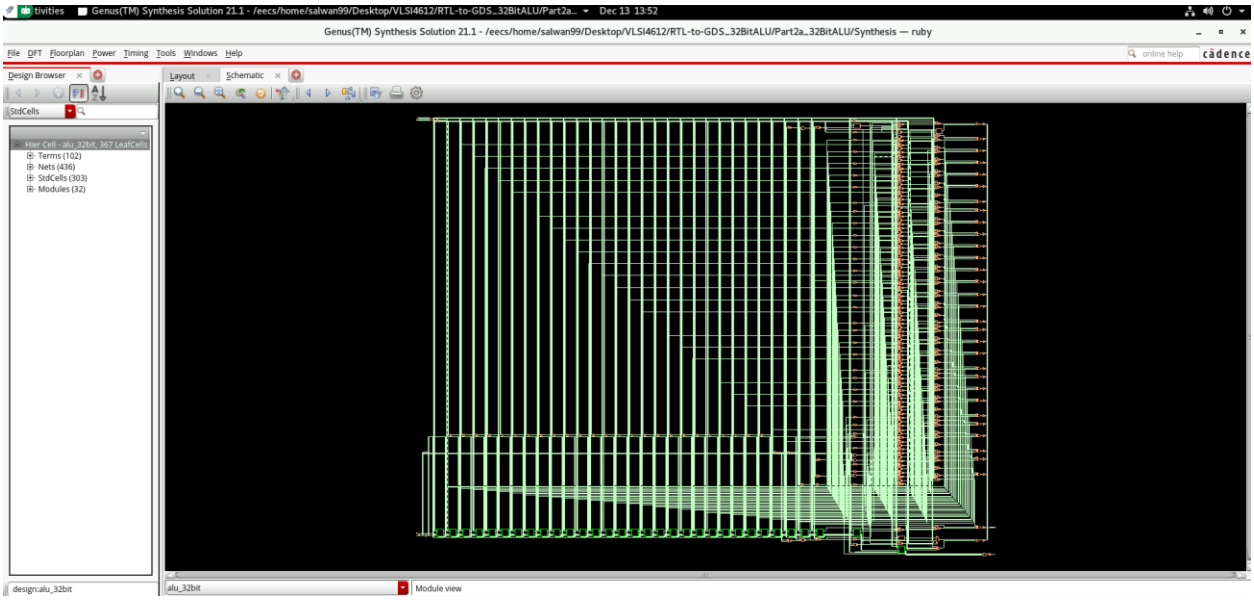
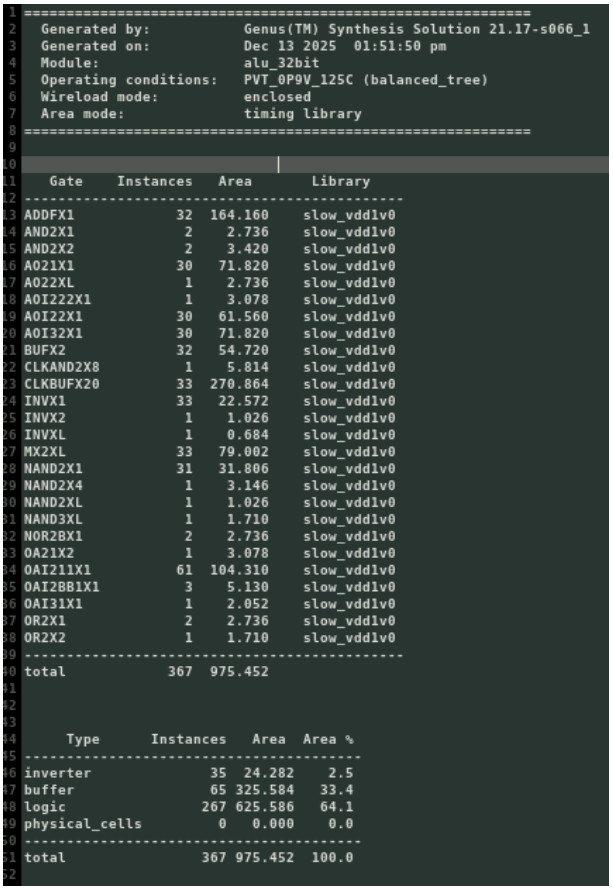


Figure 13: Synthesis Layout of the 32-bit ALU from Part2a



```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.17-s066_1
  Generated on:           Dec 13 2025  01:51:50 pm
  Module:                 alu_32bit
  Operating conditions:   PVT_0P9V_125C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

   Gate    Instances   Area       Library
-------------------------------------------
ADDFX1            32  164.160    slow_vdd1v0
AND2X1             2    2.736    slow_vdd1v0
AND2X2             2    3.420    slow_vdd1v0
AO21X1            30   71.820    slow_vdd1v0
AO22XL             1    2.736    slow_vdd1v0
AOI222X1           1    3.078    slow_vdd1v0
AOI22X1           30   61.560    slow_vdd1v0
AOI32X1           30   71.820    slow_vdd1v0
BUFX2             32   54.720    slow_vdd1v0
CLKAND2X8          1    5.814    slow_vdd1v0
CLKBUFX20         33  270.864    slow_vdd1v0
INVX1             33   22.572    slow_vdd1v0
INVX2              1    1.026    slow_vdd1v0
INVXL              1    0.684    slow_vdd1v0
MX2XL             33   79.002    slow_vdd1v0
NAND2X1           31   31.806    slow_vdd1v0
NAND2X4            1    3.146    slow_vdd1v0
NAND2XL            1    1.026    slow_vdd1v0
NAND3XL            1    1.710    slow_vdd1v0
NOR2BX1            2    2.736    slow_vdd1v0
OA21X2             1    3.078    slow_vdd1v0
OAI211X1          61  104.310    slow_vdd1v0
OAI2BB1X1          3    5.130    slow_vdd1v0
OAI31X1            1    2.052    slow_vdd1v0
OR2X1              2    2.736    slow_vdd1v0
OR2X2              1    1.710    slow_vdd1v0
-------------------------------------------
total            367  975.452



     Type      Instances   Area  Area %
----------------------------------------
inverter              35  24.282    2.5
buffer                65 325.584   33.4
logic                267 625.586   64.1
physical_cells         0   0.000    0.0
----------------------------------------
total                367 975.452  100.0
```

Figure 14: Area Report from 32-bit ALU Part2a

```
Instance: /alu_32bit
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  ------------------------------------------------------------------------------
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
    register     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       logic     3.64544e-08  3.30270e-07  2.49493e-05  2.53160e-05 100.00%
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       clock     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ------------------------------------------------------------------------------
    Subtotal     3.64544e-08  3.30270e-07  2.49493e-05  2.53160e-05 100.00%
  Percentage           0.14%        1.30%       98.55%      100.00% 100.00%
  ------------------------------------------------------------------------------
```

Figure 15: Power Report for 32-bit ALU Part2a

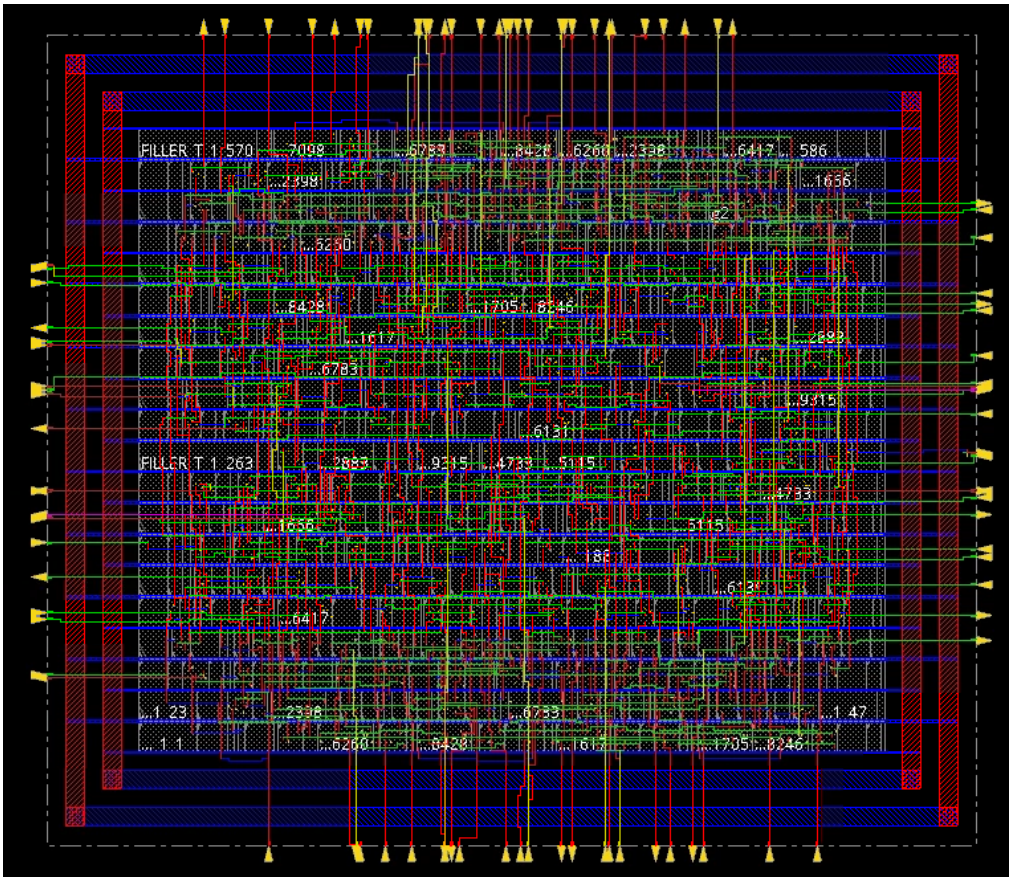


Figure 16: Place and Route in Innovus for 32-bit ALU for Part2a

```
#-check_same_via_cell true              # bool, default=false, user setting
#-exclude_pg_net true                   # bool, default=false, user setting
#-report alu_32bit.drc.rpt              # string, default="", user setting
 *** Starting Verify DRC (MEM: 2628.6) ***

  VERIFY DRC ..... Starting Verification
  VERIFY DRC ..... Initializing
  VERIFY DRC ..... Deleting Existing Violations
  VERIFY DRC ..... Creating Sub-Areas
  VERIFY DRC ..... Using new threading
  VERIFY DRC ..... Sub-Area: {0.000 0.000 50.800 44.460} 1 of 1
  VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

  Verification Complete : 0 Viols.

 *** End Verify DRC (CPU: 0:00:00.1  ELAPSED TIME: 0.00  MEM: 264.1M) ***

innovus 1>
```

Figure 17: DRc Verification for 32 Bit ALU Part2a

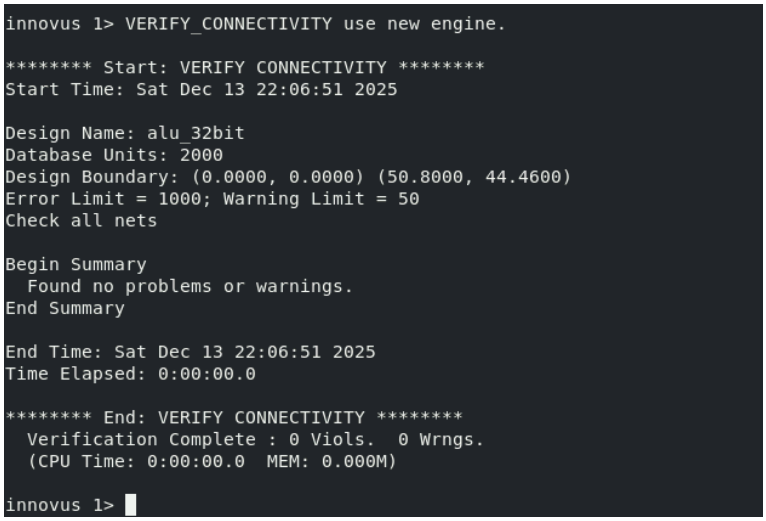


Figure 18: Connectivity Verification for 32 Bit ALU for Part2a

Part 2 b – ALU 32 Bit Behavioral:

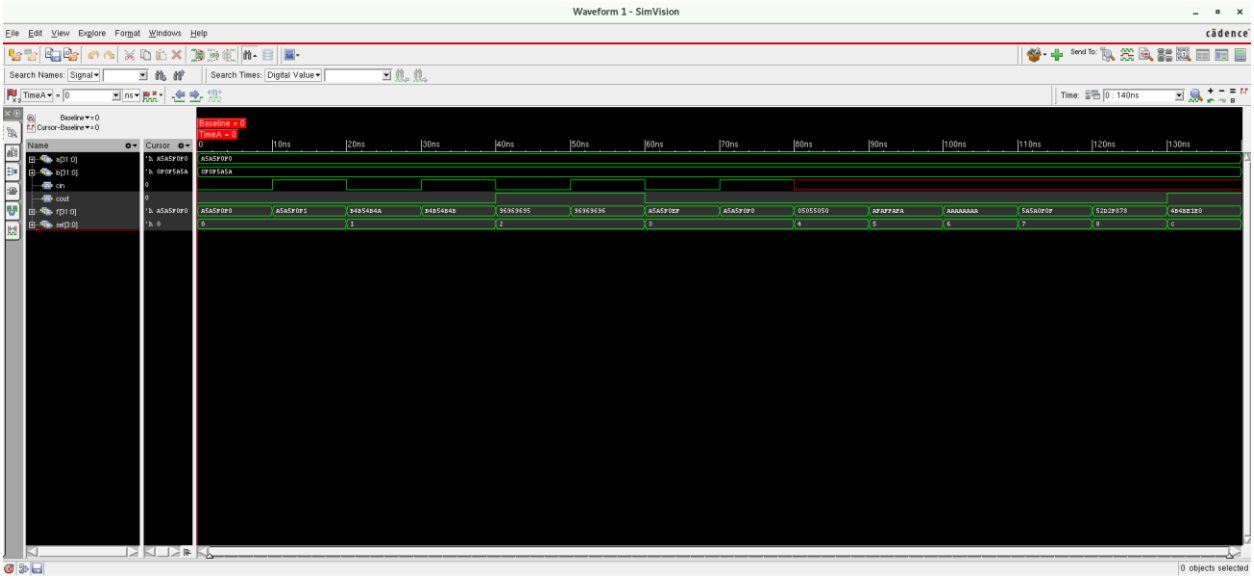


Figure 19: 32-bit ALU Behavioral Simulation Waveform

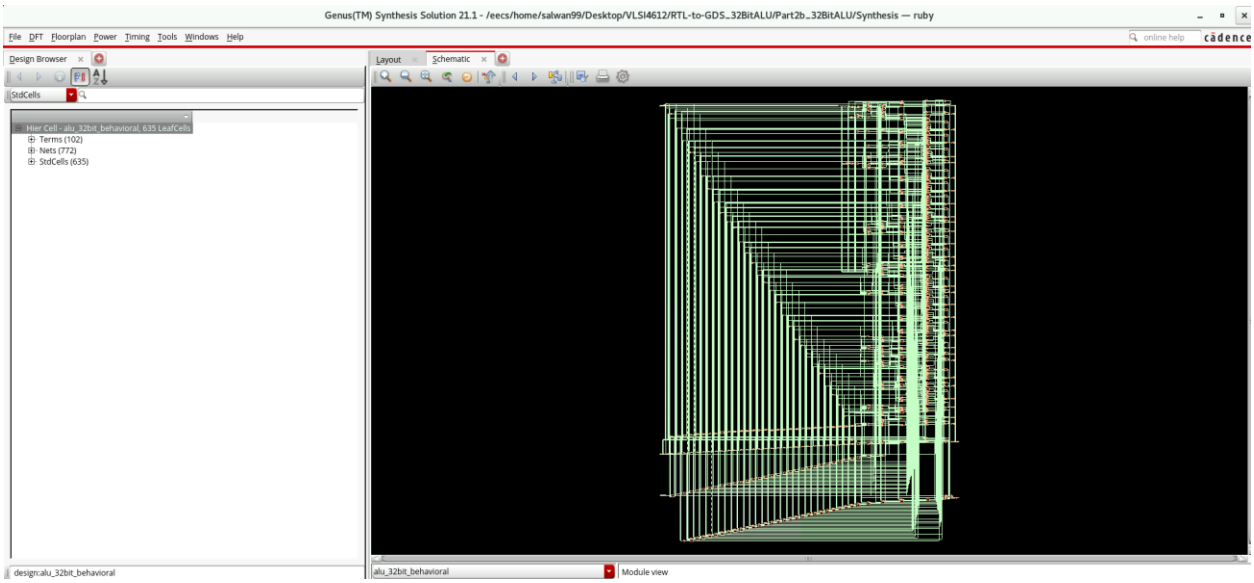
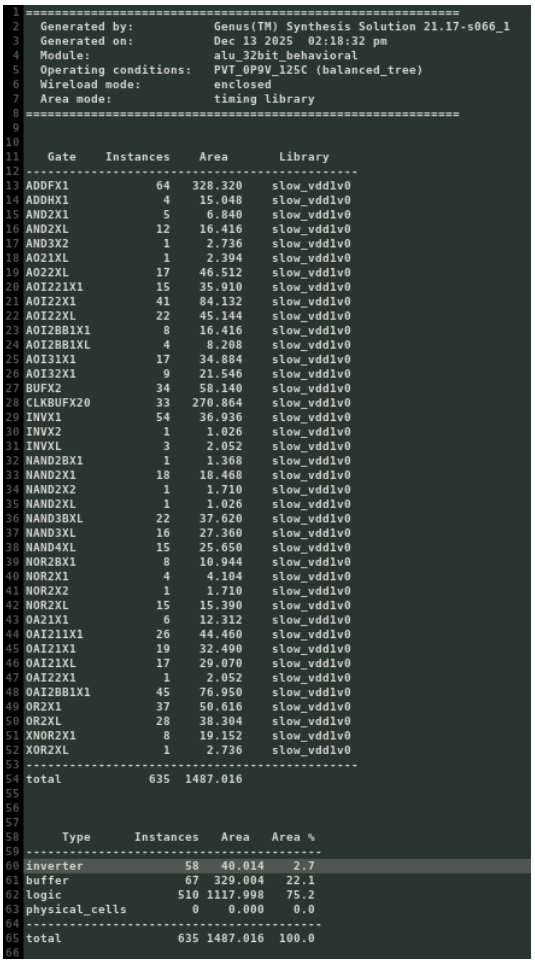
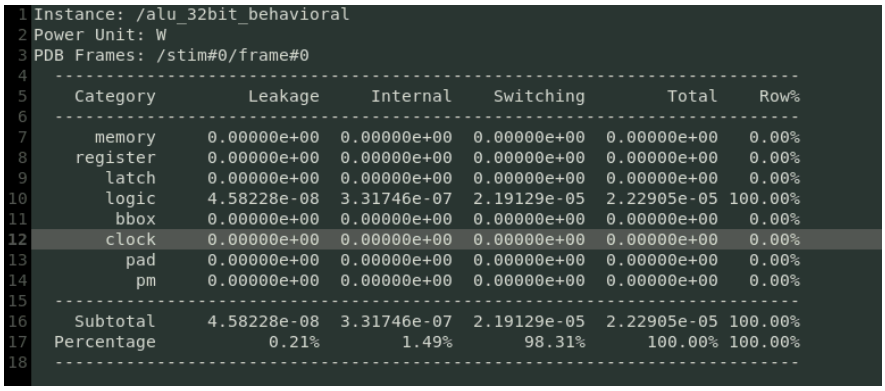


Figure 20: Synthesis Layout of 32-bit Behavioral ALU for Part2b



```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.17-s066_1
  Generated on:           Dec 13 2025  02:18:32 pm
  Module:                 alu_32bit_behavioral
  Operating conditions:   PVT_0P9V_125C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================


   Gate    Instances    Area       Library
-----------------------------------------------
ADDFX1            64   328.320    slow_vdd1v0
ADDHX1             4    15.048    slow_vdd1v0
AND2X1             5     6.840    slow_vdd1v0
AND2XL            12    16.416    slow_vdd1v0
AND3X2             1     2.736    slow_vdd1v0
AO21XL             1     2.394    slow_vdd1v0
AO22XL            17    46.512    slow_vdd1v0
AOI221X1          15    35.910    slow_vdd1v0
AOI22X1           41    84.132    slow_vdd1v0
AOI22XL           22    45.144    slow_vdd1v0
AOI2BB1X1          8    16.416    slow_vdd1v0
AOI2BB1XL          4     8.208    slow_vdd1v0
AOI31X1           17    34.884    slow_vdd1v0
AOI32X1            9    21.546    slow_vdd1v0
BUFX2             34    58.140    slow_vdd1v0
CLKBUFX20         33   270.864    slow_vdd1v0
INVX1             54    36.936    slow_vdd1v0
INVX2              1     1.026    slow_vdd1v0
INVXL              3     2.052    slow_vdd1v0
NAND2BX1           1     1.368    slow_vdd1v0
NAND2X1           18    18.468    slow_vdd1v0
NAND2X2            1     1.710    slow_vdd1v0
NAND2XL            1     1.026    slow_vdd1v0
NAND3BXL          22    37.620    slow_vdd1v0
NAND3XL           16    27.360    slow_vdd1v0
NAND4XL           15    25.650    slow_vdd1v0
NOR2BX1            8    10.944    slow_vdd1v0
NOR2X1             4     4.104    slow_vdd1v0
NOR2X2             1     1.710    slow_vdd1v0
NOR2XL            15    15.390    slow_vdd1v0
OA21X1             6    12.312    slow_vdd1v0
OAI211X1          26    44.460    slow_vdd1v0
OAI21X1           19    32.490    slow_vdd1v0
OAI21XL           17    29.070    slow_vdd1v0
OAI22X1            1     2.052    slow_vdd1v0
OAI2BB1X1         45    76.950    slow_vdd1v0
OR2X1             37    50.616    slow_vdd1v0
OR2XL             28    38.304    slow_vdd1v0
XNOR2X1            8    19.152    slow_vdd1v0
XOR2XL             1     2.736    slow_vdd1v0
-----------------------------------------------
total            635  1487.016


     Type      Instances   Area   Area %
---------------------------------------
inverter             58   40.014    2.7
buffer               67  329.004   22.1
logic               510 1117.998   75.2
physical_cells        0    0.000    0.0
---------------------------------------
total               635 1487.016  100.0
```

Figure 21: Area Report for 32-bit Behavioral ALU



```
Instance: /alu_32bit_behavioral
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  ------------------------------------------------------------------------
       memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
     register     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        logic     4.58228e-08  3.31746e-07  2.19129e-05  2.22905e-05 100.00%
         bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        clock     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
          pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
           pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ------------------------------------------------------------------------
    Subtotal     4.58228e-08  3.31746e-07  2.19129e-05  2.22905e-05 100.00%
  Percentage           0.21%        1.49%       98.31%      100.00% 100.00%
  ------------------------------------------------------------------------
```

Figure 22: Power Report for 32-bit Behavioral ALU

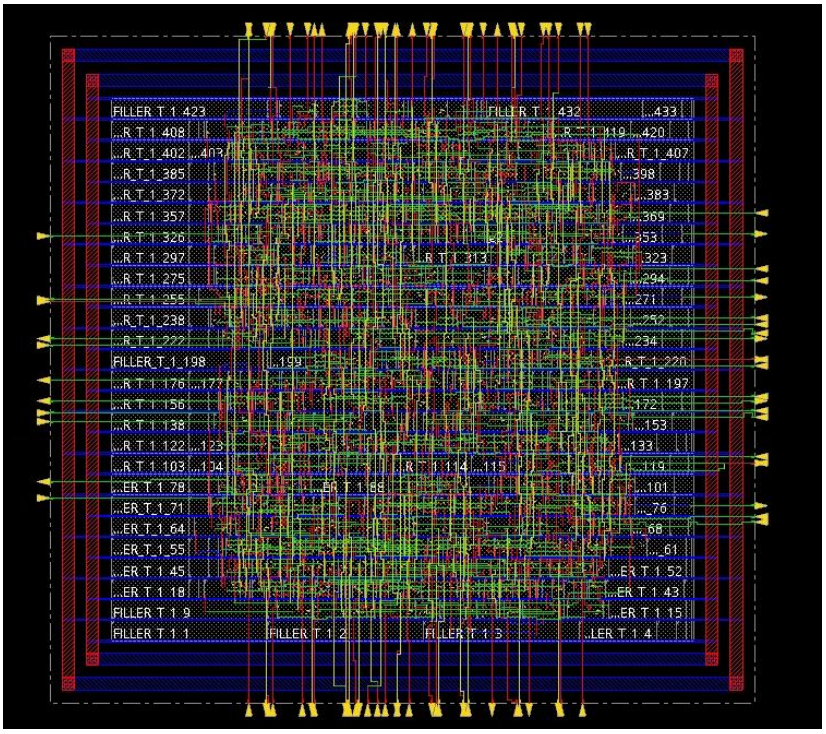


Figure 23: Place and Route in Innovus for 32-bit Behavioral ALU for Part2b

```
 *** Starting Verify DRC (MEM: 2644.3) ***

  VERIFY DRC ..... Starting Verification
  VERIFY DRC ..... Initializing
  VERIFY DRC ..... Deleting Existing Violations
  VERIFY DRC ..... Creating Sub-Areas
  VERIFY DRC ..... Using new threading
  VERIFY DRC ..... Sub-Area: {0.000 0.000 57.800 54.720} 1 of 1
  VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

  Verification Complete : 0 Viols.

 *** End Verify DRC (CPU: 0:00:00.1  ELAPSED TIME: 1.00  MEM: 256.1M) ***

innovus 1>
```

Figure 24: DRC Verification Results for 32-bit Behavioral ALU

```
******** Start: VERIFY CONNECTIVITY ********
Start Time: Sat Dec 13 21:17:18 2025

Design Name: alu_32bit_behavioral
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (57.8000, 54.7200)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Sat Dec 13 21:17:18 2025
Time Elapsed: 0:00:00.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.000M)

innovus 1>
```

Figure 25: Connectivity Verification for 32-bit Behavioral ALU

Final Layout in Virtuoso for the Least Area Design:

From the area report performed in Part2a and Part2b, the 32-bit ALU in Part2a with the hierarchical design in Verilog had less area; therefore, I imported the pad frame and the GDS layout for Part2a from Innovus to Virtuoso software to design the chip. However, I ran out of time and couldn't finish connecting all the inputs and outputs to the pad frame.

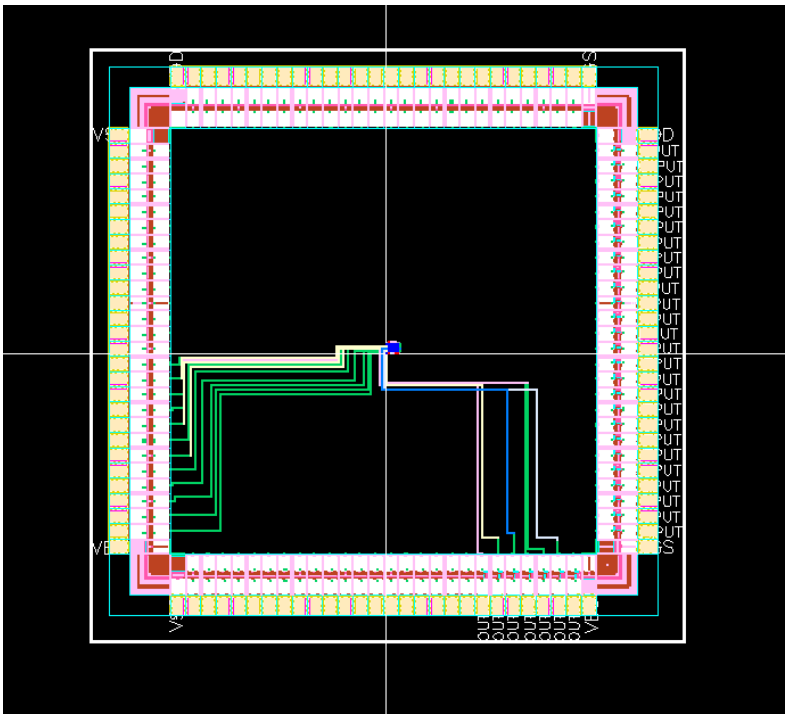


Figure 26: Hierarchical 32 Bit ALU Layout with Pad Frame

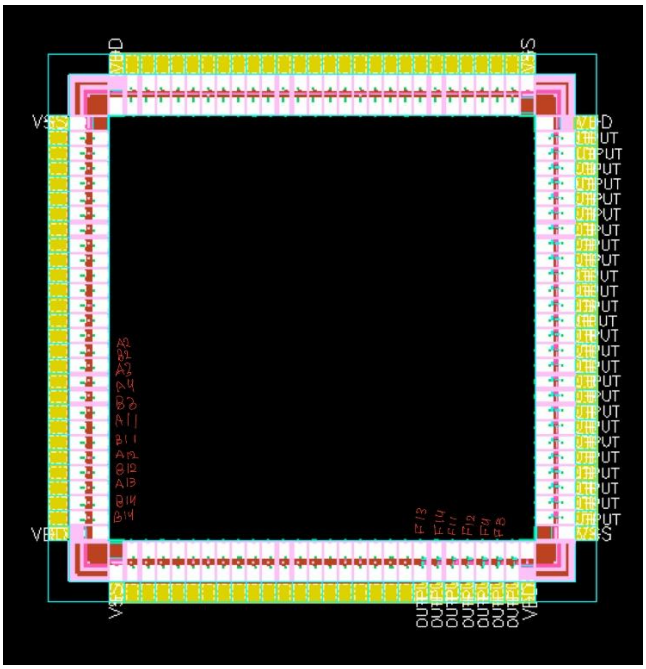


Figure 27: Pin Diagram for 32 Bit ALU Layout