ICT 1206Y Computer Organisation and Architecture

BSc (Hons) Computer Science – Level 1 Semester 2 (2024/2025)

Assignment Title: Exploring the Memory Hierarchy and Architectural Features of Intel Core i7/i9 Processors

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Objectives:

1. Understand the memory hierarchy in Intel Core i7/i9 processors.
2. Explore and analyze cache mapping techniques and cache design in modern CPUs.
3. Gain insights into addressing modes, system bus architecture, and pipelining in Intel processors.
4. Develop a comprehensive understanding of how these features influence system performance.

Assignment Brief:

You are required to analyze and document the key architectural aspects of Intel Core i7 or i9 processors, focusing on the memory hierarchy, cache organization, and system bus design. You will also investigate how addressing modes and pipelining enhance processor efficiency. The assignment includes both theoretical analysis and practical simulation.

Tasks:

1. **Memory Hierarchy Analysis**
    - Describe the memory hierarchy in Intel Core i7/i9 processors (registers, L1/L2/L3 caches, main memory).
    - Explain the role of each level in the hierarchy and its impact on performance.
2. **Cache Design and Mapping Techniques**
    - Research and document the cache organization in Intel Core i7/i9 processors.

- Explain different cache mapping techniques (e.g., direct mapping, associative mapping, and set-associative mapping) and identify the mapping technique(s) used in these processors.
- Discuss cache replacement policies and how they are implemented.

3. **Addressing Modes**
   - Identify the addressing modes supported by Intel Core i7/i9 processors.
   - Provide examples of how these modes are used in assembly language instructions.
4. **System Bus Architecture**
   - Analyze the system bus architecture of Intel Core i7/i9 processors.
   - Explain the role of different buses (address bus, data bus, control bus) in facilitating communication.
5. **Pipelining and Performance**
   - Describe the pipelining mechanism in Intel Core i7/i9 processors.
   - Discuss the challenges (e.g., pipeline hazards) and techniques used to overcome them.
6. **Practical Component** **
   - Use a simulation tool (e.g., MARIE Simulator, SimCache, or a similar CPU simulation platform) to demonstrate cache behavior, pipelining, or addressing modes.
   - Provide screenshots or documentation of your findings.

Deliverables:

1. A detailed report (3,000–4,000 words) addressing all tasks.
2. Diagrams or tables to explain concepts such as memory hierarchy, cache organization, and system bus.
3. For the practical component **, include the simulation setup, code (if applicable), and output results.

Evaluation Criteria:

1. **Depth of Analysis** (40%): Clarity and detail in explaining the memory hierarchy, cache design, addressing modes, system bus, and pipelining.

2. **Use of Examples** (20%): Relevance and accuracy of examples provided.
3. **Presentation** (20%): Organization of content, use of diagrams, and quality of explanations.
4. **Practical Component**** (20%): Completeness and accuracy of simulations or practical demonstrations.

Timeline:

- Week 2-4: Research and data collection.
- Week 5-8: Draft report and complete simulations.
- Week 9-10: Finalize and submit the assignment.

Additional Resources:

- Intel Architecture Optimization Manuals
- Tools: MARIE Simulator, SimCache, or other CPU simulation tools
- Research papers or articles on Intel Core i7/i9 architecture

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This assignment allows students to delve deeply into modern processor architectures while incorporating theoretical and practical elements for a holistic learning experience.

Group Assignment (2 students per group)

Deadline**: 08 April 2025**

Late submission 50% penalty

Submit on Turnitin Platform Only

Class ID 47140620

Enrolment Key: qwerty

Use Filename: ICT1206Y_ IDofStudent1_IDofStudent2.pdf

****Practical Simulation Component:**

Use a CPU simulation tool such as **MARIE Simulator**, **SimCache**, or a similar platform to explore and demonstrate **<u>one</u>** of the following aspects of Intel Core i7/i9 architecture:

Option 1: Cache Behavior Simulation

1. Simulate cache operations such as:
    - Cache hits and misses.
    - Effects of different cache mapping techniques (direct mapping, associative mapping, and set-associative mapping).
    - Cache replacement policies (e.g., LRU, FIFO).
2. Analyze how cache size, block size, and associativity affect performance metrics such as hit rate and miss rate.
3. Include screenshots and a discussion of your observations.

Option 2: Pipelining Simulation

1. Simulate an instruction pipeline to demonstrate:
    - Instruction fetch, decode, execute, memory access, and write-back stages.
    - Pipeline stalls due to hazards (data, structural, or control).
2. Experiment with techniques to overcome hazards, such as pipeline forwarding or branch prediction.
3. Provide visual representations of pipeline behavior and explain the impact on performance.

Option 3: Addressing Modes Simulation

1. Simulate various addressing modes, such as:
    - Immediate, direct, indirect, register, indexed, and base-relative addressing.
2. Provide examples of assembly instructions using each addressing mode and show how the CPU resolves memory addresses.
3. Document your findings with sample input/output and memory content screenshots.

Recommended Tools:

- **MARIE Simulator**: Suitable for exploring addressing modes and basic pipeline behavior.
- **SimCache**: Ideal for demonstrating cache operations and cache performance metrics.
- **QtSPIM (MIPS Simulator)**: Can simulate pipelining, cache behavior, and instruction execution.
- **Gem5**: Advanced simulation tool for detailed CPU architecture analysis.
- **SimpleScalar**: For in-depth simulations of processor features.

Deliverables for Simulation:

1. **Setup Documentation**: Briefly describe the simulation tool used and how you configured it for the task.
2. **Screenshots/Outputs**: Include outputs of the simulation, such as cache performance graphs, pipeline execution charts, or memory addressing results.
3. **Analysis**: Discuss the results obtained from the simulation. Link these findings to the theoretical concepts studied in the assignment.