Cache Simulator Project

This project is to help students understand cache structure.

Given a small memory shown below:

| | Cache Worksheet Small Memory Example: | | | | | | | | | | |
|---------|---------------------------------------|------|---------|--------|------|---------|--------|------|---------|--------|------|
| Address | Binary | Data | Address | Binary | Data | Address | Binary | Data | Address | Binary | Data |
| 0 | 000000 | 92 | 16 | 010000 | FB | 32 | 100000 | A | 48 | 110000 | 85 |
| 1 | 000001 | 70 | 17 | 010001 | 44 | 33 | 100001 | F1 | 49 | 110001 | 13 |
| 2 | 000010 | 8C | 18 | 010010 | DD | 34 | 100010 | 4C | 50 | 110010 | 60 |
| 3 | 000011 | FD | 19 | 010011 | F6 | 35 | 100011 | 45 | 51 | 110011 | C5 |
| 4 | 000100 | B9 | 20 | 010100 | A6 | 36 | 100100 | 63 | 52 | 110100 | 56 |
| 5 | 000101 | E2 | 21 | 010101 | 43 | 37 | 100101 | 2C | 53 | 110101 | F2 |
| 6 | 000110 | 40 | 22 | 010110 | 11 | 38 | 100110 | 40 | 54 | 110110 | 89 |
| 7 | 000111 | C2 | 23 | 010111 | 17 | 39 | 100111 | 98 | 55 | 110111 | 9E |
| 8 | 001000 | D | 24 | 011000 | 98 | 40 | 101000 | 91 | 56 | 111000 | 6 |
| 9 | 001001 | 9A | 25 | 011001 | 88 | 41 | 101001 | 65 | 57 | 111001 | E2 |
| 10 | 001010 | D1 | 26 | 011010 | 8 | 42 | 101010 | E | 58 | 111010 | В |
| 11 | 001011 | F8 | 27. | 011011 | 6A | 43 | 101011 | 76 | 59 | 111011 | A2 |
| 12 | 001100 | 43 | 28 | 011100 | 6D | 44 | 101100 | EE | 60 | 111100 | B2 |
| 13 | 001101 | 7E | 29 | 011101 | B8 | 45 | 101101 | 5D | 61 | 111101 | 41 |
| 14 | 001110 | B7 | 30 | 011110 | BC | 46 | 101110 | 18 | 62 | 111110 | B1 |
| 15 | 001111 | 75 | 31 | 011111 | 12 | 47 | 101111 | 29 | 63 | 111111 | 7B |

Please implement a two way set associative cache for this memory system as shown below:

C) Set Associative Cache of Size 8 words and set size 2 with FIFO replacement.

| set | Tag | Data | tag | Data |
|-----|-----|------|-----|------|
| 0 | | | | |
| 1 | | | | |
| 2 | | | | |
| 3 | | | | |

- 1. Use the high level programming language of your choice to implement this project. The final product should be able to be tested on my office laptop.
- 2. Your project should fulfill the following functions:
 - a. Allow user to input any requested memory address
 - b. The cache simulator will use the input address and try to find it in cache.
 - c. If the data requested is in the cache, output "Cache Hit" and output the requested data along with it; if the data requested is not in the cache, the project should output "Cache Miss", and also bring in the data from memory to the corresponding cache location.
 - d. No matter you will have GUI or not, the small cache should be displayed and updated as each time the user input memory address to request data. The display of the small memory is optional.
 - e. Please submit your project through moodle link and provide with detailed instructions on how to test your project. (Readme.txt file).