# 9

# 嵌入式深度神經網路

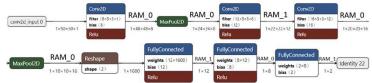
# M11102142 張祈安 M11102270 黎姿伶 嵌入式深度神經網路處理 Embedded Deep Neural Network Processing

# 一、設計理念

本研究在PYNQ板上對PS端進行Verilog編寫,並完成CNN模型在 Vivado中的設計,以確保所設計的硬體模塊能夠正確且有效地被 PYNQ板上的可程式邏輯 (PL) 部分使用。

# 二、架構

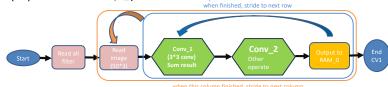
# (一)本研究的CNN model架構如下:



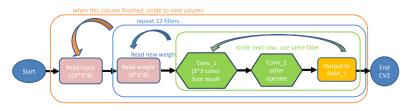
其中不同model讀取與寫入標示RAM\_0、RAM\_1,並非代表多使用一個RAM,而是將原本RAM拆成兩半使用,目的在於不讓還未處理的值被覆蓋掉,RAM示意圖於圖一,0~32767代表RAM\_0,32767~65535代表RAM\_1。

RAM\_0 RAM\_1
0 32,767 65535=2<sup>16</sup>-1

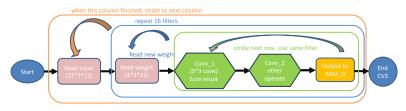
## (二) Convolution1架構:



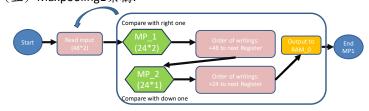
### (三) Convolution2架構:



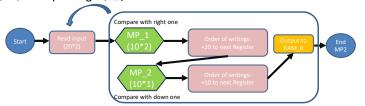
#### (四) Convolution3架構:



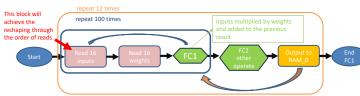
# (五) Maxpooling1架構:



# (六) Maxpooling2架構:



## (七) Fully Connected1架構:



#### (八) Fully Connected2架構:



#### (九) Fully Connected3架構:



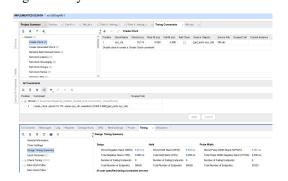
# 三、資源利用率和時序分析

模擬時的總clock cycles數:12,426,164.5

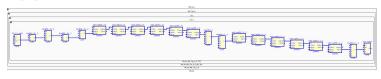
# (一) Utilization:

Name ^1	Slice LUTs (53200)	Slice Registers (106400)	F7 Muxes (26600)	F8 Muxes (13300)	Sāce (13300)	LUT as Logic (53200)	LUT as Memory (17400)	Block RAM Tile (140)	DSPs (220)	Bonded IOPADs (130)	BUFGCTRL (32)
∨ N Lab_final_bd_wrapper	17909	29490	1398	519	9333	17746	163	27.5	4	130	ė
→ II Lab_final_bd_i (Lab_final_bd)	17909	29490	1398	519	9333	17746	163	27.5	4	0	
> II axi_dma_0 (Lab_final_bd_ax	1175	1764	0	0	416	1087	88	2	0	0	
> II axi_mem_intercon (Lab_fina	482	579	0	0	198	469	13	0	0	0	
> II bk_ram_inimg (Lab_final_bc	0	0	0	0	0	0	0	1	0	0	
> myip_v1_0_0 (Lab_final_bd_	107	278	0	0	71	107	0	0	0	0	
> III NN (NN_imp_13PLRVM)	15614	26181	1398	519	8372	15614	0	24.5	4	0	
> II processing_system7_0 (Lat	0	0	0	0	0	0	0	0	0	0	,
> II ps7_0_axi_periph (Lab_final	514	655	0	0	229	453	61	0	0	0	
> II ret_ps7_0_50M (Lab_final_b	17	33	0	0	11	16	1	0	0	0	(
> II blk_ram_temp (Lab_final	14	1	0	0	14	14	0	16	0	0	
NN (NN_imp_13PLRVM)	15614	26181	1398	519	8372	15614	0	24.5	4	0	
> II blk_rom_other_weight (L:	0	0	0	0	0	0	0	0.5	0	0	
>   bk_rom_weight (Lab_fine	20	6	8	0	7	20	0	8	0	0	
↓ II NN_Top_0 (Lab_final_bid)	15580	26174	1390	519	8363	15580	0	0	4	0	
→ III inst (Lab final bd NN)	15575										
	100/0	26174	1390	519	8363	15575	0	0	- 4	0	
ConV_1 (Lab_final)	2875	26174 3915	1390	519 31	8363 1340	15575 2875	0	0	4 2	0	
ConV_1 (Lab_final)	2875	3915	130	31	1340	2875	0	0	2	0	
ConV_1 (Lab_final_ ConV_2 (Lab_final_	2875 3531	3915 6657	130 220	31 64	1340 1986	2875 3531	0	0	2	0	
CortV_1 (Lab_final) CortV_2 (Lab_final) CortV_3 (Lab_final)	2875 3531 4236	3915 6657 8690	130 220 963	31 64 412	1340 1986 2987	2875 3531 4236	0	0 0	0 0	0	
[] ConV_1 (Lab_final_ [] ConV_2 (Lab_final_ [] ConV_3 (Lab_final_br	2875 3531 4236 1216	3915 6657 8690 1675	130 220 963 39	31 64 412 12	1340 1986 2987 553	2875 3531 4236 1215	0 0 0	0 0 0	0 0 2	0 0 0	
ConV_1 (Lab_final)     ConV_2 (Lab_final)     ConV_3 (Lab_final)     FC_1 (Lab_final_b)     FC_2 (Lab_final_b)	2875 3531 4236 1215 1205	3915 6657 8690 1675 1592	130 220 963 39 12	31 64 412 12 0	1340 1986 2987 563 516	2875 3531 4238 1215 1205	0 0 0 0	0 0 0 0	2 0 0 2	0 0 0	
() CortV_1 (Lab_final, () CortV_2 (Lab_final, () CortV_3 (Lab_final, () FC_1 (Lab_final, b) () FC_2 (Lab_final, b) () FC_2 (Lab_final, b) () FC_3 (Lab_final, b)	2875 3531 4236 1215 1205 1106	3915 6657 8690 1676 1592 1539	130 220 963 39 12 26	31 64 412 12 0	1340 1986 2987 563 516 526	2875 3531 4238 1215 1205 1106	0 0 0 0 0	0 0 0 0 0	2 0 0 2 0	0 0 0 0	

# (二) Timing Summary:



#### (三) Critical Path:



#### 四、結論

在PYNQ板上對PS端進行Verilog編寫,需要仔細執行合成、實現和生成位流等步驟,以確保設計能夠在FPGA上正確運行,同時滿足時序和面積的要求。