嵌入式深度神經網路

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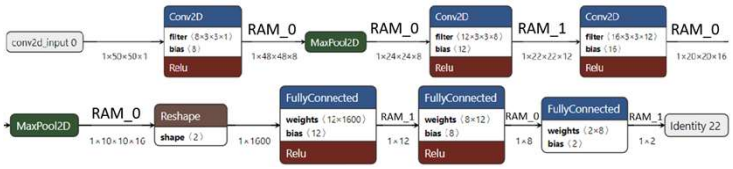
嵌入式深度神經網路處理 Embedded Deep Neural Network Processing

一、設計理念

本研究在PYNQ板上對PS端進行Verilog編寫，並完成CNN模型在Vivado中的設計，以確保所設計的硬體模塊能夠正確且有效地被PYNQ板上的可程式邏輯（PL）部分使用。

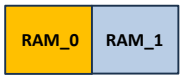
二、架構

(一)本研究的CNN model架構如下:



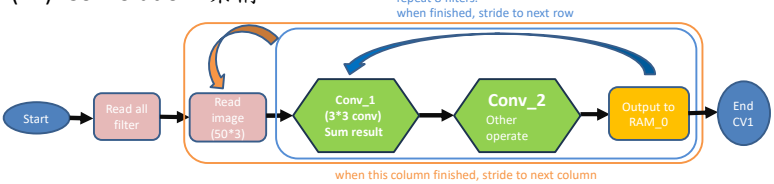
其中不同model讀取與寫入標示RAM_0、RAM_1，並非代表多使用一個RAM，而是將原本RAM拆成兩半使用，目的在於不讓還未處理的值被覆蓋掉，RAM示意圖於圖一，0~32767代表RAM_0，32767~65535代表RAM_1。

圖一、

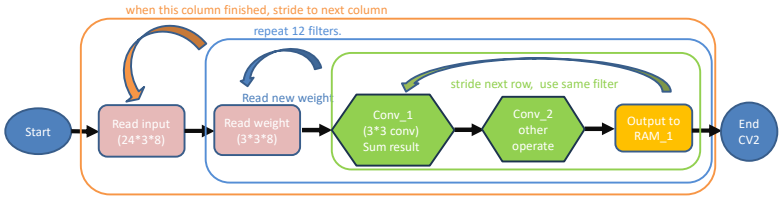


0　　32,767　65535=2^{16}-1

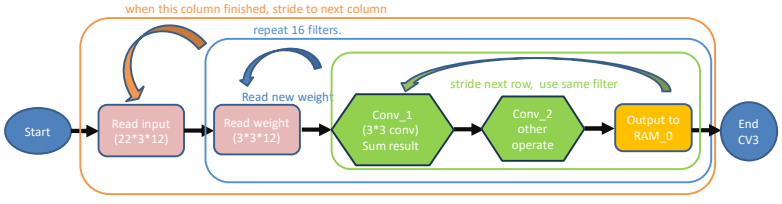
(二) Convolution1架構:



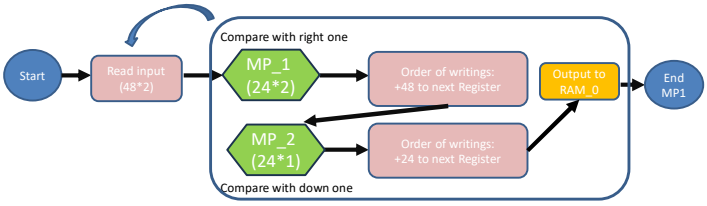
（三）Convolution2架構:



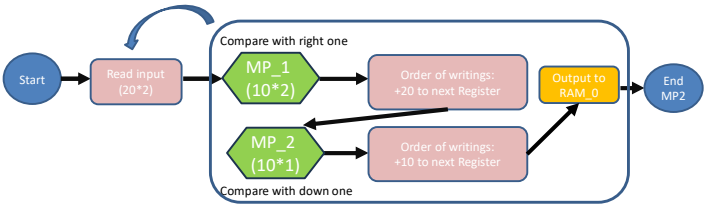
（四）Convolution3架構:



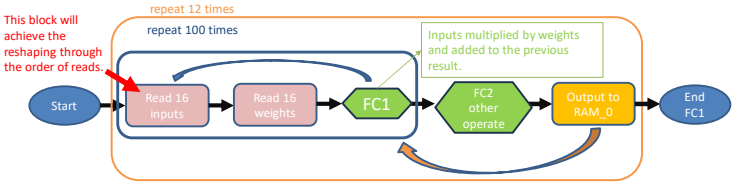
（五）Maxpooling1架構:



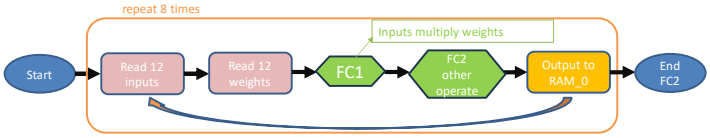
（六）Maxpooling2架構:



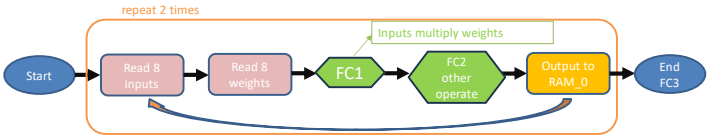
（七）Fully Connected1架構:



（八）Fully Connected2架構:



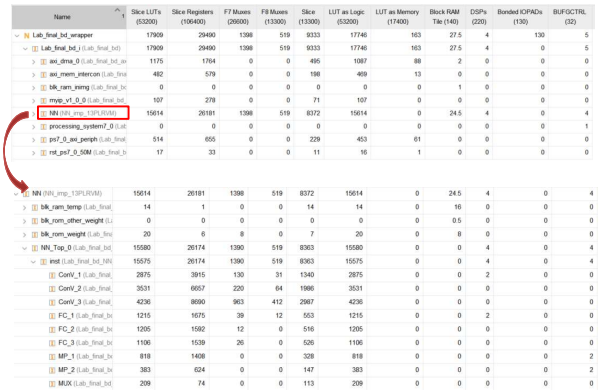
（九）Fully Connected3架構:



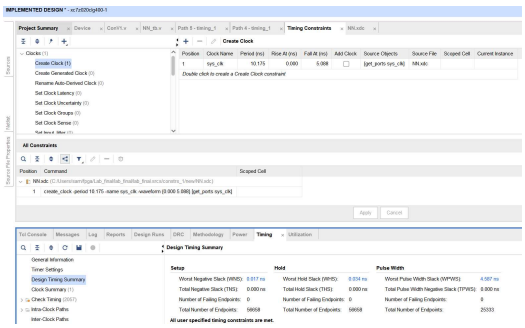
三、資源利用率和時序分析

模擬時的總clock cycles數:12,426,164.5

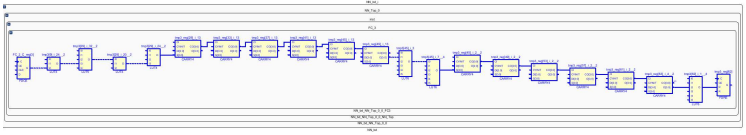
(一) Utilization:



(二) Timing Summary:



(三) Critical Path:



四、結論

在PYNQ板上對PS端進行Verilog編寫，需要仔細執行合成、實現和生成位流等步驟，以確保設計能夠在FPGA上正確運行，同時滿足時序和面積的要求。