2021 Digital IC Design Homework 1

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Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	X

```
#         502 data is correct
#         503 data is correct
#         504 data is correct
#         505 data is correct
#         506 data is correct
#         507 data is correct
#         508 data is correct
#         509 data is correct
#         510 data is correct
#         511 data is correct
# --------------------PASS--------------------
# All data have been generated successfully!
# Break in Module RCA_tb at C:/Users/user/Desktop/DIC/HW1/RCA_tb.v line 45
```

```
#         502 data is correct
#         503 data is correct
#         504 data is correct
#         505 data is correct
#         506 data is correct
#         507 data is correct
#         508 data is correct
#         509 data is correct
#         510 data is correct
#         511 data is correct
# --------------------PASS--------------------
# All data have been generated successfully!
# Break in Module RCA_tb at C:/Users/user/Desktop/DIC/HW1_upload/HW1/postsim/RCA_
```

Synthesis Result

Total logic elements	10
Total memory bit	0
Embedded multiplier 9-bit element	0
Clock Width (Cycle)	2

Flow Summary

Flow Status	Successful - Wed Mar 31 21:51:39 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	RCA
Top-level Entity Name	RCA
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	10 / 68,416 (< 1 %)
Total combinational functions	10 / 68,416 (< 1 %)
Dedicated logic registers	0 / 68,416 (0 %)
Total registers	0
Total pins	14 / 622 (2 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

先使用一個 XOR 和 AND gate 組合出一個半加器，再透過將兩個半加器以及一個 OR gate 組合成一個全加器，最後再將四個全加器串接在一起即可得到一個完整的 4bit RCA