# 2021 Digital IC Design Homework 3

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|---|---|
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**Simulation Result**

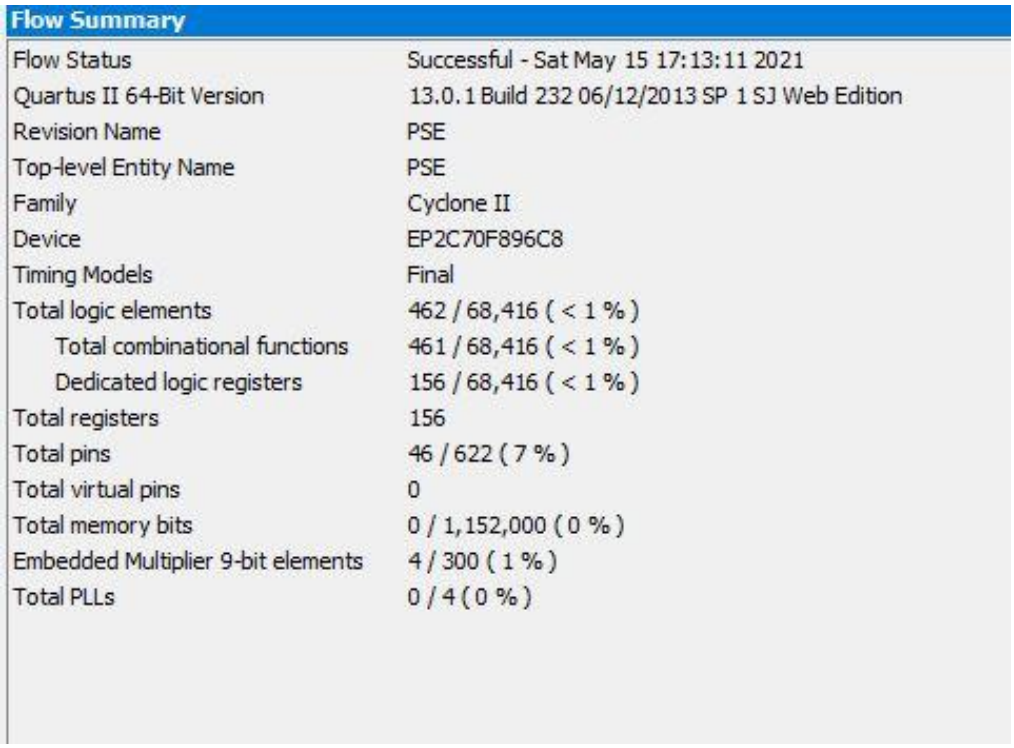
| Functional simulation | Pass | Gate-level simulation | Pass | Gate-level simulation time | 37050 (ns) |
|---|---|---|---|---|---|


(your pre-sim result)


(your post-sim result)

**Synthesis Result**

| Total logic elements | 462 |
|---|---|
| Total memory bit | 0 |
| Embedded multiplier 9-bit element | 4 |
| Clock width (Cycle) | 50 |



| Flow Summary | |
|---|---|
| Flow Status | Successful - Sat May 15 17:13:11 2021 |
| Quartus II 64-Bit Version | 13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition |
| Revision Name | PSE |
| Top-level Entity Name | PSE |
| Family | Cyclone II |
| Device | EP2C70F896C8 |
| Timing Models | Final |
| Total logic elements | 462 / 68,416 ( < 1 % ) |
| Total combinational functions | 461 / 68,416 ( < 1 % ) |
| Dedicated logic registers | 156 / 68,416 ( < 1 % ) |
| Total registers | 156 |
| Total pins | 46 / 622 ( 7 % ) |
| Total virtual pins | 0 |
| Total memory bits | 0 / 1,152,000 ( 0 % ) |
| Embedded Multiplier 9-bit elements | 4 / 300 ( 1 % ) |
| Total PLLs | 0 / 4 ( 0 % ) |

(your flow summary)

**Description of your design**

總共將程式碼分成四個區塊，state register、next state logic、data register、control signal。State register 和 next state logic 是負責狀態轉換的，data register 則是負責每個 clk 需要存值的部分，最後 control signal 是負責一些像是 bubble sort 或是轉換 state 所需的 count 訊號。而我的 state 狀態共有三個，第一個 state S0 是將資料一個一個讀進 x、y 陣列裡面儲存，第二個 state S1 是會利用由組合電路所算出來的外積來進行氣泡排序的判斷，最後一個 state S2 則是用來將資料一個 clk 一個 clk 讀出。

*Scoring = Total logic elements*