2021 Digital IC Design Homework 2

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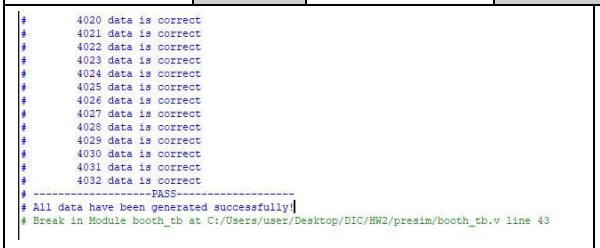
Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	X



Synthesis Result

Total logic elements	107
Total memory bit	0
Embedded multiplier 9-bit element	0
Clock width (Cycle)	27

Flow Summary

Flow Status	Successful - Fri Apr 09 17:36:17 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	booth
Top-level Entity Name	booth
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	107 / 68,416 (< 1 %)
Total combinational functions	107 / 68,416 (< 1 %)
Dedicated logic registers	0 / 68,416 (0 %)
Total registers	0
Total pins	24 / 622 (4 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

透過{} operator 將中間值 P 給連接好，之後以 case 語法將 P 的最小的兩個 bit 可能會遇到的狀態各別寫出該如何處理。
而因為這次作業是 combination circuit，表示每一次的乘法計算都必須在一個 cycle 內完成，因此會有重複六份的 case 狀態，來讓多次的移位以及運算動作一口氣在一個 cycle 內完成。

Scoring = Clock width