2021 Digital IC Design Homework 4

NAME	鄭丞祥
Student ID	N26094891

Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	5308511 (ns)

(your pre-sim result)

(your post-sim result)

Synthesis Result

Total logic elements	617
Total memory bit	0
Embedded multiplier 9-bit element	0
Clock width (Cycle)	21.6

Flow Summary

Flow Status	Successful - Sun May 30 18:37:43 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	MFE
Top-level Entity Name	MFE
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	617 / 68,416 (< 1 %)
Total combinational functions	608 / 68,416 (< 1 %)
Dedicated logic registers	246 / 68,416 (< 1 %)
Total registers	246
Total pins	57 / 622 (9 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

(your flow summary)

Description of your design

此次作業會分成 next state logic、control logic、calculate coordinate、compute value 這四個部分，next state logic、control logic 就顧名思義，用來判斷狀態甚麼時候要變化，control logic 則再用來控制 calculate coordinate、9 filter value 這兩塊電路所需要的訊號線，calculate coordinate 的部分會透過 column counter 和 row column 來去決定 iaddr 的大小，判斷甚麼時候該拿甚麼數值，並且在特定 state 下會將 column、row 做數值的增加，以及拿取中間值放回原 pixel，最後是 9 filter value，這塊電路是用來製作 filter 每個 pixel 的數值，以即將 filter 的中間值透過排序電路算出來以利 calculate coordinate 這塊電路可以拿到正確的中間值。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (longest gate-level simulation time in ns)*