2021 Digital IC Design Homework 5

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Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	36236(ns)

Tb1

```
# FFT dataout on pattern         880 ~         895, PASS!!
# FFT dataout on pattern         896 ~         911, PASS!!
# FFT dataout on pattern         912 ~         927, PASS!!
# FFT dataout on pattern         928 ~         943, PASS!!
# FFT dataout on pattern         944 ~         959, PASS!!
# FFT dataout on pattern         960 ~         975, PASS!!
# FFT dataout on pattern         976 ~         991, PASS!!
# FFT dataout on pattern         992 ~        1007, PASS!!
# FFT dataout on pattern        1008 ~        1023, PASS!!
# ------------------------------------------------------
#
# Congratulations! All data have been generated successfully!
#
# -------------------------PASS-------------------------
#
# ** Note: $finish    : C:/Users/user/Desktop/DIC/HW5/presim_tb1/testfixture1.v(240)
#    Time: 56600 ns  Iteration: 0  Instance: /testfixture1
# 1
# Break in Module testfixture1 at C:/Users/user/Desktop/DIC/HW5/presim_tb1/testfixture1.v line 240
```

Tb1

```
# FFT dataout on pattern         800 ~         815, PASS!!
# FFT dataout on pattern         816 ~         831, PASS!!
# FFT dataout on pattern         832 ~         847, PASS!!
# FFT dataout on pattern         848 ~         863, PASS!!
# FFT dataout on pattern         864 ~         879, PASS!!
# FFT dataout on pattern         880 ~         895, PASS!!
# FFT dataout on pattern         896 ~         911, PASS!!
# FFT dataout on pattern         912 ~         927, PASS!!
# FFT dataout on pattern         928 ~         943, PASS!!
# FFT dataout on pattern         944 ~         959, PASS!!
# FFT dataout on pattern         960 ~         975, PASS!!
# FFT dataout on pattern         976 ~         991, PASS!!
# FFT dataout on pattern         992 ~        1007, PASS!!
# FFT dataout on pattern        1008 ~        1023, PASS!!
# ------------------------------------------------------
#
# Congratulations! All data have been generated successfully!
#
# -------------------------PASS-------------------------
#
# ** Note: $finish    : C:/Users/user/Desktop/DIC/HW5/postsim_tb1/testfixture1.v(240)
#    Time: 36236263 ps  Iteration: 0  Instance: /testfixture1
# 1
# Break in Module testfixture1 at C:/Users/user/Desktop/DIC/HW5/postsim_tb1/testfixture1.v line 240
```

Tb2

```
# FFT dataout on pattern         864 ~         879, PASS!!
# FFT dataout on pattern         880 ~         895, PASS!!
# FFT dataout on pattern         896 ~         911, PASS!!
# FFT dataout on pattern         912 ~         927, PASS!!
# FFT dataout on pattern         928 ~         943, PASS!!
# FFT dataout on pattern         944 ~         959, PASS!!
# FFT dataout on pattern         960 ~         975, PASS!!
# FFT dataout on pattern         976 ~         991, PASS!!
# FFT dataout on pattern         992 ~        1007, PASS!!
# FFT dataout on pattern        1008 ~        1023, PASS!!
# ------------------------------------------------------
#
# Congratulations! All data have been generated successfully!
#
# -------------------------PASS-------------------------
#
# ** Note: $finish    : C:/Users/user/Desktop/DIC/HW5/presim_tb2/testfixture2.v(241)
#    Time: 11320 ns  Iteration: 0  Instance: /testfixture1
# 1
# Break in Module testfixture1 at C:/Users/user/Desktop/DIC/HW5/presim_tb2/testfixture2.v line 241
```

Tb2

```
# FFT dataout on pattern         784 ~         799, PASS!!
# FFT dataout on pattern         800 ~         815, PASS!!
# FFT dataout on pattern         816 ~         831, PASS!!
# FFT dataout on pattern         832 ~         847, PASS!!
# FFT dataout on pattern         848 ~         863, PASS!!
# FFT dataout on pattern         864 ~         879, PASS!!
# FFT dataout on pattern         880 ~         895, PASS!!
# FFT dataout on pattern         896 ~         911, PASS!!
# FFT dataout on pattern         912 ~         927, PASS!!
# FFT dataout on pattern         928 ~         943, PASS!!
# FFT dataout on pattern         944 ~         959, PASS!!
# FFT dataout on pattern         960 ~         975, PASS!!
# FFT dataout on pattern         976 ~         991, PASS!!
# FFT dataout on pattern         992 ~        1007, PASS!!
# FFT dataout on pattern        1008 ~        1023, PASS!!
# ------------------------------------------------------
#
# Congratulations! All data have been generated successfully!
#
# -------------------------PASS-------------------------
#
# ** Note: $finish    : C:/Users/user/Desktop/DIC/HW5/postsim_tb2/testfixture2.v(241)
#    Time: 36236263 ps  Iteration: 0  Instance: /testfixture1
# 1
# Break in Module testfixture1 at C:/Users/user/Desktop/DIC/HW5/postsim_tb2/testfixture2.v line 241
```

Synthesis Result

Total logic elements	29876
Total memory bit	0
Embedded multiplier 9-bit element	278
Clock width (Cycle)	32

Flow Summary	
Flow Status	Successful - Mon Jun 28 16:55:00 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	FAS
Top-level Entity Name	FAS
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	29,876 / 68,416 (44 %)
Total combinational functions	21,594 / 68,416 (32 %)
Dedicated logic registers	20,164 / 68,416 (29 %)
Total registers	20164
Total pins	554 / 622 (89 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	278 / 300 (93 %)
Total PLLs	0 / 4 (0 %)

Description of your design

這次作業依照 spec 的要求，總共分成了三個 part，分別是 FIR 電路，FFT 電路以及 analysis 電路，FIR 電路的話因為其係數有對稱性，所以我將乘上相同數值的資料先做相加後儲存在 add_x 裡面，再將它拿去乘上係數，等所有乘上係數的值都出來以後再做最後的相加。

FFT 電路的話他因為一次要吃 16 筆 data，所以 FIR 出來的資料會先存進一個 1024 大小的 reg，而這個 reg 我利用 counter 的方式去取出現在要哪 16 筆資料給 FFT，FFT 基本的組成是 BU，而因為是 16 點的 FFT，每一層會有 8 個 BU，因此 4 級共會有 32 個 BU 去計算。

最後是分析電路，因為分析電路是要看 FFT 出來的頻率哪個做平方和才是最大的，因此會先用暫存器將每一組的每個頻率算出來的平方和存起來並相加，等到 64 組 FFT output 都計算後就得到每個頻率的平方和相加總和。

最後將這些頻率總和拿去求最大值即可求出 freq 的答案。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (longest gate-level simulation time in ns)*