DRAM Simulator

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Outline

▶ Introduction

▶ DRAM controller

▶ Simplified DRAM Simulator

❯ Timing Specification

❯ Waveform

Introduction

▶ Dynamic random-access memory (dynamic RAM or DRAM) is a type of random-access semiconductor memory.

▶ Consisting only a capacitor and a transistor for each bit of data.

▶ The electric charge on the capacitors slowly leaks off.

➤ refresh!

Introduction

■ Three Basic Operations
  ❯ Row Access
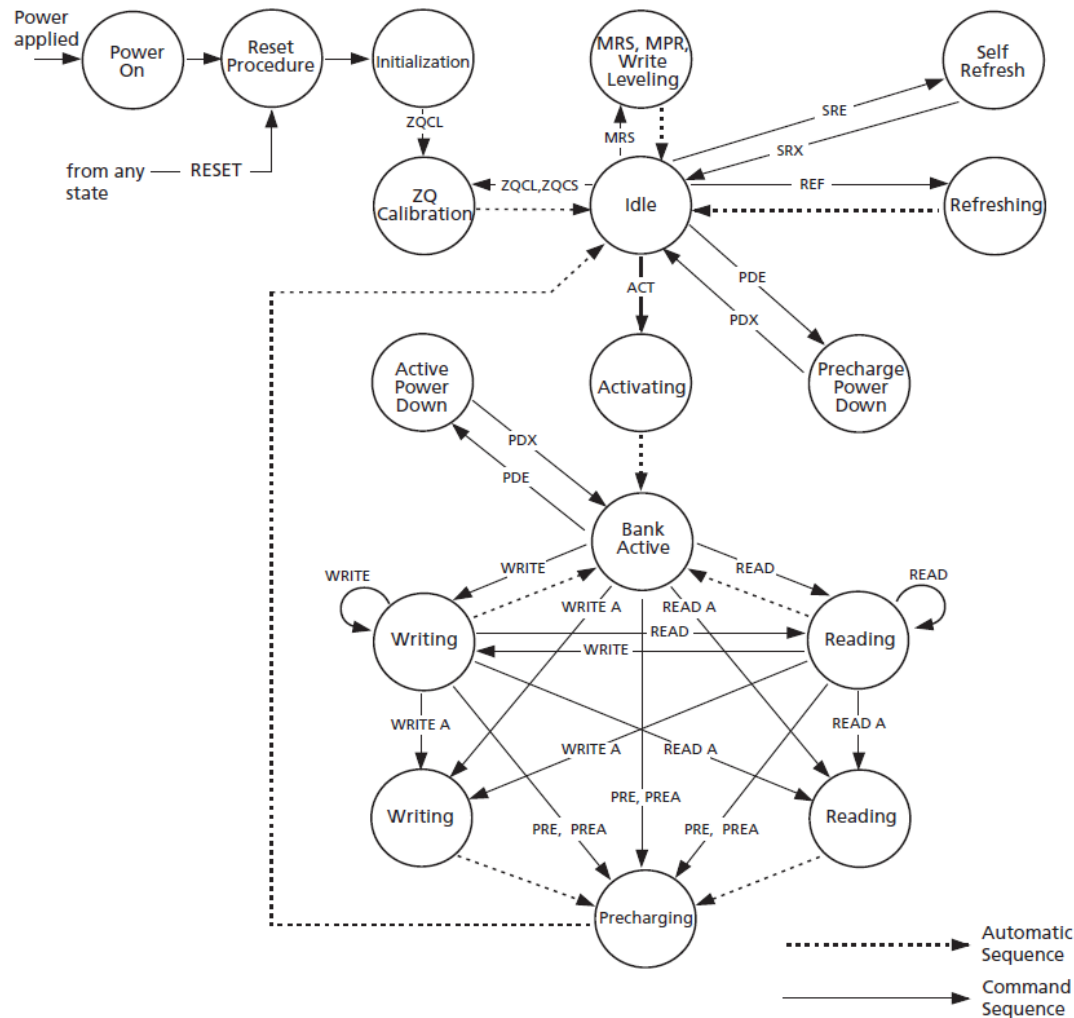 ❯ Column Access
  ❯ Pre-charge

DRAM controller
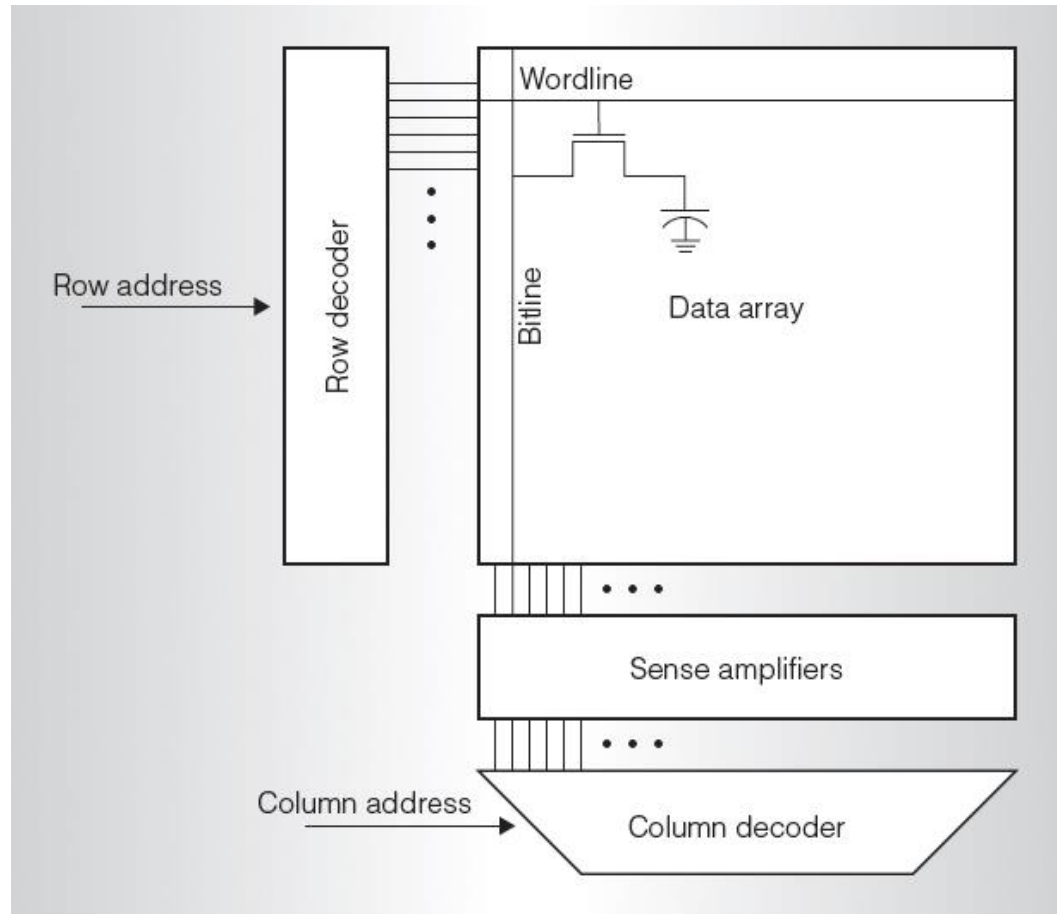
- Ensure correct operation of DRAM
  - Address Mapping, refresh and timing
- Translate request to DRAM command sequences
- Buffer and schedule requests to improve performance
  - Reordering, row-buffer, bank, rank, bus management
- Manage power consumption and thermals in DRAM
  - Turn off/on DRAM chips, manage power modes

DRAM controller

State diagram

Simplified DRAM Simulator

▶ Act : Activate row
- ▸ RASn = low
- ▸ CASn = high
- ▸ WEn = 4'hf

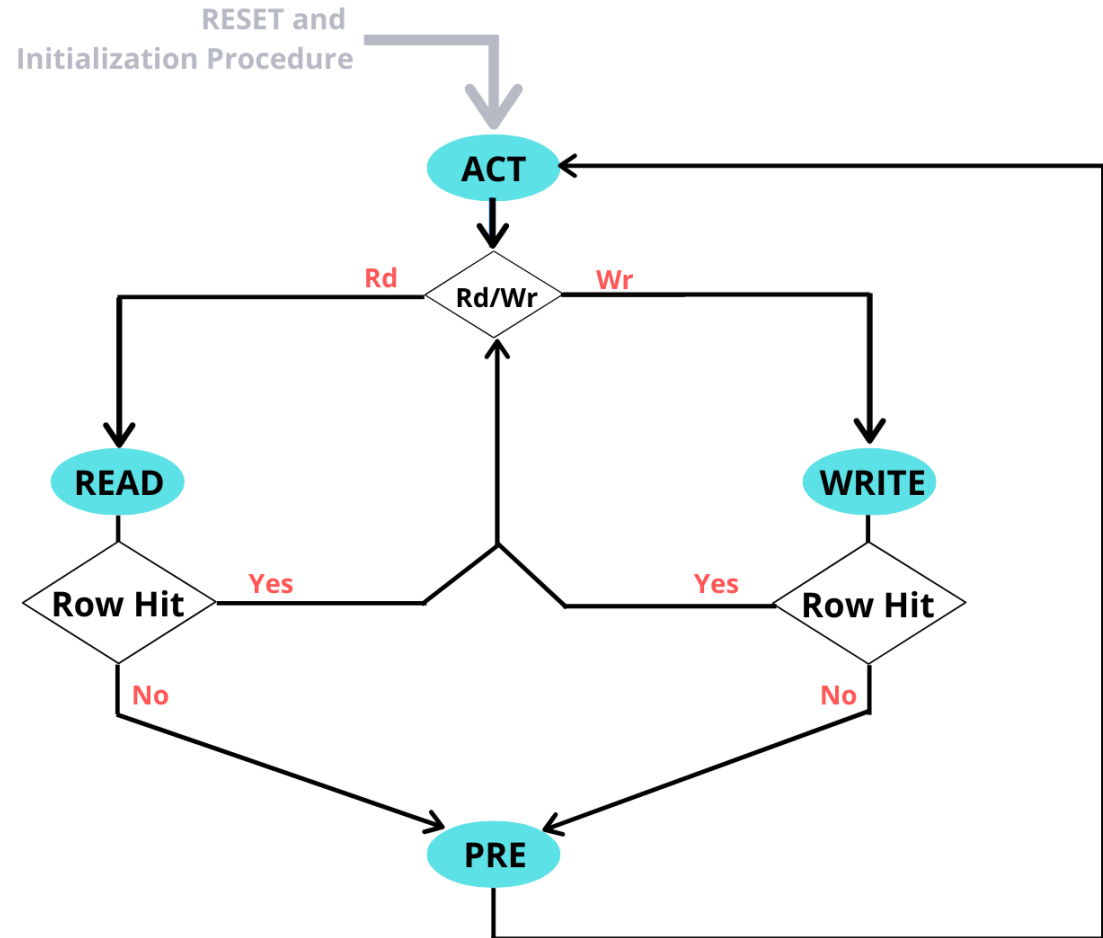▶ READ: Read operation and access column address
- ▸ RASn = high
- ▸ CASn = low
- ▸ WEn = 4'hf

▶ WRITE: Write operation and access column address
- ▸ RASn = high
- ▸ CASn = low
- ▸ WEn = 4'h0 (for a word)

▶ PRE : Pre-charge
- ▸ RASn = low
- ▸ CASn = high
- ▸ WEn = 4'h0
- ▸ The address should be the same as the one that activated last time.

RESET and
Initialization Procedure

ACT

Rd/Wr
Rd   Wr

READ   WRITE

Row Hit   Row Hit
Yes   Yes

No   No

PRE

Simplified DRAM Simulator

DRAM	System signals			
	CK	input	1	System clock
	RST	input	1	System reset (active high)
	Memory ports			
	CSn	input	1	DRAM Chip Select (active low)
	WEn	input	4	DRAM Write Enable (active low)
	RASn	input	1	DRAM Row Access Strobe (active low)
	CASn	input	1	DRAM Column Access Strobe (active low)
	A	input	11	DRAM Address input
	D	input	32	DRAM data input
	Q	output	32	DRAM data output
	VALID	output	1	DRAM data output valid
	Memory space			
	Memory_byte0	reg	8	Size: [0:2097151]
	Memory_byte1	reg	8	Size: [0:2097151]
	Memory_byte2	reg	8	Size: [0:2097151]
	Memory_byte3	reg	8	Size: [0:2097151]

★ Row address is 11-bit and column address is 10-bit

Timing Specification
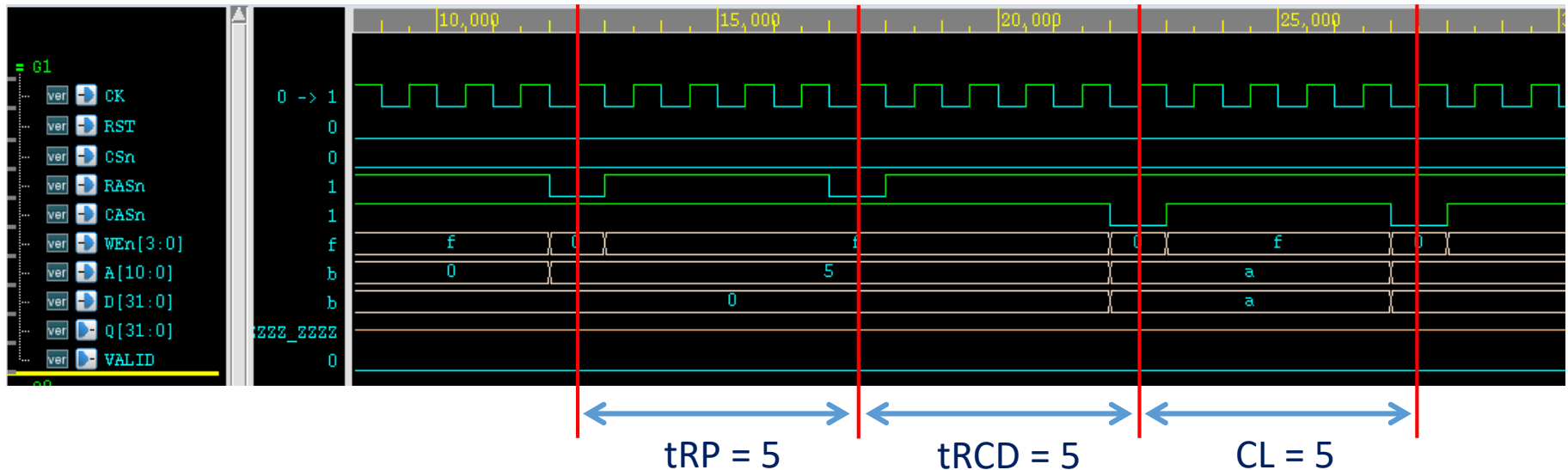
tRP -Precharge Time
Delay time until the next RAS is asserted

tRCD -Row Address to Column Address Delay
Active to Read/Write command time

CL -CAS Latency
Delay time between the READ command and the moment data is available

Timing Specification

▶ If the transition violates the timing specification, it will show error or terminates the execution .
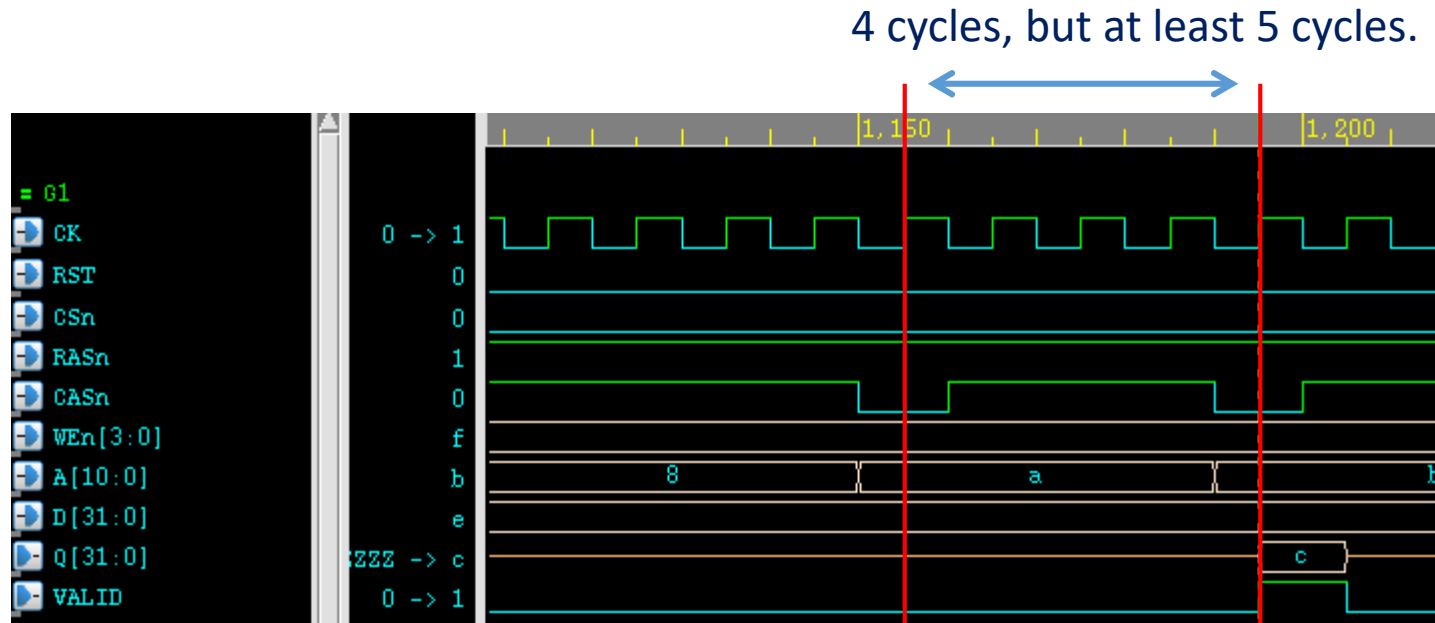
4 cycles, but at least 5 cycles.

Waveform

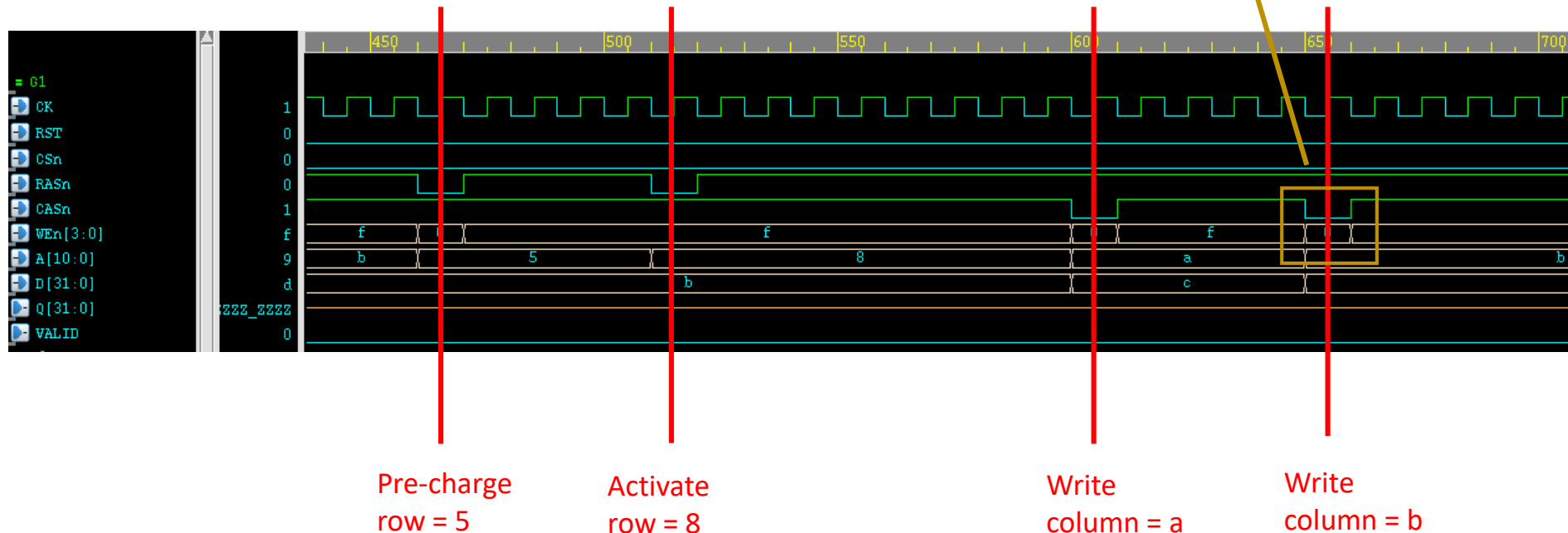▶ RAS → Set Row

> A should be ready

▶ CAS → Set Column

> READ : A and WEn should be ready

> WRITE : A, WEn and D should be ready
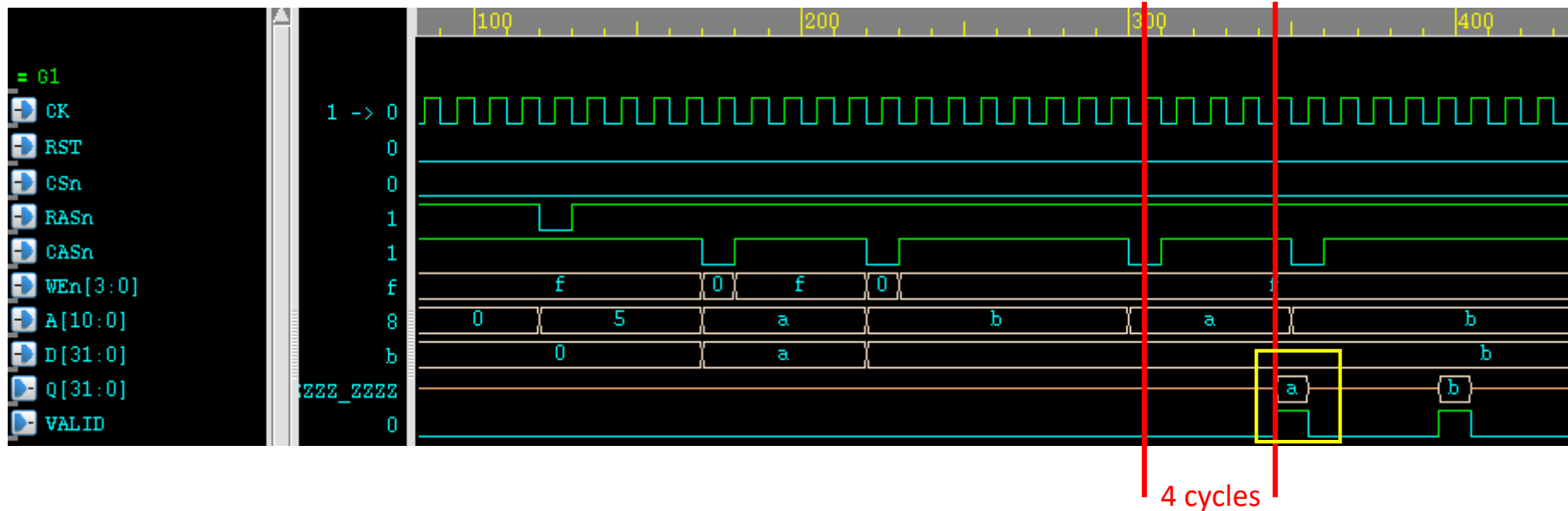
Read/Write command Registration
READ if WEn = 4'hf
WRITE if WEn != 4'hf

Pre-charge
row = 5

Activate
row = 8

Write
column = a

Write
column = b

Waveform

▶ Read operation

> Data will output with a valid signal

4 cycles

Thanks for listening