

2021 Digital IC Design Homework 2

NAME	楊承翰																																				
Student ID	NE6091124																																				
Simulation Result																																					
Functional simulation	none	Gate-level simulation	none	Gate-level simulation time	none																																
<pre># 4013 data is correct # 4014 data is correct # 4015 data is correct # 4016 data is correct # 4017 data is correct # 4018 data is correct # 4019 data is correct # 4020 data is correct # 4021 data is correct # 4022 data is correct # 4023 data is correct # 4024 data is correct # 4025 data is correct # 4026 data is correct # 4027 data is correct # 4028 data is correct # 4029 data is correct # 4030 data is correct # 4031 data is correct # 4032 data is correct # -----PASS----- # All data have been generated successfully! # Break in Module booth_tb at C:/Users/sam24/Desktop/DIC/hw2/file/presim/booth_tb.v line 43</pre>			<pre># 4013 data is correct # 4014 data is correct # 4015 data is correct # 4016 data is correct # 4017 data is correct # 4018 data is correct # 4019 data is correct # 4020 data is correct # 4021 data is correct # 4022 data is correct # 4023 data is correct # 4024 data is correct # 4025 data is correct # 4026 data is correct # 4027 data is correct # 4028 data is correct # 4029 data is correct # 4030 data is correct # 4031 data is correct # 4032 data is correct # -----PASS----- # All data have been generated successfully! # Break in Module booth_tb at C:/Users/sam24/Desktop/DIC/hw2/file/postsim/booth_tb.v line 43</pre>																																		
Synthesis Result																																					
Total logic elements			107																																		
Total memory bit			0																																		
Embedded multiplier 9-bit element			0																																		
Clock width (Cycle)			26																																		
Flow Summary																																					
<table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%;">Flow Status</td> <td>Successful - Sat Apr 03 19:37:58 2021</td> </tr> <tr> <td>Quartus II 64-Bit Version</td> <td>13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition</td> </tr> <tr> <td>Revision Name</td> <td>booth</td> </tr> <tr> <td>Top-level Entity Name</td> <td>booth</td> </tr> <tr> <td>Family</td> <td>Cyclone II</td> </tr> <tr> <td>Device</td> <td>EP2C70F896C8</td> </tr> <tr> <td>Timing Models</td> <td>Final</td> </tr> <tr> <td>Total logic elements</td> <td>107 / 68,416 (< 1 %)</td> </tr> <tr> <td> Total combinational functions</td> <td>107 / 68,416 (< 1 %)</td> </tr> <tr> <td> Dedicated logic registers</td> <td>0 / 68,416 (0 %)</td> </tr> <tr> <td>Total registers</td> <td>0</td> </tr> <tr> <td>Total pins</td> <td>24 / 622 (4 %)</td> </tr> <tr> <td>Total virtual pins</td> <td>0</td> </tr> <tr> <td>Total memory bits</td> <td>0 / 1,152,000 (0 %)</td> </tr> <tr> <td>Embedded Multiplier 9-bit elements</td> <td>0 / 300 (0 %)</td> </tr> <tr> <td>Total PLLs</td> <td>0 / 4 (0 %)</td> </tr> </table>						Flow Status	Successful - Sat Apr 03 19:37:58 2021	Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition	Revision Name	booth	Top-level Entity Name	booth	Family	Cyclone II	Device	EP2C70F896C8	Timing Models	Final	Total logic elements	107 / 68,416 (< 1 %)	Total combinational functions	107 / 68,416 (< 1 %)	Dedicated logic registers	0 / 68,416 (0 %)	Total registers	0	Total pins	24 / 622 (4 %)	Total virtual pins	0	Total memory bits	0 / 1,152,000 (0 %)	Embedded Multiplier 9-bit elements	0 / 300 (0 %)	Total PLLs	0 / 4 (0 %)
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Description of your design																																					

按照 booth algorithm 去完成
因為 width = 6
所以總共做六次
再依照最右兩 bits 去決定要做哪些事

Scoring = Clock width