

2021 Digital IC Design Homework 1

NAME	楊承翰																																				
Student ID	NE6091124																																				
Simulation Result																																					
Functional simulation	none	Gate-level simulation	none	Gate-level simulation time	none																																
<pre># 492 data is correct # 493 data is correct # 494 data is correct # 495 data is correct # 496 data is correct # 497 data is correct # 498 data is correct # 499 data is correct # 500 data is correct # 501 data is correct # 502 data is correct # 503 data is correct # 504 data is correct # 505 data is correct # 506 data is correct # 507 data is correct # 508 data is correct # 509 data is correct # 510 data is correct # 511 data is correct # -----PASS----- # All data have been generated successfully! # Break in Module RCA_tb at C:/Users/sam24/Desktop/DIC/hwl/file/presim/RCA_tb.v line 45</pre>			<pre># 492 data is correct # 493 data is correct # 494 data is correct # 495 data is correct # 496 data is correct # 497 data is correct # 498 data is correct # 499 data is correct # 500 data is correct # 501 data is correct # 502 data is correct # 503 data is correct # 504 data is correct # 505 data is correct # 506 data is correct # 507 data is correct # 508 data is correct # 509 data is correct # 510 data is correct # 511 data is correct # -----PASS----- # All data have been generated successfully! # Break in Module RCA_tb at C:/Users/sam24/Desktop/DIC/hwl/file/postsim/RCA_tb.v line 45</pre>																																		
Synthesis Result																																					
Total logic elements			10																																		
Total memory bit			0																																		
Embedded multiplier 9-bit element			0																																		
Clock Width (Cycle)			10																																		
<div>Flow Summary</div> <table><tr><td>Flow Status</td><td>Successful - Sat Apr 03 19:17:46 2021</td></tr><tr><td>Quartus II 64-Bit Version</td><td>13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition</td></tr><tr><td>Revision Name</td><td>RCA</td></tr><tr><td>Top-level Entity Name</td><td>RCA</td></tr><tr><td>Family</td><td>Cyclone II</td></tr><tr><td>Device</td><td>EP2C70F896C8</td></tr><tr><td>Timing Models</td><td>Final</td></tr><tr><td>Total logic elements</td><td>10 / 68,416 (< 1 %)</td></tr><tr><td> Total combinational functions</td><td>10 / 68,416 (< 1 %)</td></tr><tr><td> Dedicated logic registers</td><td>0 / 68,416 (0 %)</td></tr><tr><td>Total registers</td><td>0</td></tr><tr><td>Total pins</td><td>14 / 622 (2 %)</td></tr><tr><td>Total virtual pins</td><td>0</td></tr><tr><td>Total memory bits</td><td>0 / 1,152,000 (0 %)</td></tr><tr><td>Embedded Multiplier 9-bit elements</td><td>0 / 300 (0 %)</td></tr><tr><td>Total PLLs</td><td>0 / 4 (0 %)</td></tr></table>						Flow Status	Successful - Sat Apr 03 19:17:46 2021	Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition	Revision Name	RCA	Top-level Entity Name	RCA	Family	Cyclone II	Device	EP2C70F896C8	Timing Models	Final	Total logic elements	10 / 68,416 (< 1 %)	Total combinational functions	10 / 68,416 (< 1 %)	Dedicated logic registers	0 / 68,416 (0 %)	Total registers	0	Total pins	14 / 622 (2 %)	Total virtual pins	0	Total memory bits	0 / 1,152,000 (0 %)	Embedded Multiplier 9-bit elements	0 / 300 (0 %)	Total PLLs	0 / 4 (0 %)
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Description of your design																																					

按照 pdf 的說明

分別寫好 half-adder, full-adder, ripple-carry-adder