

## 2021 Digital IC Design Homework 5

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<b>Simulation Result</b>					
Functional simulation	<b>Pass</b>	Gate-level simulation	<b>Pass</b>	Gate-level simulation time	<b>19581 (ns)</b>
<pre> Transcript # FFT dataout on pattern 920 ~ 943, PASS!! # FFT dataout on pattern 944 ~ 969, PASS!! # FFT dataout on pattern 940 ~ 975, PASS!! # FFT dataout on pattern 976 ~ 991, PASS!! # FFT dataout on pattern 992 ~ 1007, PASS!! # FFT dataout on pattern 1008 ~ 1023, PASS!! # # Congratulations! All data have been generated successfully! # # -----PASS----- # ** Note: Cfinish : C:/Users/sam24/Desktop/sam/2020 winter/DIC/hw5/file/postain/testfigure1.v(240) Time: 10700 ns Iteration: 0 Instance: /testfigure1 </pre>		<pre> Transcript # FFT dataout on pattern 954 ~ 911, PASS!! # FFT dataout on pattern 912 ~ 927, PASS!! # FFT dataout on pattern 928 ~ 943, PASS!! # FFT dataout on pattern 944 ~ 959, PASS!! # FFT dataout on pattern 960 ~ 975, PASS!! # FFT dataout on pattern 976 ~ 991, PASS!! # FFT dataout on pattern 992 ~ 1007, PASS!! # FFT dataout on pattern 1008 ~ 1023, PASS!! # # Congratulations! All data have been generated successfully! # # -----PASS----- # ** Note: Cfinish : C:/Users/sam24/Desktop/sam/2020 winter/DIC/hw5/file/postain/testfigure2.v(241) Time: 19581 ns Iteration: 0 Instance: /testfigure2 # # Break in Module testfigure2 at C:/Users/sam24/Desktop/sam/2020 winter/DIC/hw5/file/postain/testfigure2.v line 241 </pre>			
<b>Synthesis Result</b>					
Total logic elements	4375				
Total memory bit	0				
Embedded multiplier 9-bit element	108				
Clock width (Cycle)	18.3				
<b>Flow Summary</b>					
Flow Status		Successful - Wed Jun 30 18:35:33 2021			
Quartus II 64-Bit Version		13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition			
Revision Name		FAS			
Top-level Entity Name		FAS			
Family		Cyclone II			
Device		EP2C70F896C8			
Timing Models		Final			
Total logic elements		4,375 / 68,416 ( 6 % )			
Total combinational functions		3,425 / 68,416 ( 5 % )			
Dedicated logic registers		3,126 / 68,416 ( 5 % )			
Total registers		3126			
Total pins		554 / 622 ( 89 % )			
Total virtual pins		0			
Total memory bits		0 / 1,152,000 ( 0 % )			
Embedded Multiplier 9-bit elements		108 / 300 ( 36 % )			
Total PLLs		0 / 4 ( 0 % )			
<b>Description of your design</b>					

因為這題 data 會一直輸入，所以我用 pipeline 讓資料可以一直往下傳，首先 FIR 的部分從第 32 個 clk 後才会有正確的值，然後我用 2 層 adder tree 來做相加避免 critical path 太大。

FFT 每個 stage 也都有切 pipeline，另外因為 fft\_coefficient 0,4 剛好是(1,0),(0,-1) 所以 stage3 之後的都不需要做乘法，直接作加法即可。

最後階段因為助教有提到只要算 1 跟 15，但是看 textfixture2，答案都是 1，所以我就只比 0,1,15 這三個頻段，取最大值並輸出該頻段

*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) × (longest gate-level simulation time in ns)*