2021 Digital IC Design Homework 3

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Simulation Result						
Functional		Gate-level		Gate-level	0-1-0/	
simulation	Pass	simulation	Pass	simulation time	85450 (ns)	
# Object43: PASS Object44: FASS Object44: FASS Object47: PASS Object48: PASS Obje						
Synthesis Result						
Total logic elements			453	453		
Total memory bit			0	0		
Embedded multiplier 9-bit element			2	2		
Clock width (Cycle)			50	50		
Flow Summary						
				ssful - Thu May 13 13:	:46:48 2021	
				13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition		
			PSE	PSE		
Top-level Entity Name			PSE	PSE		
Family			Cyclo	Cyclone II		
Device E			EP2C	EP2C70F896C8		
Timing Models			Final	Final		
Total logic elements			453 /	453 / 68,416 (< 1 %)		
Total combinational functions			453 /	453 / 68,416 (< 1 %)		
Dedicated logic registers			197 /	197 / 68,416 (< 1 %)		
Total registers			197	197		
Total pins			46 / 6	46 / 622 (7 %)		
Total virtual pins			0	0		
Total memory bits			0 / 1,	0 / 1,152,000 (0 %)		
Embedded Multiplier 9-bit elements			2/30	2 / 300 (< 1 %)		
Total PLLs (0/4	0/4(0%)		
Description of your design						

我先寫了一個 FSM 來控制 data 的 input 及 output

分成四個 state

第一個 reset

用來 reset 各個 reg 的

第二個 load

會根據輸入的 point_num 的值來決定要跑幾個 cycle, 每個 cycle 會去讀 Xin,

Yin 並分別存到 coordinate_x, coordinate_y

第三個 sort

做 bubble sort

第四個 write

依序將排序好的座標送給 Xout,Yout

Scoring = Total logic elements