2021 Digital IC Design Homework 2

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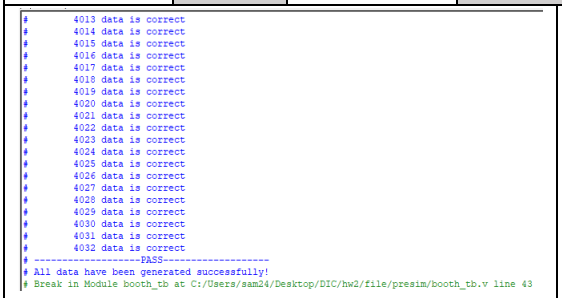
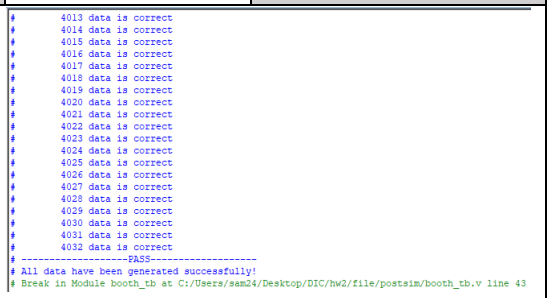
Simulation Result

Functional simulation	none	Gate-level simulation	none	Gate-level simulation time	none





Synthesis Result

Total logic elements	107
Total memory bit	0
Embedded multiplier 9-bit element	0
Clock width (Cycle)	26

Flow Summary

Flow Status	Successful - Sat Apr 03 19:37:58 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	booth
Top-level Entity Name	booth
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	107 / 68,416 (< 1 %)
Total combinational functions	107 / 68,416 (< 1 %)
Dedicated logic registers	0 / 68,416 (0 %)
Total registers	0
Total pins	24 / 622 (4 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

按照 booth algorithm 去完成
因為 width = 6
所以總共做六次
再依照最右兩 bits 去決定要做哪些事

Scoring = Clock width