

2021 Digital IC Design Homework 4

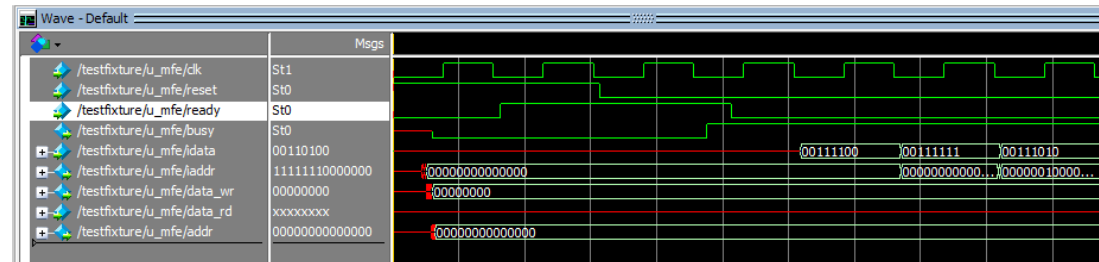
NAME	楊承翰																																						
Student ID	NE6091124																																						
Simulation Result																																							
Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	3733677.09 (ns)																																		
<pre> # Transcript: # ----- # Result image is correct ! # ----- # S U M M A R Y ----- # Congratulations! Result image data have been generated successfully! The result is PASS!! # ----- # ** Note: \$finish : C:/Users/sam24/Desktop/DIC/bw4/file/presim/testfixture.v(123) # Time: 6140900 ns Iteration: 0 Instance: /testfixture # 1 # Break in Module testfixture at C:/Users/sam24/Desktop/DIC/bw4/file/presim/testfixture.v line 123 </pre>		<pre> # Transcript # ----- # QSM2> run -all # ----- # START!!! Simulation Start # ----- # Result image is correct ! # ----- # S U M M A R Y ----- # Congratulations! Result image data have been generated successfully! The result is PASS!! # ----- # ** Note: \$finish : C:/Users/sam24/Desktop/DIC/bw4/file/postsim/testfixture.v(123) # Time: 3733677090 ps Iteration: 0 Instance: /testfixture # 1 # Break in Module testfixture at C:/Users/sam24/Desktop/DIC/bw4/file/postsim/testfixture.v line 123 </pre>																																					
Synthesis Result																																							
Total logic elements		490																																					
Total memory bit		0																																					
Embedded multiplier 9-bit element		0																																					
Clock width (Cycle)		15.2																																					
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #0070C0; color: white;"> <th colspan="2">Flow Summary</th> </tr> </thead> <tbody> <tr> <td>Flow Status</td> <td>Successful - Tue Jun 01 10:52:52 2021</td> </tr> <tr> <td>Quartus II 64-Bit Version</td> <td>13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition</td> </tr> <tr> <td>Revision Name</td> <td>MFE</td> </tr> <tr> <td>Top-level Entity Name</td> <td>MFE</td> </tr> <tr> <td>Family</td> <td>Cyclone II</td> </tr> <tr> <td>Device</td> <td>EP2C70F896C8</td> </tr> <tr> <td>Timing Models</td> <td>Final</td> </tr> <tr> <td>Total logic elements</td> <td>490 / 68,416 (< 1 %)</td> </tr> <tr> <td> Total combinational functions</td> <td>461 / 68,416 (< 1 %)</td> </tr> <tr> <td> Dedicated logic registers</td> <td>197 / 68,416 (< 1 %)</td> </tr> <tr> <td>Total registers</td> <td>197</td> </tr> <tr> <td>Total pins</td> <td>57 / 622 (9 %)</td> </tr> <tr> <td>Total virtual pins</td> <td>0</td> </tr> <tr> <td>Total memory bits</td> <td>0 / 1,152,000 (0 %)</td> </tr> <tr> <td>Embedded Multiplier 9-bit elements</td> <td>0 / 300 (0 %)</td> </tr> <tr> <td>Total PLLs</td> <td>0 / 4 (0 %)</td> </tr> </tbody> </table>						Flow Summary		Flow Status	Successful - Tue Jun 01 10:52:52 2021	Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition	Revision Name	MFE	Top-level Entity Name	MFE	Family	Cyclone II	Device	EP2C70F896C8	Timing Models	Final	Total logic elements	490 / 68,416 (< 1 %)	Total combinational functions	461 / 68,416 (< 1 %)	Dedicated logic registers	197 / 68,416 (< 1 %)	Total registers	197	Total pins	57 / 622 (9 %)	Total virtual pins	0	Total memory bits	0 / 1,152,000 (0 %)	Embedded Multiplier 9-bit elements	0 / 300 (0 %)	Total PLLs	0 / 4 (0 %)
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Description of your design																																							

我用 FSM 分成了六個階段

1.reset:主要將一些 register 做歸零的動作

我這邊宣告了 9 個 register 兩組，第一組是拿來在 read 階段做儲存，第二組是在 sort 階段做排序

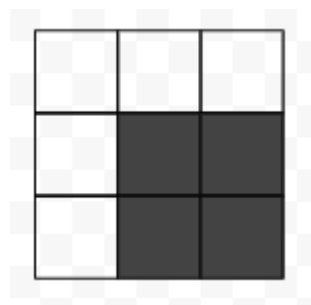
2.wait:當 ready 訊號拉起來會進這個階段空轉一個 cycle，原因是我發現跑 postsim 時，testbench 會等到 ready 降下來後才給值



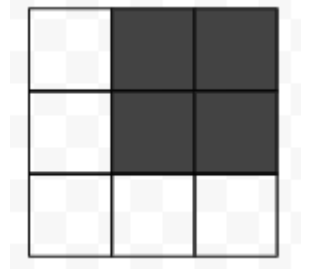
所以我會讓我的程式空轉一個 cycle 再進入 read 階段

3.read:這個階段我分成 7 種不同情況，將 read 的值存入第一組 register 對應的

(1)左上角(addr = 0) 讀四次

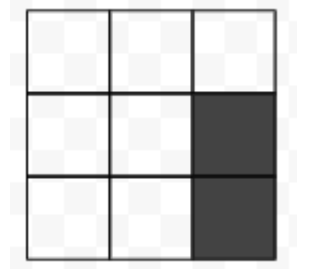


(2)左下角(addr = 16256) 讀四次



(3)last column(addr[6:0]=7h'7f) 讀 0 次

(4)first row(addr < 127) 讀 2 次



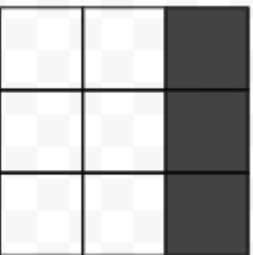
(5)last row(addr > 16256) 讀 2 次



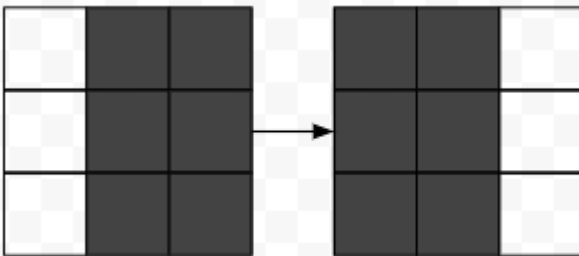
(6)first column(addr[6:0]=7h'0) 讀 6 次



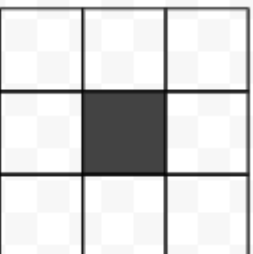
(7)other 讀 3 次



4.sort:這個階段第一個 cycle 會將第一組 register 儲存的值送給第二組 register，並且將第一組的值往右移一格，然後花 9 個 cycle 做 bubble sort



5.write:輸出第二組的中位數



6.finish:結束

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (longest gate-level simulation time in ns)*