PARALLEL (AND BIG DATA) ALGORITHMS

Parallel Random Access Machines (PRAM)

- In the PRAM model, we consider p number of RAM processors, each with its **own local registers**, which all have access to a **global memory**.
- Time is divided into **synchronous** steps and in each step, each processor can do a RAM operation or it can **read/write to one global memory location**.
- The model has four variations with regard to how concurrent reads and writes to one global memory are resolved:

1. Exclusive Read Exclusive Write (EREW)
2. Concurrent Read Exclusive Write (CREW)
3. Exclusive Read Concurrent Write (ERCW)
4. Concurrent Read Concurrent Write (CRCW)

When concurrent writes on the same memory location are allowed, there are variations on how the output is determined. A simple rule is to assume that an arbitrarily chosen one of the write operations takes effect.

Similar to NC, we use variants with index k- e.g. CRCW(k) - to denote decision problems that can be computed by the corresponding version of the PRAM model with **poly(n) processors** and in **O(log^k n)** time steps.

Q) Maximum, using Fewer Processors
The maximum of n entries can be computed in **O(log log n)** time-steps, using the **CRCW** version of PRAM with n processors.

- Computing the maximum of n numbers can be done in **O(log n)** time by any of the variants (and in particular, in the weakest of them, **EREW**), using a **simple binary tree**.
- And it is also known that computing this maximum requires **Ω(log n) time-steps** in the **EREW** version.
- However, this can be done in **O(1) time-steps** in the **CRCW** model, using **O(n^2)** processors, as follows:
- Initialize n entries in the register to be all 0.
- Use n^2 processors, one responsible to compare one pair of numbers.
- If the ith item loses the comparison (i.e., is less than some jth one), write 1 in the ith entry of the register.
- Then, make n processors check the n register entries and if an entry is still 0, which means it did not lose a comparison, write its value in the output register.

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