Vemulapalli Sri Samadarsini

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SUMMARY

Graduate student in Computer Engineering with strong foundations in RTL design, functional verification, and FPGA prototyping, combined with practical experience in hardware-software co-design. Skilled in Verilog, SystemVerilog, and UVM for IP and SoC level verification, with working knowledge of DFT techniques including scan insertion and ATPG. Experienced across the digital design flow from RTL coding to synthesis, timing closure, and physical implementation using industry standard tools such as Synopsys DC, ICC2, Cadence Innovus, and ModelSim. Brings a detail-oriented approach to building reliable, efficient digital systems.

EDUCATION

- **University of Maryland Baltimore County** Maryland, USA
  Master of Science in Computer Engineering; GPA: 3.47 *Aug 2023 - May 2025*
  - **Related Coursework:** Custom VLSI Design, Topics in VLSI, Reconfigurable System Design, VLSI Design Verification and Testing, Computer Arithmetic and Algorithms, Advanced Computer Architecture, Natural Language Processing
- **Gayatri Vidya Parishad College of Engineering** Vishakapatnam, India
  Bachelor of Technology in Electronics and Communication Engineering; GPA: 3.8 (9.31/10.00) *Sept 2019 - April 2023*

WORK EXPERIENCE

- **Graduate Research Assistant - VLSI SOC Lab** Maryland, USA
  VLSI SOC Lab, University of Maryland Baltimore County *Jan 2025 - Present*
  - Developed a 22-layer convolutional autoencoder using hardware-software co-design on Intel DE1-SoC FPGA. Implemented custom Verilog PEs for 3×3 MAC operations with parallel computation via memory-mapped I/O. Achieved 87.58% reconstruction accuracy using INT8 quantization, with efficient pipeline control in embedded C.
- **Internship - RTL Design Engineer Intern** India
  Maven Silicon *April 2023 - Aug 2023*
  - Designed and verified a RISC-V 32I processor core, implementing RTL in Verilog and validating functionality using UVM in Synopsys VCS. Focused on pipeline architecture and instruction execution accuracy, simulating end-to-end behavior and debugging corner cases to ensure design robustness.

PROJECTS

- **Direct Mapped Cache Design**: (VHDL, Cadence Virtuoso)
  - Designed, implemented, and simulated a direct-mapped cache block in VHDL, featuring byte addressability, write-through with no write allocate, and specified read/write timing.
  - Developed a detailed layout for the cache in cadence virtuoso with 45nm technology, specifications including 4-byte blocks, 6-bit addresses, 2-bit tags, and read/write operations (2 clocks for read hit, 3 clocks for write hit/miss, and 19 clocks for read miss). The implemented design has an area of 242.16 μm^2.
- **Comparison of Test Generation Schemes for Sequential Circuits**: (Verilog, TCL, Python, TetraMAX)
  - Conducted a comparative analysis of random and deterministic test pattern generation schemes for sequential circuits using Synopsys TetraMAX.
  - Implemented and compared single and multiple scan chains, and partial scan insertion, to optimize test pattern generation and fault detection efficiency. Observed that the Full scan chain and Multiple scan chain gives the best results in ATPG.
- **Matrix Convolution Hardware Accelerator**: (System Verilog, C, Intel Quartus Prime, FPGA SOC board)
  - Developed a matrix convolution hardware accelerator using Finite State Machine and Avalon-MM interface, integrating FPGA-based processing for efficient computation.
  - Validated the design through hardware-software co-design, and analyzed the effect of acceleration on a part of algorithm using the FPGA De1-SOC board.
- **Verilog_Coder: Verilog Code Generation using LLM and Evaluation using DC and ICC2 tools**: (Python, Verilog, TCL, Synopsys DC, Synopsys ICC2)
  - Developed a Verilog Coder using LLM to automate RTL code generation from natural language descriptions and evaluated it using Synopsys DC and ICC2 tools.
  - The average demonstrated area is reduced by 26.96% and power is improved by 10.41% for the verilog_coder after place and route. Verified 75% of the generated Verilog codes as functionally correct using Synopsys VCS.
- **Design and Verification of RISC-V processor**: (Verilog, System Verilog, Synopsys VCS)
  - Designed a 5-stage pipelined RISC-V processor core using Verilog, implementing instruction fetch, decode, execute, memory access, and write-back stages.
  - Verified functionality using SystemVerilog testbenches and UVM, testing for pipeline hazards, control signals, and instruction execution, ensuring correct operation across various scenarios.

SKILLS

- **Programming and Scripting languages:** Python, C, TCL, Bash
- **Digital Design & Verification:** Verilog, SystemVerilog, VHDL, RTL Design, UVM, SoC Architecture, Functional Verification, DFT, ATPG, BIST
- **EDA & Hardware Tools:** Synopsys Design Compiler, ICC2, VCS, Tetramax, Intel Quartus Prime, ModelSim, Cadence Xcelium, Virtuoso, Innovus, Xilinx Vivado, Matlab
- **Technical Skills:** FPGA Acceleration, Hardware-Software Co-design, Pipelining, Physical Design, STA, Power Optimization, Timing Closure, High-Speed Interfaces (DDR, UART, SPI, I2C)
- **Operating Systems:** Microsoft Windows, Linux