Computer Architectures
Exam of 12.2.2025 - part I

First name, Last name, ID.....

A - Question #2, Text

Consider a processor connected to 128 KB of memory and equipped with a set-associative cache consisting of 8 sets of 4 lines each, for a total of 32 different lines, each of 32 bytes. Assuming that:

- The cache is initially not empty, and its configuration is reported in the Cache table.
- The adopted replacing algorithm is the Least Recently Used (LRU). In the Cache table, blocks are marked with an ascending label indicating when they were inserted or accessed. Specifically, the most recently used block is marked with 0, while the least recently used block is marked with 3.

Given the sequence of memory accesses shown in the Accesses table, determine the corresponding set and line being accessed. Use the Cache table to help you calculate the line involved in each operation. This way, you will get the final cache status. Finish by providing the total number of hits and misses that occurred.

Accesses

Block	Block (Binary)	Accessed Set	Accessed Line	H/M
4056	1111 1101 1000			
2246	1000 1100 0110			
2698	1010 1000 1010			
458	0001 1100 1010			
582	0010 0100 0110			
677	0010 1010 0101			
1475	0101 1100 0011			
3093	1100 0001 0101			
1359	0101 0100 1111			
3	0000 0000 0011			
4007	1111 1010 0111			
1876	0111 0101 0100			
350	0001 0101 1110			
818	0011 0011 0010			
953	0011 1011 1001			
4056	1111 1101 1000			
1492	0101 1101 0100			
1111	0100 0101 0111			
3385	1101 0011 1001			
1475	0101 1100 0011			

Cache

	Set 0			Set 2			Set 4			Set 6	
Line 0	3520	2	***Line 8***	2698	1	***Line 16***	380	3	***Line 24***	2398	1
Line 1	1000	0	***Line 9***	3594	3	***Line 17***	1492	1	***Line 25***	854	3
Line 2	2784	3	***Line 10***	4050	2	***Line 18***	3924	2	***Line 26***	2246	0
Line 3	1368	1	***Line 11***	458	0	***Line 19***	388	0	***Line 27***	582	2

	Set 1			Set 3			Set 5			Set 7	
Line 4	769	0	***Line 12***	3	3	***Line 20***	45	2	***Line 28***	4007	1
Line 5	345	2	***Line 13***	3923	1	***Line 21***	3877	3	***Line 29***	1359	0
Line 6	2569	1	***Line 14***	1475	0	***Line 22***	117	1	***Line 30***	879	2
Line 7	1297	3	***Line 15***	3675	2	***Line 23***	3093	0	***Line 31***	3703	3

Number of hits: ____ Number of misses: ____

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A - Question #2, Solution 1

Consider a processor connected to 128 KB of memory and equipped with a set-associative cache consisting of 8 sets of 4 lines each, for a total of 32 different lines, each of 32 bytes. Assuming that:

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Accesses

Block	Block (Binary)	Accessed Set	Accessed Line	H/M
4056	1111 1101 **1000**	0	2	**M**
2246	1000 1100 **0110**	6	26	**H**
2698	1010 1000 **1010**	2	8	**H**
458	0001 1100 **1010**	2	11	**H**
582	0010 0100 **0110**	6	27	**H**
677	0010 1010 **0101**	5	21	**M**
1475	0101 1100 **0011**	3	14	**H**
3093	1100 0001 **0101**	5	23	**H**
1359	0101 0100 **1111**	7	29	**H**
3	0000 0000 **0011**	3	12	**H**
4007	1111 1010 **0111**	7	28	**H**
1876	0111 0101 **0100**	4	16	**M**
350	0001 0101 **1110**	6	25	**M**
818	0011 0011 **0010**	2	9	**M**
953	0011 1011 **1001**	1	7	**M**
4056	1111 1101 **1000**	0	2	**H**
1492	0101 1101 **0100**	4	17	**H**
1111	0100 0101 **0111**	7	31	**M**
3385	1101 0011 **1001**	1	5	**M**
1475	0101 1100 **0011**	3	14	**H**

Cache

Set 0		
Line 0	3520	3
Line 1	1000	1
Line 2	4056	0
Line 3	1368	2

Set 1		
Line 4	769	2
Line 5	3385	0
Line 6	2569	3
Line 7	953	1

Set 2		
Line 8	2698	2
Line 9	818	0
Line 10	4050	3
Line 11	458	1

Set 3		
Line 12	3	1
Line 13	3923	2
Line 14	1475	0
Line 15	3675	3

Set 4		
Line 16	1876	1
Line 17	1492	0
Line 18	3924	3
Line 19	388	2

Set 5		
Line 20	45	3
Line 21	677	1
Line 22	117	2
Line 23	3093	0

Set 6		
Line 24	2398	3
Line 25	350	0
Line 26	2246	2
Line 27	582	1

Set 7		
Line 28	4007	1
Line 29	1359	2
Line 30	879	3
Line 31	1111	0

Number of hits: __**12**__ Number of misses: __**8**__

This solution relies on the use of the global line numbers specified in the Cache table, which are always unique for the different sets. Their use is strongly recommended as there is less chance of writing and verification errors.

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A - Question #2, Solution 2

Consider a processor connected to 128 KB of memory and equipped with a set-associative cache consisting of 8 sets of 4 lines each, for a total of 32 different lines, each of 32 bytes. Assuming that:

- The cache is initially not empty, and its configuration is reported in the Cache table.
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Given the sequence of memory accesses shown in the Accesses table, determine the corresponding set and line being accessed. Use the Cache table to help you calculate the line involved in each operation. This way, you will get the final cache status. Finish by providing the total number of hits and misses that occurred.

Accesses

Block	Block (Binary)	Accessed Set	Accessed Line	H/M
4056	1111 1101 **1000**	0	2	**M**
2246	1000 1100 **0110**	6	2	**H**
2698	1010 1000 **1010**	2	0	**H**
458	0001 1100 **1010**	2	3	**H**
582	0010 0100 **0110**	6	3	**H**
677	0010 1010 **0101**	5	1	**M**
1475	0101 1100 **0011**	3	2	**H**
3093	1100 0001 **0101**	5	3	**H**
1359	0101 0100 **1111**	7	1	**H**
3	0000 0000 **0011**	3	0	**H**
4007	1111 1010 **0111**	7	0	**H**
1876	0111 0101 **0100**	4	0	**M**
350	0001 0101 **1110**	6	1	**M**
818	0011 0011 **0010**	2	1	**M**
953	0011 1011 **1001**	1	3	**M**
4056	1111 1101 **1000**	0	2	**H**
1492	0101 1101 **0100**	4	1	**H**
1111	0100 0101 **0111**	7	3	**M**
3385	1101 0011 **1001**	1	1	**M**
1475	0101 1100 **0011**	3	2	**H**

Cache

Set 0		
Line 0	3520	3
Line 1	1000	1
Line 2	4056	0
Line 3	1368	2

Set 1		
Line 4	769	2
Line 5	3385	0
Line 6	2569	3
Line 7	953	1

Set 2		
Line 8	2698	2
Line 9	818	0
Line 10	4050	3
Line 11	458	1

Set 3		
Line 12	3	1
Line 13	3923	2
Line 14	1475	0
Line 15	3675	3

Set 4		
Line 16	1876	1
Line 17	1492	0
Line 18	3924	3
Line 19	388	2

Set 5		
Line 20	45	3
Line 21	677	1
Line 22	117	2
Line 23	3093	0

Set 6		
Line 24	2398	3
Line 25	350	0
Line 26	2246	2
Line 27	582	1

Set 7		
Line 28	4007	1
Line 29	1359	2
Line 30	879	3
Line 31	1111	0

Number of hits: __**12**__ Number of misses: __**8**__

This solution relies on the use of local line numbers, which are not unique for the different sets. Their use is strongly discouraged as there is a greater possibility of writing and verification errors.

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B - Question #2, Text

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Accesses

Block	Block (Binary)	Accessed Set	Accessed Line	H/M
2633	1010 0100 1001			
345	0001 0101 1001			
1750	0110 1101 0110			
3675	1110 0101 1011			
677	0010 1010 0101			
995	0011 1110 0011			
854	0011 0101 0110			
4056	1111 1101 1000			
1860	0111 0100 0100			
117	0000 0111 0101			
818	0011 0011 0010			
3520	1101 1100 0000			
388	0001 1000 0100			
3093	1100 0001 0101			
167	0000 1010 0111			
1475	0101 1100 0011			
1359	0101 0100 1111			
1750	0110 1101 0110			
3594	1110 0000 1010			
808	0011 0010 1000			

Cache

	Set 0		Set 2		Set 4		Set 6	
Line 0	0	3	2698	0	388	2	774	1
Line 1	3520	1	154	2	3172	0	2566	3
Line 2	4056	0	818	1	1492	3	350	2
Line 3	2000	2	3506	3	1444	1	1750	0

	Set 1		Set 3		Set 5		Set 7	
Line 4	257	3	995	1	117	0	3239	2
Line 5	345	1	2915	3	677	2	167	0
Line 6	3385	2	1475	0	3765	1	1111	3
Line 7	2777	0	579	2	3493	3	4007	1

Number of hits: ____ Number of misses: ____

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B - Question #2, Solution 1

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Accesses

Block	Block (Binary)	Accessed Set	Accessed Line	H/M
2633	1010 0100 1**001**	1	4	**M**
345	0001 0101 1**001**	1	5	**H**
1750	0110 1101 0**110**	6	27	**H**
3675	1110 0101 1**011**	3	13	**M**
677	0010 1010 0**101**	5	21	**H**
995	0011 1110 0**011**	3	12	**H**
854	0011 0101 0**110**	6	25	**M**
4056	1111 1101 1**000**	0	2	**H**
1860	0111 0100 0**100**	4	18	**M**
117	0000 0111 0**101**	5	20	**H**
818	0011 0011 0**010**	2	10	**H**
3520	1101 1100 0**000**	0	1	**H**
388	0001 1000 0**100**	4	16	**H**
3093	1100 0001 0**101**	5	23	**M**
167	0000 1010 0**111**	7	29	**H**
1475	0101 1100 0**011**	3	14	**H**
1359	0101 0100 1**111**	7	30	**M**
1750	0110 1101 0**110**	6	27	**H**
3594	1110 0000 1**010**	2	11	**M**
808	1000 0000 1**000**	0	0	**M**

Cache

	Set 0			Set 2			Set 4			Set 6	
Line 0	808	0	***Line 8***	2698	2	***Line 16***	388	0	***Line 24***	774	2
Line 1	3520	1	***Line 9***	154	3	***Line 17***	3172	2	***Line 25***	854	1
Line 2	4056	2	***Line 10***	818	1	***Line 18***	1860	1	***Line 26***	350	3
Line 3	2000	3	***Line 11***	3594	0	***Line 19***	1444	3	***Line 27***	1750	0

	Set 1			Set 3			Set 5			Set 7	
Line 4	2633	1	***Line 12***	995	1	***Line 20***	117	1	***Line 28***	3239	3
Line 5	345	0	***Line 13***	3675	2	***Line 21***	677	2	***Line 29***	167	1
Line 6	3385	3	***Line 14***	1475	0	***Line 22***	3765	3	***Line 30***	1359	0
Line 7	2777	2	***Line 15***	579	3	***Line 23***	3093	0	***Line 31***	4007	2

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Accesses

Block	Block (Binary)	Accessed Set	Accessed Line	H/M
2633	1010 0100 1**001**	1	0	**M**
345	0001 0101 1**001**	1	1	**H**
1750	0110 1101 0**110**	6	3	**H**
3675	1110 0101 1**011**	3	1	**M**
677	0010 1010 0**101**	5	1	**H**
995	0011 1110 0**011**	3	0	**H**
854	0011 0101 0**110**	6	1	**M**
4056	1111 1101 1**000**	0	2	**H**
1860	0111 0100 0**100**	4	2	**M**
117	0000 0111 0**101**	5	0	**H**
818	0011 0011 0**010**	2	2	**H**
3520	1101 1100 0**000**	0	1	**H**
388	0001 1000 0**100**	4	0	**H**
3093	1100 0001 0**101**	5	3	**M**
167	0000 1010 0**111**	7	1	**H**
1475	0101 1100 0**011**	3	2	**H**
1359	0101 0100 1**111**	7	2	**M**
1750	0110 1101 0**110**	6	3	**H**
3594	1110 0000 1**010**	2	3	**M**
808	1000 0000 1**000**	0	0	**M**

Cache

Set 0

Line 0	808	0
Line 1	3520	1
Line 2	4056	2
Line 3	2000	3

Set 1

Line 4	2633	1
Line 5	345	0
Line 6	3385	3
Line 7	2777	2

Set 2

Line 8	2698	2
Line 9	154	3
Line 10	818	1
Line 11	3594	0

Set 3

Line 12	995	1
Line 13	3675	2
Line 14	1475	0
Line 15	579	3

Set 4

Line 16	388	0
Line 17	3172	2
Line 18	1860	1
Line 19	1444	3

Set 5

Line 20	117	1
Line 21	677	2
Line 22	3765	3
Line 23	3093	0

Set 6

Line 24	774	2
Line 25	854	1
Line 26	350	3
Line 27	1750	0

Set 7

Line 28	3239	3
Line 29	167	1
Line 30	1359	0
Line 31	4007	2

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