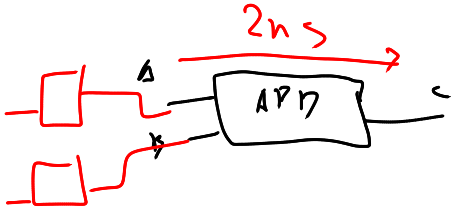
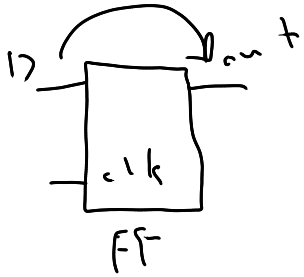
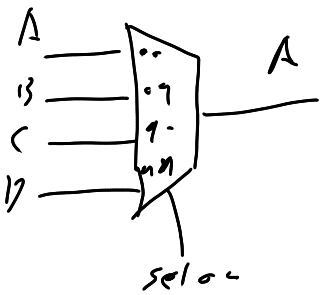
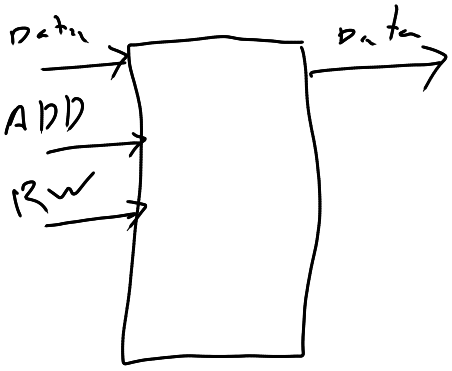




FF

MUX





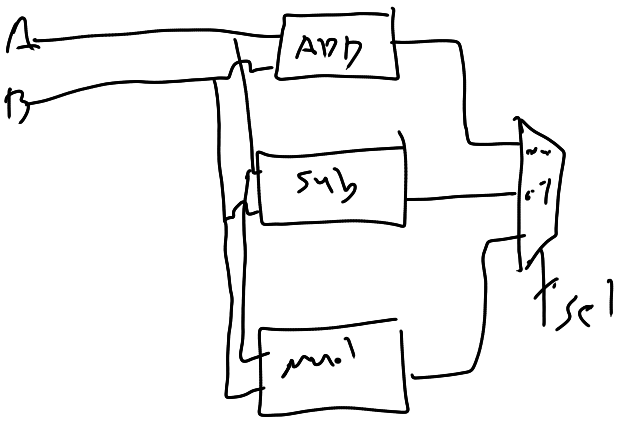
1 byte

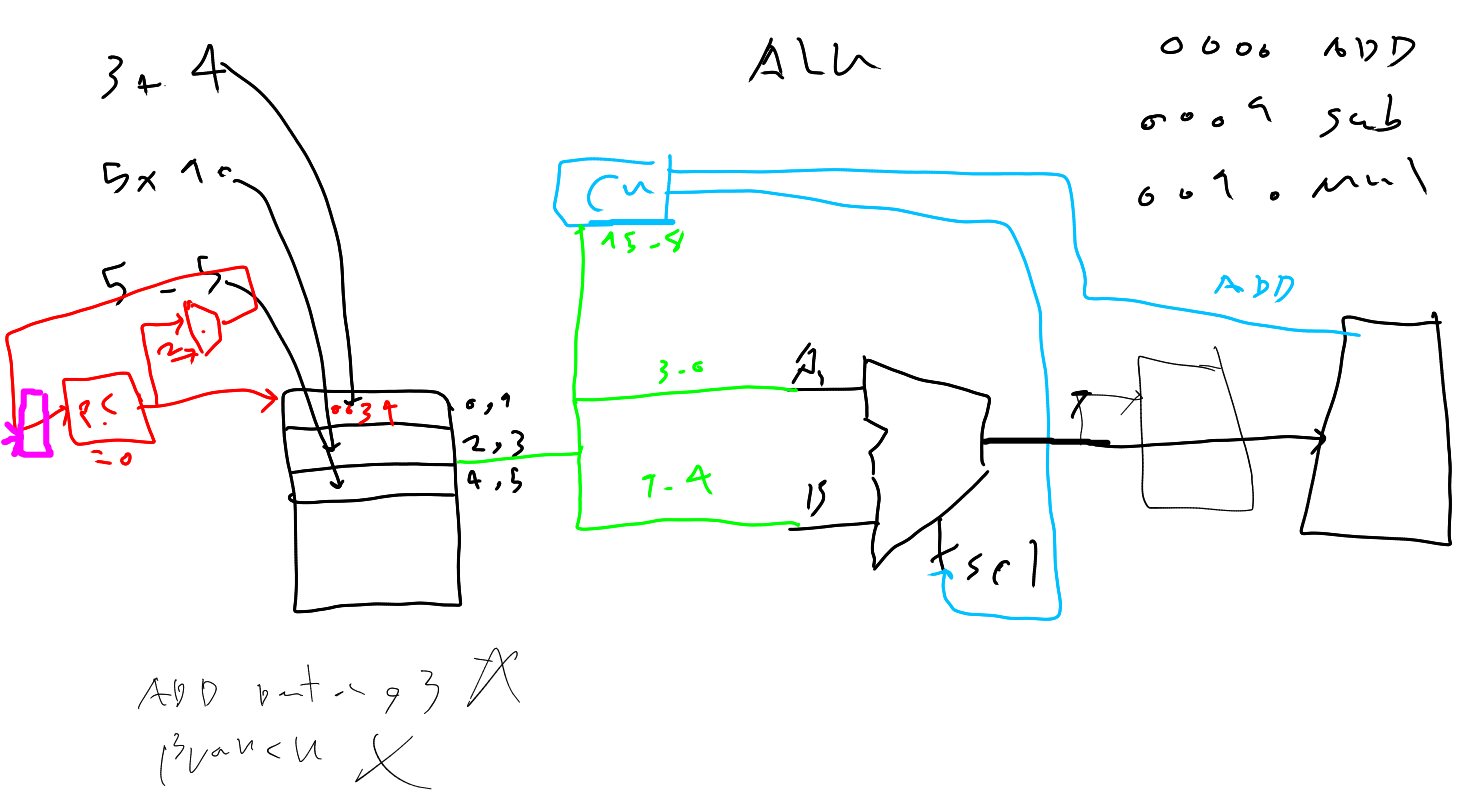
Add = 0

RW = 0

RW = 1

ALU





ADD 명령어 X

Branch X

1byte ⇒ 2byte ⇒ 16bit → 4bit 4bit 4bit 4bit

X opcode Data1 Data2

.... 0000 0011 0100

compiler 0x34

Assembler

ADD 3,4 → 0x34

mul 5,10

ADD R_1, R_2, #20 (imm) $R_1 \leftarrow R_2 + 20$

ADD R_1, R_2, R_3 $R_1 \leftarrow R_2 + R_3$

J test

Cache

RAM.

HDD

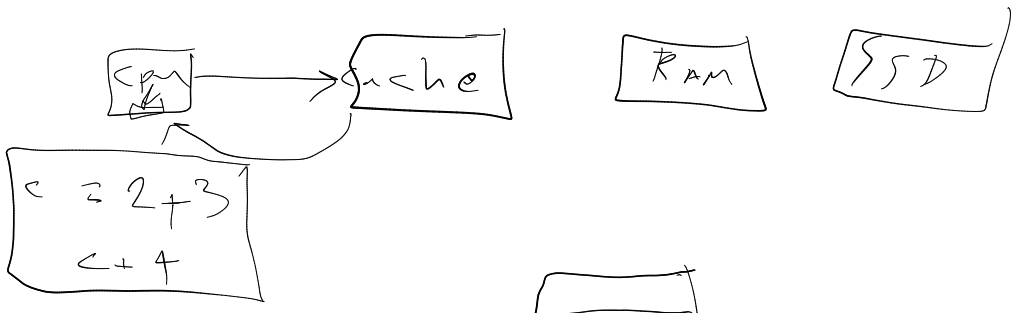
SSD

GHz

Cpu

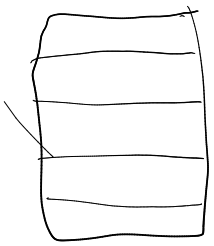
MHz

mem



Register

Register file



32

64

$log_2^{32} = 5$

6

ADD R1, R2, R3

ADDI R4, R5, Imm +16 bit

J label 26

Bnez R10, label 31-25

LD R1, R6(32)

R1 ← mem[R6+32]

SD R1, R6(32)

R1 → Mem[R6+32]

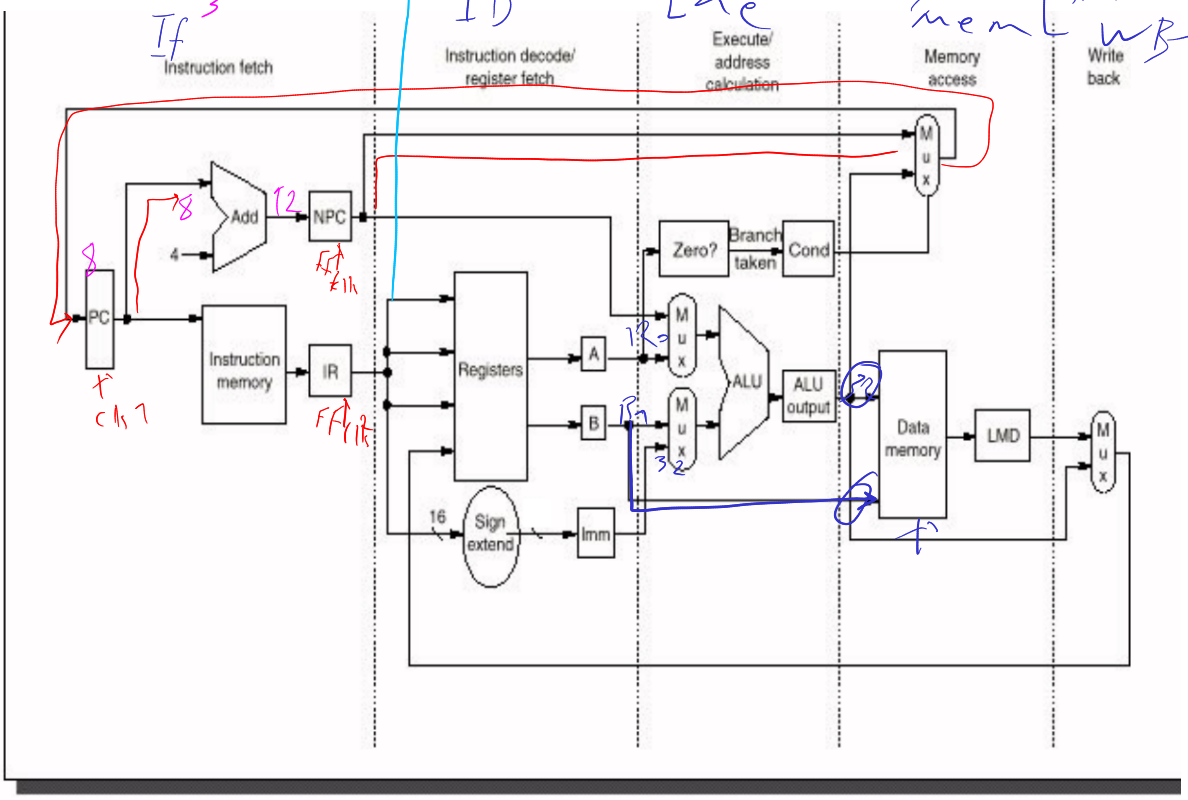
mem WB

PC

IF 3

ID

EX



$R_4 \leftarrow 1$

$R_3 \leftarrow 1$

$R_2 \leftarrow 8$

$R_1 \leftarrow 8$

$R_4 \leftarrow 2$

$R_3 \leftarrow 3$

$R_2 \leftarrow 96$

$R_1 \leftarrow 8$

$R_4 \leftarrow 3$

$R_3 \leftarrow 6$

$R_2 \leftarrow 24$

$R_4 \leftarrow 7$

$k_1 = 6$