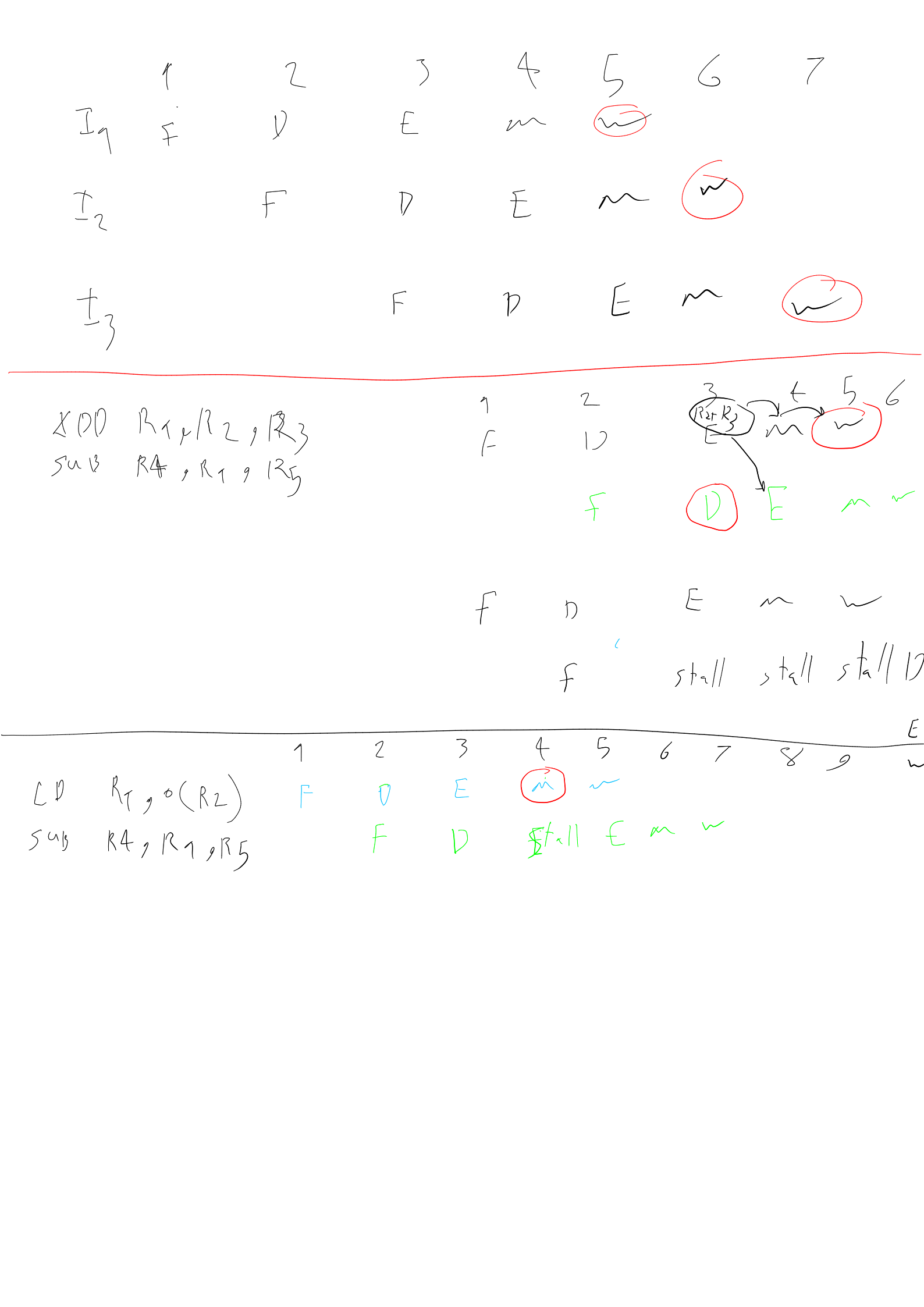
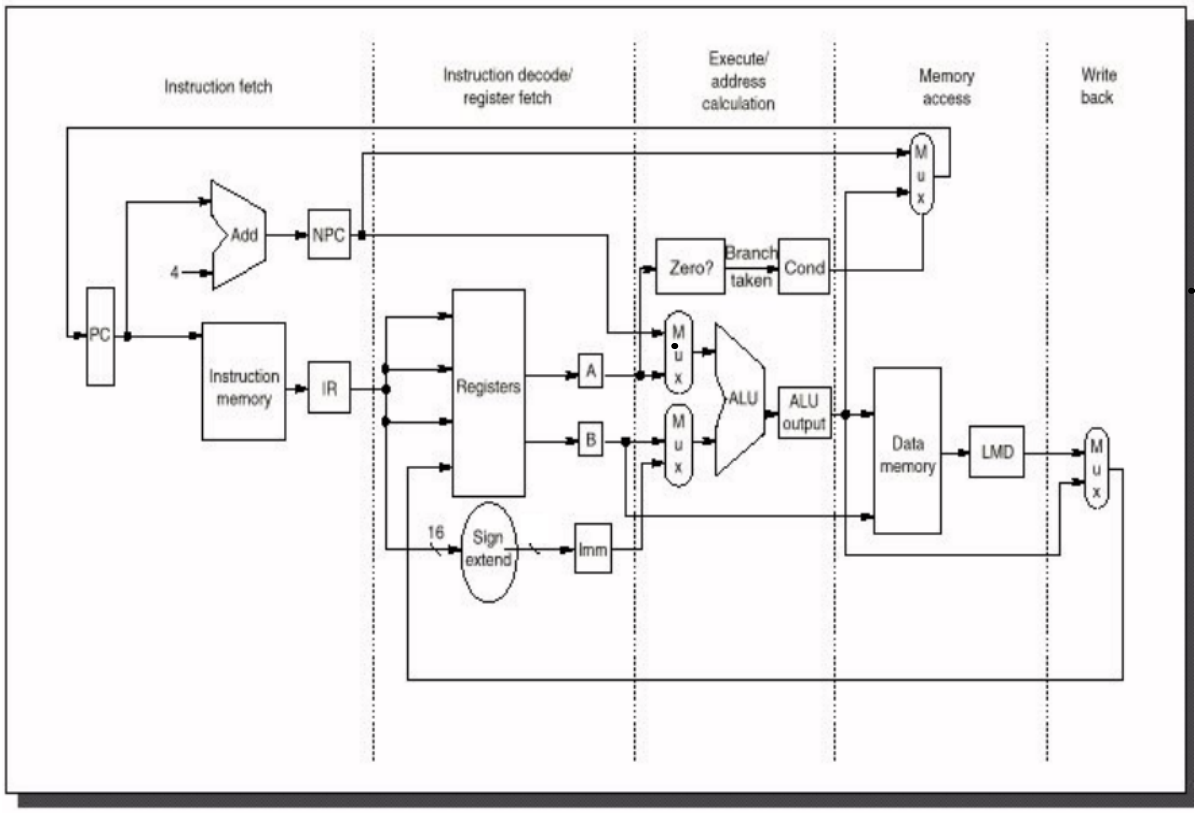
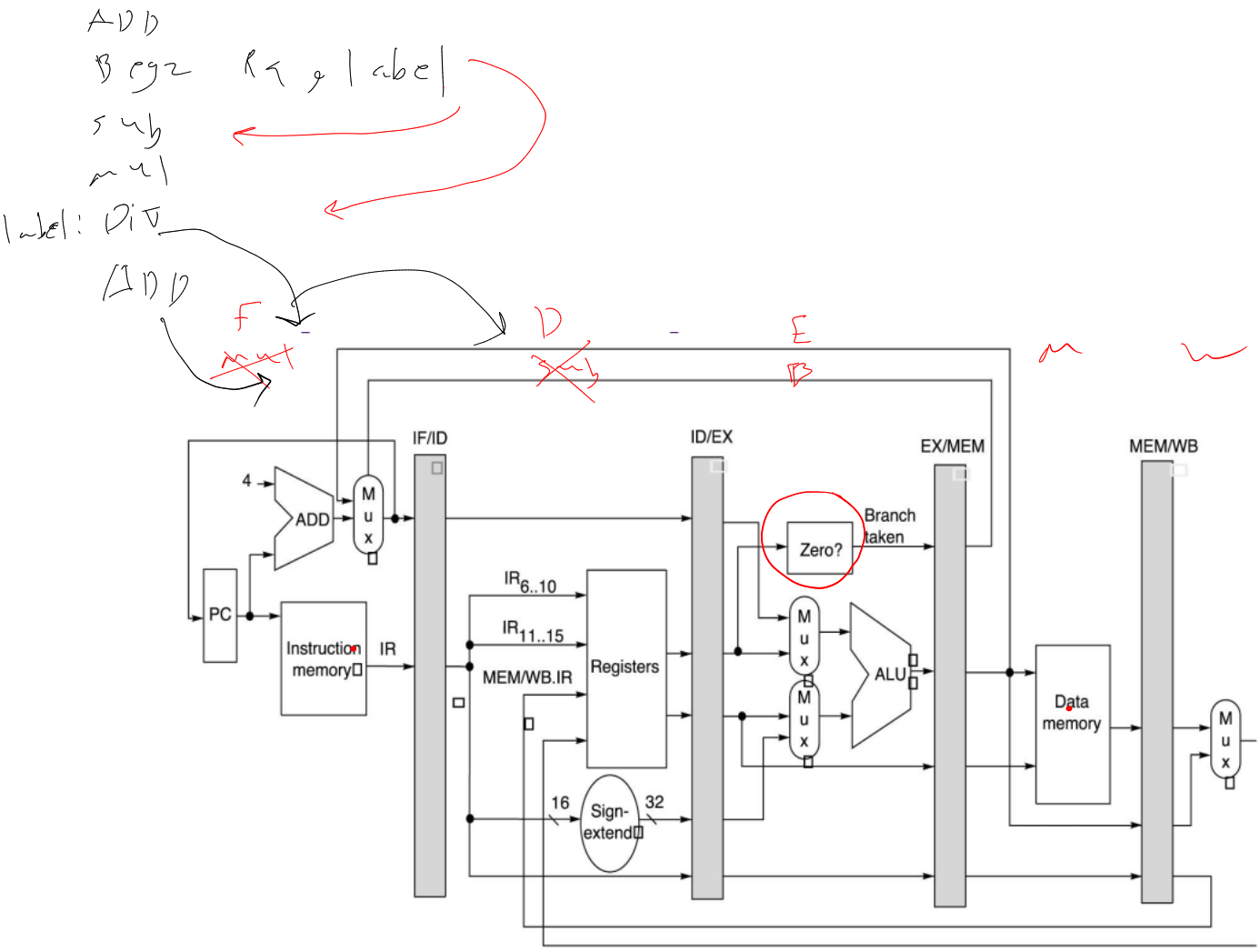


ADD R1, R2, R3
SUB R4, R1, R5

LD R1, 0(R2)
SUB R4, R1, R5


Instruction fetch
Instruction decode/ register fetch
Execute/ address calculation
Memory access
Write back
Add
4
NPC
PC
Instruction memory
IR
Registers
A
B
16
Sign extend
Imm
Zero?
Branch taken
Cond
M u x
ALU
ALU output
Data memory
LMD


IF/ID
ID/EX
EX/MEM
MEM/WB
4
ADD
PC
Instruction memory
IR
IR6..10
IR11..15
MEM/WB.IR
Registers
16
Sign-extend
32
Zero?
Branch taken
ALU
Data memory

Pipeline

Hazard
- structural → HW
- Data → { forward / stall } → load
- Control → branch { stall