Computer Architectures
Exam of 29.1.2025 - part I

First name, Last name, ID.....

A - Question #2

Let's consider a MIPS architecture using a Branch History Table (BHT) composed of 16 1-bit entries. It orderly executes the instructions reported in the table below, which also indicates the hex address of the corresponding memory cell. You are asked to describe the evolution of the content of the BHT during the execution of such instructions assuming that, before executing them, the BHT is filled with null values (corresponding to the Not Taken, NT, prediction). Write in the correct cells whether the prediction (PRED) of the current branch and the outcome (RES) is Taken (T) or Not Taken (NT).

ADDR	Code	Address in Binary	Entry #	PRED	RES
0x0058	daddui r30, r30, 1				
0x005c	beq r30, r29, trm	*0000 0000 0000 0000 0000 0000 0***1101** *1100*	7	NT	NT
0x0060	daddui r22, r22, 8				
0x0064	lb r10, vec(r22)				
0x0068	dsrl r10, r10, 2				
0x006c	bne r10, r19, ts1	*0000 0000 0000 0000 0000 0000 0***1101** *1100*	11	NT	T
0x0078	bne r10, r16, ts2	*0000 0000 0000 0000 0000 0000 0***1110***000*	14	NT	T
0x0084	bne r10, r12, cyc	*0000 0000 0000 0000 0000 0000 1***0001***00*	1	NT	NT
0x0088	daddui r25, r25, 1				
0x008c	j cyc				
0x0058	daddui r30, r30, 1				
0x005c	beq r30, r29, trm	*0000 0000 0000 0000 0000 0000 0***1101** *1100*	7	NT	NT
0x0060	daddui r22, r22, 8				
0x0064	lb r10, vec(r22)				
0x0068	dsrl r10, r10, 2				
0x006c	bne r10, r19, ts1	*0000 0000 0000 0000 0000 0000 0***1101** *1100*	11	T	T
0x0078	bne r10, r16, ts2	*0000 0000 0000 0000 0000 0000 0***1110***000*	14	T	NT
0x007c	daddui r21, r21, 1				
0x0080	j cyc				
0x0058	daddui r30, r30, 1				
0x005c	beq r30, r29, trm	*0000 0000 0000 0000 0000 0000 0***1101** *1100*	7	NT	NT
0x0060	daddui r22, r22, 8				
0x0064	lb r10, vec(r22)				
0x0068	dsrl r10, r10, 2				
0x006c	bne r10, r19, ts1	*0000 0000 0000 0000 0000 0000 0***1101** *1100*	11	T	NT
0x0070	daddui r28, r28, 1				
0x0074	j cyc				
0x0058	daddui r30, r30, 1				
0x005c	beq r30, r29, trm	*0000 0000 0000 0000 0000 0000 0***1101** *1100*	7	NT	T
0x0090	halt				

a) Based on the results obtained, indicate the total number of correct and incorrect predictions and fill in the BHT content at the end of the run.

Correctly predicted branches: ___**5**___ Mispredicted branches: ___**5**___

BHT - Final content

Entry 0	0	Entry 4	0	Entry 8	0	Entry 12	0
Entry 1	0	Entry 5	0	Entry 9	0	Entry 13	0
Entry 2	0	Entry 6	0	Entry 10	0	Entry 14	0
Entry 3	0	Entry 7	1	Entry 11	0	Entry 15	0

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b) Next, reconstruct the program structure by examining the sequence of instructions.

Code:

```
daddui r30, r30, 1
beq r30, r29, trm
daddui r22, r22, 8
lb r10, vec(r22)
dsrl r10, r10, 2
bne r10, r19, ts1
daddui r28, r28, 1
j cyc
bne r10, r16, ts2
daddui r21, r21, 1
j cyc
bne r10, r12, cyc
daddui r25, r25, 1
j cyc
halt
```

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B - Question #2

Let's consider a MIPS architecture using a Branch History Table (BHT) composed of 16 1-bit entries. It orderly executes the instructions reported in the table below, which also indicates the hex address of the corresponding memory cell. You are asked to describe the evolution of the content of the BHT during the execution of such instructions assuming that, before executing them, the BHT is filled with null values (corresponding to the Not Taken, NT, prediction). Write in the highlighted cells whether the prediction (PRED) of the current branch and the outcome (RES) is Taken (T) or Not Taken (NT).

ADDR	Code	Address in Binary	Entry #	PRED	RES
0x002c	daddui r18, r18, 1				
0x0030	beq r18, r16, trm	*0000 0000 0000 0000 0000 0000 00**11 00**00*	12	NT	NT
0x0034	daddui r20, r20, 1				
0x0038	lb r4, vec(r20)				
0x003c	dsrl r4, r4, 2				
0x0040	bne r4, r23, ts1	*0000 0000 0000 0000 0000 0000 01**00 00**00*	0	NT	NT
0x0044	daddui r14, r14, 1				
0x0048	j cyc				
0x002c	daddui r18, r18, 1				
0x0030	beq r18, r16, trm	*0000 0000 0000 0000 0000 0000 00**11 00**00*	12	NT	NT
0x0034	daddui r20, r20, 1				
0x0038	lb r4, vec(r20)				
0x003c	dsrl r4, r4, 2				
0x0040	bne r4, r23, ts1	*0000 0000 0000 0000 0000 0000 01**00 00**00*	0	NT	T
0x004c	bne r4, r9, ts2	*0000 0000 0000 0000 0000 0000 01**00 11**00*	3	NT	T
0x0058	bne r4, r8, cyc	*0000 0000 0000 0000 0000 0000 01**01 10**00*	6	NT	NT
0x005c	daddui r2, r2, 1				
0x0060	j cyc				
0x002c	daddui r18, r18, 1				
0x0030	beq r18, r16, trm	*0000 0000 0000 0000 0000 0000 00**11 00**00*	12	NT	NT
0x0034	daddui r20, r20, 1				
0x0038	lb r4, vec(r20)				
0x003c	dsrl r4, r4, 2				
0x0040	bne r4, r23, ts1	*0000 0000 0000 0000 0000 0000 01**00 00**00*	0	T	T
0x004c	bne r4, r9, ts2	*0000 0000 0000 0000 0000 0000 01**00 11**00*	3	T	NT
0x0050	daddui r21, r21, 1				
0x0054	j cyc				
0x002c	daddui r18, r18, 1				
0x0030	beq r18, r16, trm	*0000 0000 0000 0000 0000 0000 00**11 00**00*	12	NT	T
0x0064	halt				

a) Based on the results obtained, indicate the total number of correct and incorrect predictions and fill in the BHT content at the end of the run.

Correctly predicted branches: ___6___ Mispredicted branches: ___4___

BHT - Final content

Entry 0	1	Entry 4	0	Entry 8	0	Entry 12	1
Entry 1	0	Entry 5	0	Entry 9	0	Entry 13	0
Entry 2	0	Entry 6	0	Entry 10	0	Entry 14	0
Entry 3	0	Entry 7	0	Entry 11	0	Entry 15	0

First name, Last name, ID.....

b) Next, reconstruct the program structure by examining the sequence of instructions.

Code:

```
daddui r18, r18, 1
beq r18, r16, trm
daddui r20, r20, 1
lb r4, vec(r20)
dsrl r4, r4, 2
bne r4, r23, ts1
daddui r14, r14, 1
j cyc
bne r4, r9, ts2
daddui r21, r21, 1
j cyc
bne r4, r8, cyc
daddui r2, r2, 1
j cyc
halt
```

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C - Question #2

Let's consider a MIPS architecture using a Branch History Table (BHT) composed of 16 1-bit entries. It orderly executes the instructions reported in the table below, which also indicates the hex address of the corresponding memory cell. You are asked to describe the evolution of the content of the BHT during the execution of such instructions assuming that, before executing them, the BHT is filled with null values (corresponding to the Not Taken, NT, prediction). Write in the highlighted cells whether the prediction (PRED) of the current branch and the outcome (RES) is Taken (T) or Not Taken (NT).

ADDR	Code	Address in Binary	Entry #	PRED	RES
0x0044	daddui r31, r31, 1				
0x0048	beq r31, r18, trm	*0000 0000 0000 0000 0000 0000 0100 1000*	2	NT	NT
0x004c	daddui r17, r17, 1				
0x0050	lb r7, vec(r17)				
0x0054	dsrl r7, r7, 1				
0x0058	bne r7, r27, ts1	*0000 0000 0000 0000 0000 0000 0101 1000*	6	NT	T
0x0064	bne r7, r5, ts2	*0000 0000 0000 0000 0000 0000 0110 0100*	9	NT	NT
0x0068	daddui r13, r13, 1				
0x006c	j cyc				
0x0044	daddui r31, r31, 1				
0x0048	beq r31, r18, trm	*0000 0000 0000 0000 0000 0000 0100 1000*	2	NT	NT
0x004c	daddui r17, r17, 1				
0x0050	lb r7, vec(r17)				
0x0054	dsrl r7, r7, 1				
0x0058	bne r7, r27, ts1	*0000 0000 0000 0000 0000 0000 0101 1000*	6	T	NT
0x005c	daddui r24, r24, 1				
0x0060	j cyc				
0x0044	daddui r31, r31, 1				
0x0048	beq r31, r18, trm	*0000 0000 0000 0000 0000 0000 0100 1000*	2	NT	NT
0x004c	daddui r17, r17, 1				
0x0050	lb r7, vec(r17)				
0x0054	dsrl r7, r7, 1				
0x0058	bne r7, r27, ts1	*0000 0000 0000 0000 0000 0000 0101 1000*	6	NT	T
0x0064	bne r7, r5, ts2	*0000 0000 0000 0000 0000 0000 0110 0100*	9	NT	T
0x0070	bne r10, r12, cyc	*0000 0000 0000 0000 0000 0000 0111 0000*	12	NT	NT
0x0074	daddui r11, r11, 1				
0x0078	j cyc				
0x0044	daddui r31, r31, 1				
0x0048	beq r31, r18, trm	*0000 0000 0000 0000 0000 0000 0100 1000*	2	NT	T
0x007c	halt				

a) Based on the results obtained, indicate the total number of correct and incorrect predictions and fill in the BHT content at the end of the run.

Correctly predicted branches: ___5___ Mispredicted branches: ___5___

BHT - Final content

Entry 0	0	Entry 4	0	Entry 8	0	Entry 12	0
Entry 1	0	Entry 5	0	Entry 9	1	Entry 13	0
Entry 2	1	Entry 6	1	Entry 10	0	Entry 14	0
Entry 3	0	Entry 7	0	Entry 11	0	Entry 15	0

First name, Last name, ID.....

b) Next, reconstruct the program structure by examining the sequence of instructions.

Code:

```
daddui r31, r31, 1
beq r31, r18, trm
daddui r17, r17, 1
lb r7, vec(r17)
dsrl r7, r7, 1
bne r7, r27, ts1
daddui r24, r24, 1
j cyc
bne r7, r5, ts2
daddui r13, r13, 1
j cyc
bne r10, r12, cyc
daddui r11, r11, 1
j cyc
halt
```