## Computer Architectures Exam of 12/02/2025

## **Question 2 (6 points)**

Consider a processor connected to 128 KB of memory and equipped with a set-associative cache consisting of 8 sets of 4 lines each, for a total of 32 different lines, each of 32 bytes. Assuming that:

- The cache is initially not empty, and its configuration is reported in the Cache table.
- The adopted replacing algorithm is the Least Recently Used (LRU). In the Cache table, blocks are marked with an ascending label indicating when they were inserted or accessed. Specifically, the most recently used block is marked with 0, while the least recently used block is marked with 3.

Given the sequence of memory accesses shown in the Accesses table, determine the corresponding set and line being accessed. Use the Cache table to help you calculate the line involved in each operation. This way, you will get the final cache status. Finish by providing the total number of hits and misses that occurred

## Accesses

Accesses											
Block	Block (Binary)	Accessed Set	Accessed Line	H/M							
4056	1111 1101 1000										
2246	1000 1100 0110										
2698	1010 1000 1010										
458	0001 1100 1010										
582	0010 0100 0110										
677	0010 1010 0101										
1475	0101 1100 0011										
3093	1100 0001 0101										
1359	0101 0100 1111										
3	0000 0000 0011										
4007	1111 1010 0111										
1876	0111 0101 0100										
350	0001 0101 1110										
818	0011 0011 0010										
953	0011 1011 1001										
4056	1111 1101 1000										
1492	0101 1101 0100										
1111	0100 0101 0111										
3385	1101 0011 1001										
1475	0101 1100 0011										

## Cache

	Set 0			Set 2			Set 4			Set 6	
Line 0	3520	2	Line 8	2698	1	Line 16	380	3	Line 24	2398	1
Line 1	1000	0	Line 9	3594	3	Line 17	1492	1	Line 25	854	3
Line 2	2784	3	Line 10	4050	2	Line 18	3924	2	Line 26	2246	0
Line 3	1368	1	Line 11	458	0	Line 19	388	0	Line 27	582	2
	Set 1		_	Set 3		_	Set 5			Set 7	
Line 4	<b>Set 1</b> 769	0	Line 12	Set 3	3	Line 20	Set 5 45	2	Line 28	Set 7 4007	1
Line 4 Line 5		0	Line 12 Line 13		3	Line 20 Line 21		3	Line 28 Line 29		1 0
	769	Ť		3	3 1 0		45			4007	1 0 2
Line 5	769 345	Ť	Line 13	3 3923	1	Line 21	45 3877	3	Line 29	4007 1359	
Line 5 Line 6	769 345 2569	2	Line 13 Line 14	3 3923 1475	1 0	Line 21 Line 22	45 3877 117	3	Line 29 Line 30	4007 1359 879	2

Number of hits: \_\_\_\_ Number of misses: \_\_\_\_