## Digital Logic and System Design

## Syllabus for Minor 2

| Chapter | Topics  | Sections   | Relevant     |
|---------|---|------------|--------------|
|         |   | to read    | Exercises    |
| 3       | Transistor circuits   | 3.1 – 3.4  | 3.1 - 3.13,  |
|         | <ul> <li>NMOS/PMOS/CMOS gates, transistor characteristics, voltage levels,</li> </ul> | 3.6 - 3.10 | 3.25 - 3.28, |
|         | noise margins, delays, power, fan-in, fan-out, tri-state buffer,                      |            | 3.36 - 3.55  |
|         | transmission gate   |            |              |
|         | Programmable modules  |            |              |
|         | • Look-up tables, PLAs, PALs, CPLDs, FPGAs, Various programmable                      |            |              |
|         | structures, mask programmable gate arrays, field programming                          |            |              |
|         | techniques, floating gate transistor, SRAM and DRAM cells                             |            |              |
| 5       | Number representation and arithmetic circuits   | 5.1 - 5.6, | all          |
|         | Representing unsigned and signed numbers, radix conversion, BCD                       | 5.7.3, 5.9 |              |
|         | Operations and circuit design for binary addition, subtraction,                       |            |              |
|         | comparison, shift   |            |              |
|         | Overflow detection, addition speed up using carry look ahead                          |            |              |
|         | Array multipliers with carry propagate and carry save adders                          |            |              |
|         | Circuits for sequential multiplication and division                                   |            |              |
| 6       | Multiplexers and LUTs as universal logic modules (ULMs), Shannon's                    | 6.1 - 6.2  | 6.1 - 6.17   |
|         | expansion   |            |              |
| Xilinx  | Configurable logic block in Spartan 6 FPGA, types of slices,                          |            |              |
| Data-   | resources in a slice (look-up tables, flip-flops, multiplexers, fast                  |            |              |
| sheets  | carry chain)  |            |              |
|         | DSP48A1 in Spartan 6 FPGA, using DSP48A1 for weighted sum, pipelining options         |            |              |