COL215 Quiz-2 SetB

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TOTAL POINTS

3.5 / 5

QUESTION 1

1 Q1 **2 / 3**

+ **0** Nothing is correct

+ **1** Only few steps are correct

✓ + **2** **Partially correct**

+ **3** Fully correct

QUESTION 2

2 Q2 **1.5 / 2**

+ **0** Nothing is correct

+ **0.5** Sensitivity list explanation

✓ + **0.5** **Sensitivity list example**

✓ + **0.5** **Clock edge & initialization signal explanation**

✓ + **0.5** **Clock edge & initialization signal example**

SET B

Left neighbor	Your Name	Your Entry No.	Right neighbour
Udit Jain	Samarth Aggarwal	2016CS10395	Ujjwal Gupta

COL215 Digital Logic and System Design **Quiz 2** **20.09.2017**

Q 1. Show all the steps of binary unsigned division of 11001110 by 00001101 using the method in which dividend and quotient shift together and the divisor does not shift.

Q 2. While describing a sequential circuit using a process in VHDL, how would you **ensure** that it is fully synchronous except for initialization? Give your answer with illustrations.

A1) At every step, dividend shifts left and the new bit generated is filled by a bit of quotient.
~~Initially~~

~~0~~
~~00001101 | 0000000011001110~~
~~- 00000000~~
~~00000001100111 00~~
~~- 00000000~~
~~00000~~

12×16 + 14 = 206

13)206 -13 / 76 -65 / 11

0 × 2^7

0000111
00001101 | 0000000011001110
- 00000000
0000000011001110
0000000110011100 (left shift)
- 00000000
0000000110011100
0000001100111000 (left shift)
- 00000000
0000001100111000
0000011001110000 (left shift)
- 00000000
~~000000000~~
0000011001110000
0000110011100000 (left shift)
- 00001101
0000011001100000
0000110011000001
- 00001101
0000011001000001
0000110010000011
- 00001101
0000011000000011

```
0 0 0 0 1 1 0 0 0 0 0 0 0 1 1 1   (left shift)
- 0 0 0 0 0 0 0 0
-----------------
0 0 0 0 1 1 0 0 0 0 0 0 0 1 1 1
```

A2) process (clk)

begin
if clk = '1' and clk'event then
{
}
end if
end process

I will ensure a synchronous process by executing the loop only when the clk changes hence the circuit is synchronous.