Left neighbour	Your Name	Your Entry No.	Right neighbour

COL215 Digital Logic and System Design Quiz 4 16.11.2017

Q 1. A VHDL description below uses a case statement in a process. Give an equivalent VHDL description for the architecture without using any of the following - process, case statement, if statement, conditional signal assignment and selected signal assignment.

```
entity example is
  port (
    s : input bit_vector (1 downto 0);
    y : output bit_vector (3 downto 0)
  )
```

```
architecture casestmt of example is
begin
  process (s)
    begin
      case s is
         when “00”       => y <= “0001”;
         when “01”       => y <= “0010”;
         when “10”       => y <= “0100”;
         when others     => y <= “1000”;
       end case;
  end process;
end architecture casestmt;
```

```
architecture dataflow of example is
begin
    y (0) <= not s (1) and not s (0);
    y (1) <= not s (1) and s (0);
    y (2) <= s (1) and not s (0);
    y (3) <= s (1) and s (0);
end architecture dataflow;
```

[1 mark]

Another way:

```
architecture dataflow of example is
begin
    y <= (not s (1) and not s (0)) &
         (not s (1) and s (0)) &
         (s (1) and not s (0)) &
         (s (1) and s (0));
end architecture dataflow;
```

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Q 2. Consider addition of two n-bit signed integers using 2's complement representation. Show that when two numbers with opposite signs are added, carries c_n and c_{n-1} are always equal. What does it imply about overflow?

Solution:

Let the two numbers be $A = a_{n-1}\ a_{n-2}\ \ldots\ a_1\ a_0$ and $B = b_{n-1}\ b_{n-2}\ \ldots\ b_1\ b_0$.
Without any loss of generality, let us assume that A is non-negative and B is negative. That is, $a_{n-1} = 0$ and $b_{n-1} = 1$. Let us now examine addition of a_{n-1} and b_{n-1} with carry c_{n-1}.

Case (i)
Let $c_{n-1} = 0$
Addition of a_{n-1} and b_{n-1} with carry c_{n-1} means adding 0, 1 and 0.
We get carry $c_n = 0$, which is same as c_{n-1}

Case (ii)
Let $c_{n-1} = 1$
Addition of a_{n-1} and b_{n-1} with carry c_{n-1} means adding 0, 1 and 1.
We get carry $c_n = 1$, which is again same as c_{n-1}

This shows that in both cases $c_n = c_{n-1}$. [1/2 mark]

This condition implies absence of overflow, which is consistent with the fact that the magnitude of the sum of two oppositely signed numbers will always be less than or equal to the magnitude of each of the numbers. [1/2 mark]

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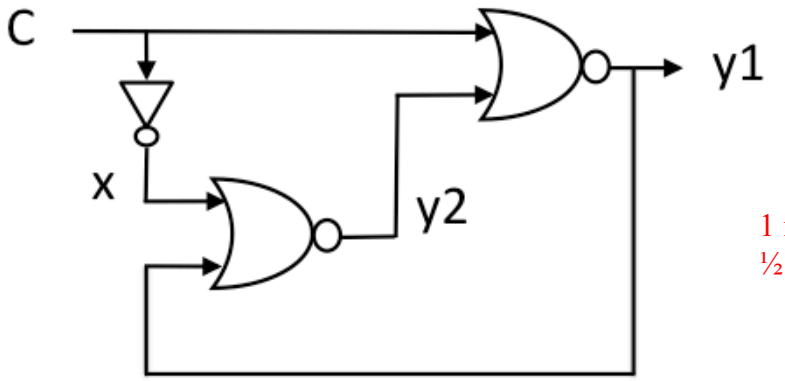
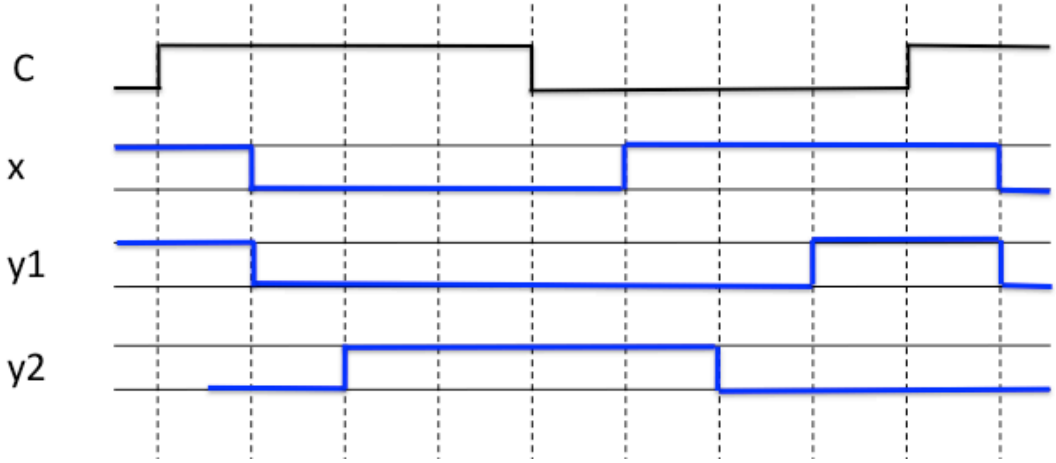
Q 3. In the circuit shown below, the input C is a square wave with time period = 8 units. Draw the waveforms for signals x, y1 and y2, assuming the delay of each gate (NOR as well as NOT) to be 1 unit.



1 mark if all 3 waveforms are correct.
½ mark if 2 waveforms are correct.



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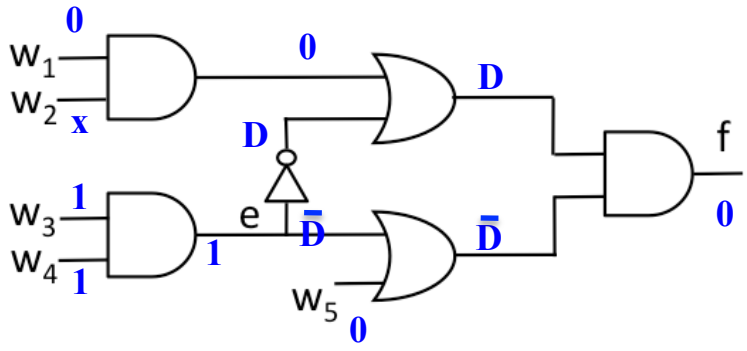
Q 4. Test input generation for e stuck_at_0 fault is being attempted for the circuit shown below using D - algorithm. Which input combination will result in cancellation of D and $\bar{D}$? What will be observed at output f under that condition?



$\bar{D}$ at the fault site results in D at the output of the inverter. These propagate through the OR gates if these gates have other inputs 0. Then these get cancelled at the AND gate. Input combination which cause this is w1, w2, w3, w4, w5 = 0x110 or
w1, w2, w3, w4, w5 = x0110.
(D and $\bar{D}$ are interchangeable).

[1 mark for any of the two answers]