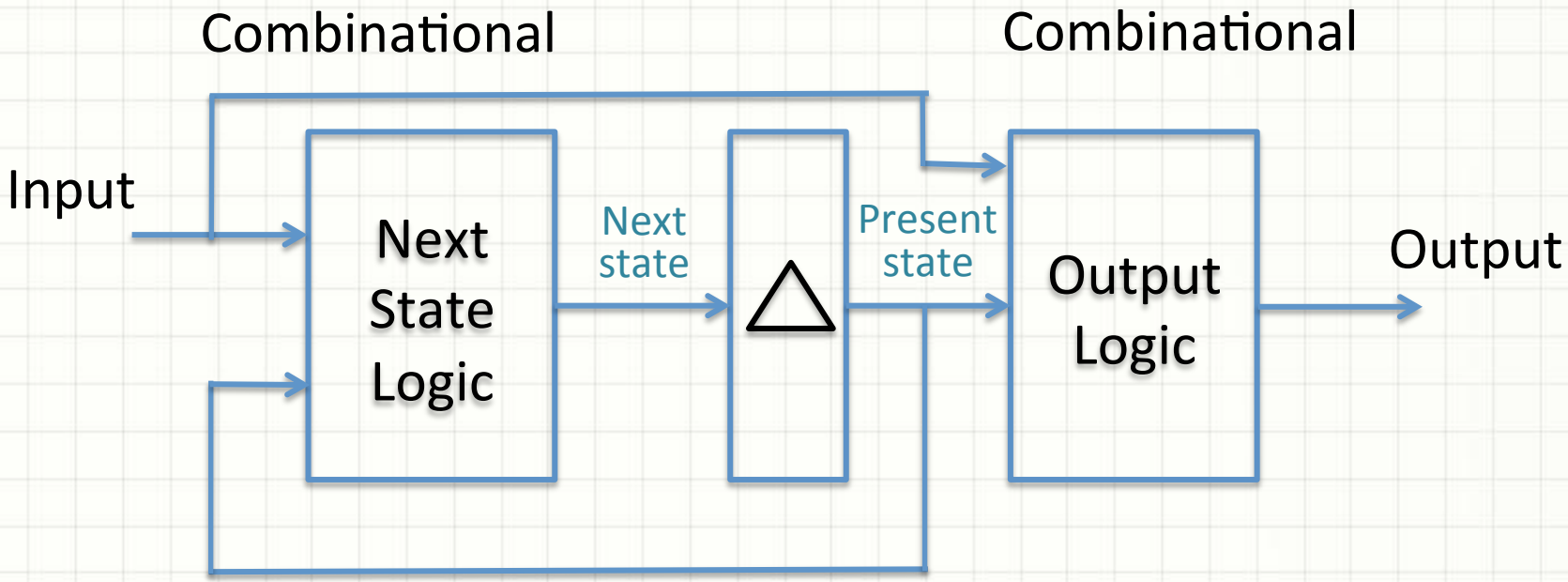
# COL215 Digital Logic and System Design

Design of asynchronous FSMs

08 November 2017

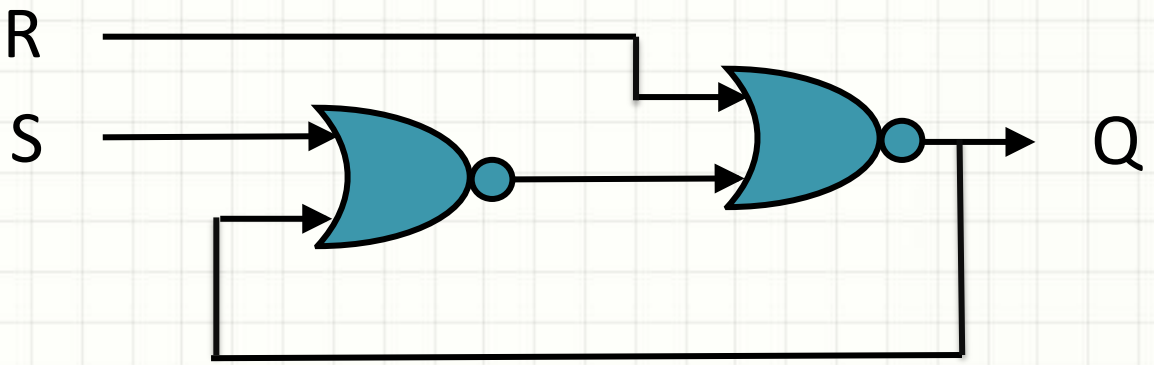
# Asynchronous FSM (Mealy)



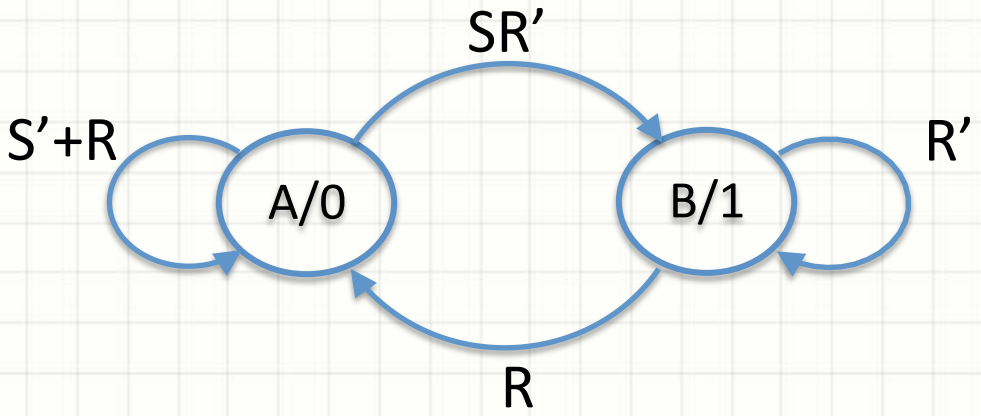
# Set-Reset (SR) Latch

R : Reset

S : Set




| Present state y | Next state Y | | | | Output Q |
|---|---|---|---|---|---|
| | SR = 00 | SR = 01 | SR = 10 | SR = 11 | |
| A | A | A | B | A | 0 |
| B | B | A | B | A | 1 |



# Analysis

Circuit =>

Excitation table =>

Flow table =>

State diagram

# Synthesis

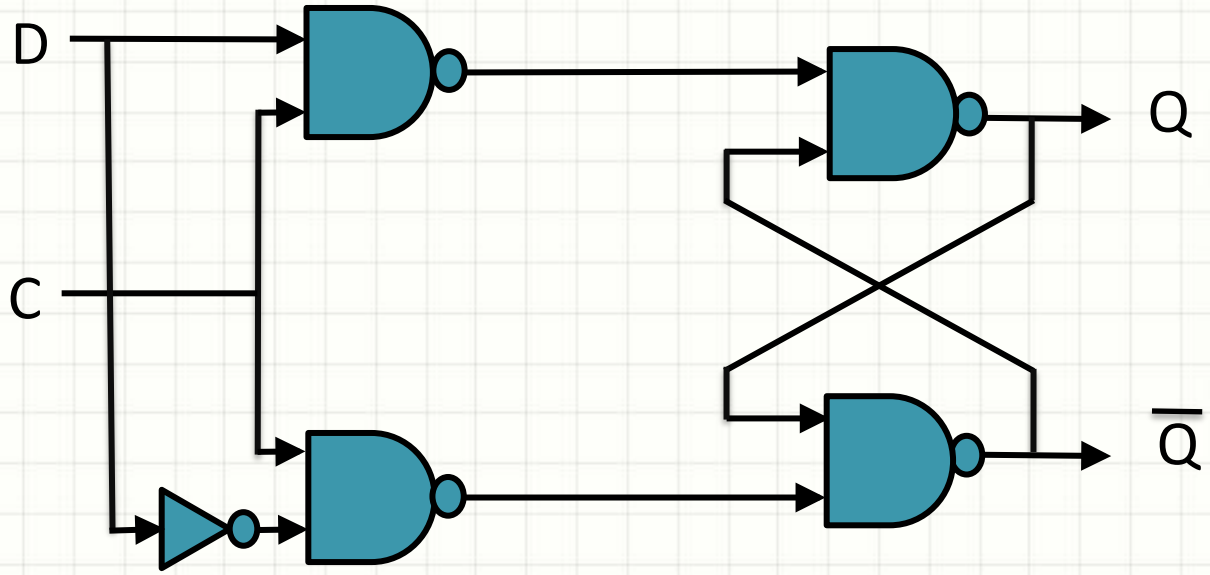
State diagram =>

Flow table =>

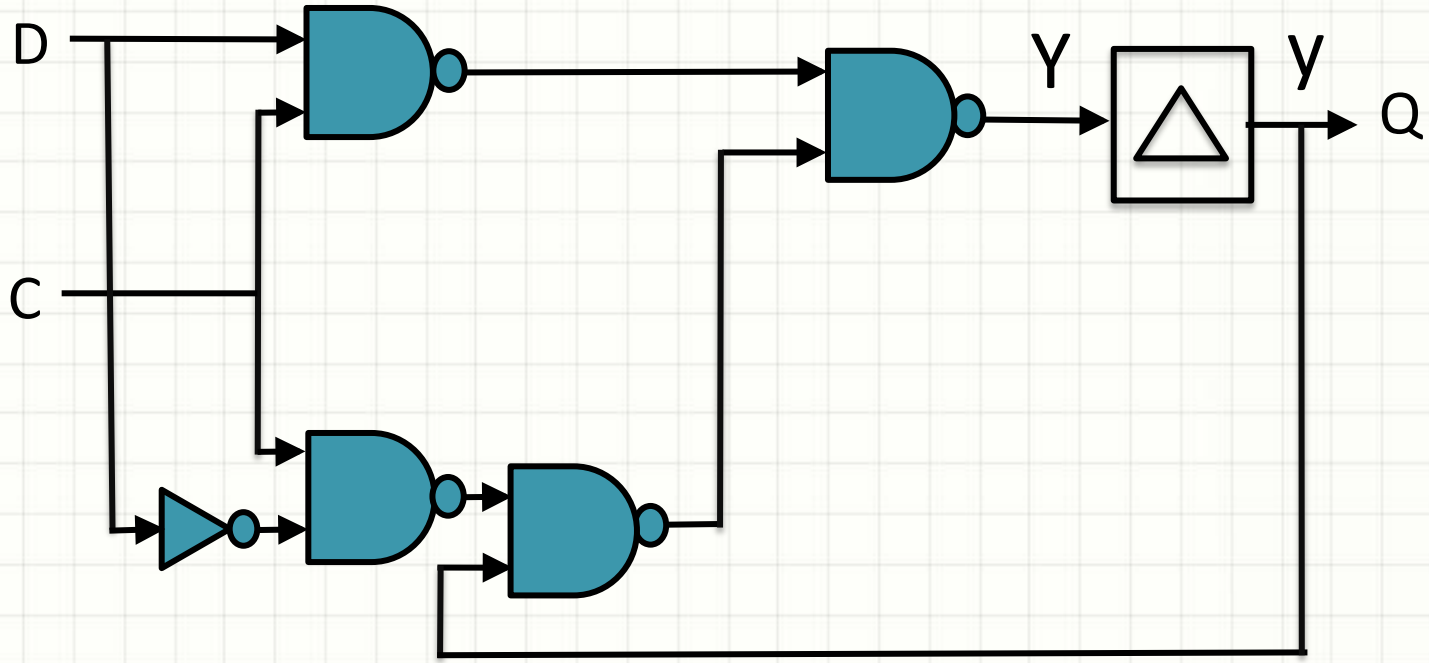
Excitation table =>

Circuit

# Gated D Latch



# Gated D Latch




$$Y = ((C.D)'.((C.D')'.y)')' = C.D + (C.D')'.y$$
$$= C.D + (C' + D).y = C.D + C'.y + D.y$$
$$= C.D + C'.y$$

# State assigned table (excitation table)

$$Y = C.D + C'.y$$

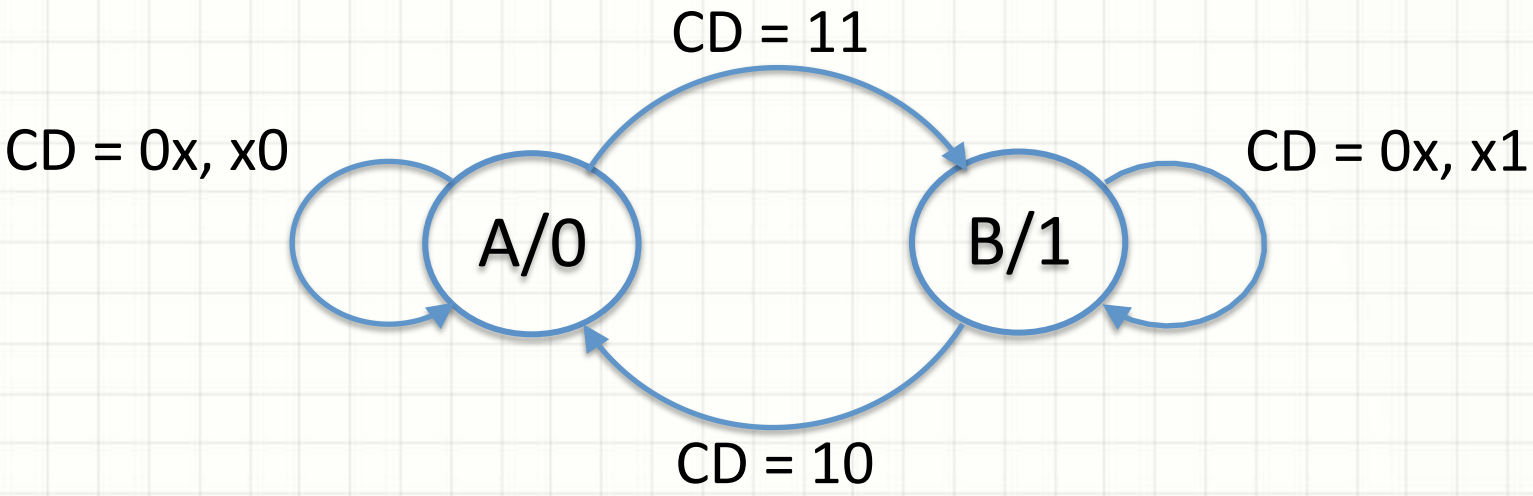
| Present state y | Next state Y | | | | Output Q |
|---|---|---|---|---|---|
| | CD = 00 | CD = 01 | CD = 10 | CD = 11 | |
| 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 |

# State transition table (flow table)

| Present state y | Next state Y | | | | Output Q |
|---|---|---|---|---|---|
| | CD = 00 | CD = 01 | CD = 10 | CD = 11 | |
| A | A | A | A | B | 0 |
| B | B | B | A | B | 1 |

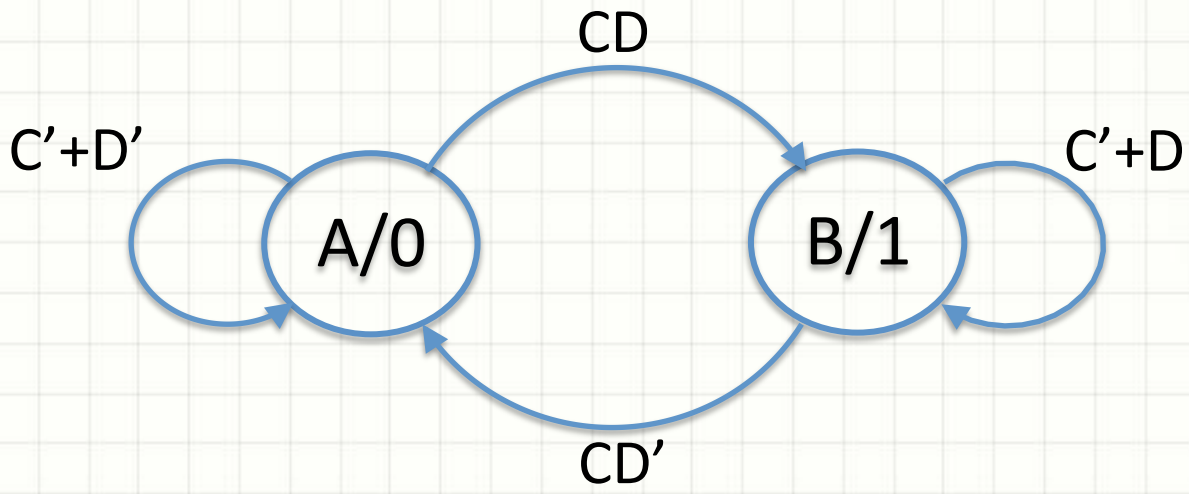
# State transition diagram

| Present state y | Next state Y | | | | Output Q |
|---|---|---|---|---|---|
| | CD = 00 | CD = 01 | CD = 10 | CD = 11 | |
| A | A | A | A | B | 0 |
| B | B | B | A | B | 1 |

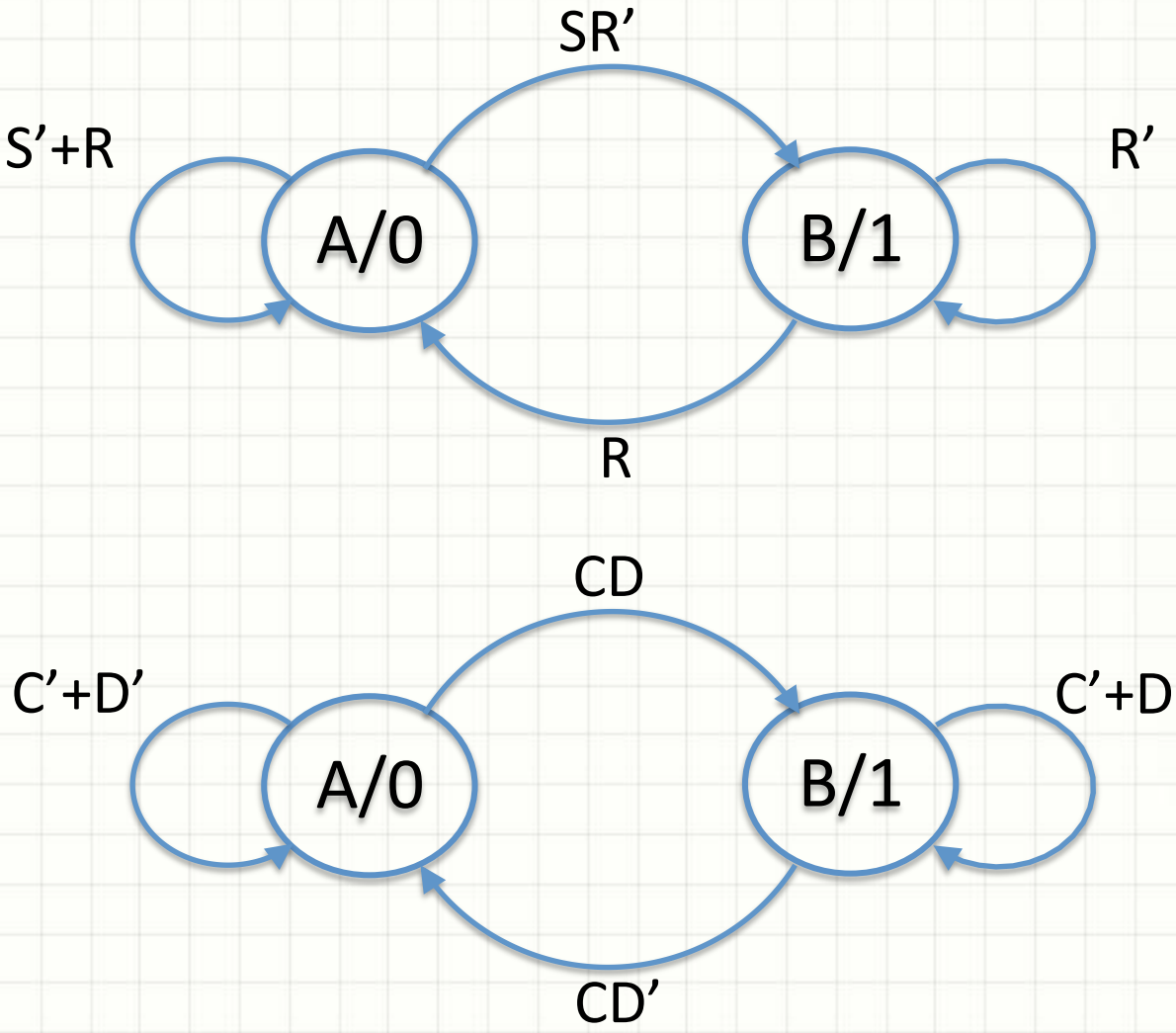


# State transition diagram

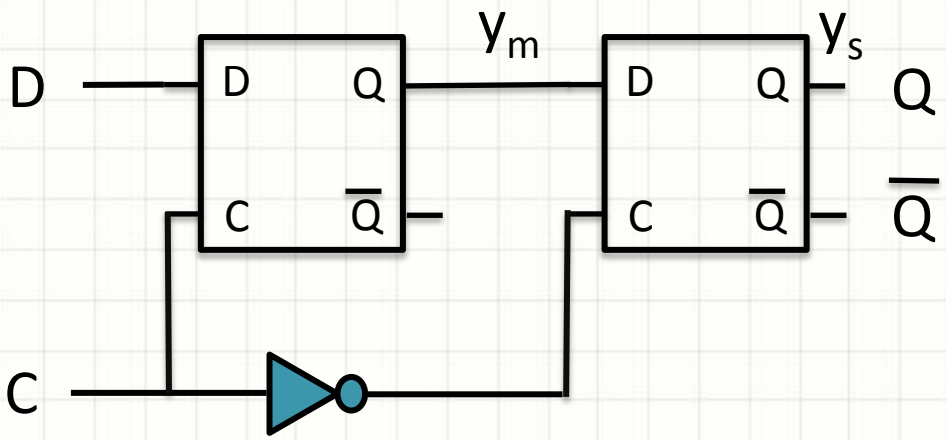
| Present state y | Next state Y | | | | Output Q |
|---|---|---|---|---|---|
| | CD = 00 | CD = 01 | CD = 10 | CD = 11 | |
| A | A | A | A | B | 0 |
| B | B | B | A | B | 1 |



# Comparing SR latch and D latch



# Master-Slave D Flip-FLop




$$Y_m = C.D + C'.y_m$$
$$Y_s = C'.y_m + C.y_s$$

# Excitation table

$$Y_m = C.D + C'.y_m$$
$$Y_s = C'.y_m + C.y_s$$

| Present state $y_m y_s$ | Next state $Y_m Y_s$ | | | | Output Q |
|---|---|---|---|---|---|
| | CD = 00 | CD = 01 | CD = 10 | CD = 11 | |
| 00 | 00 | 00 | 00 | 10 | 0 |
| 01 | 00 | 00 | 01 | 11 | 1 |
| 10 | 11 | 11 | 00 | 10 | 0 |
| 11 | 11 | 11 | 01 | 11 | 1 |

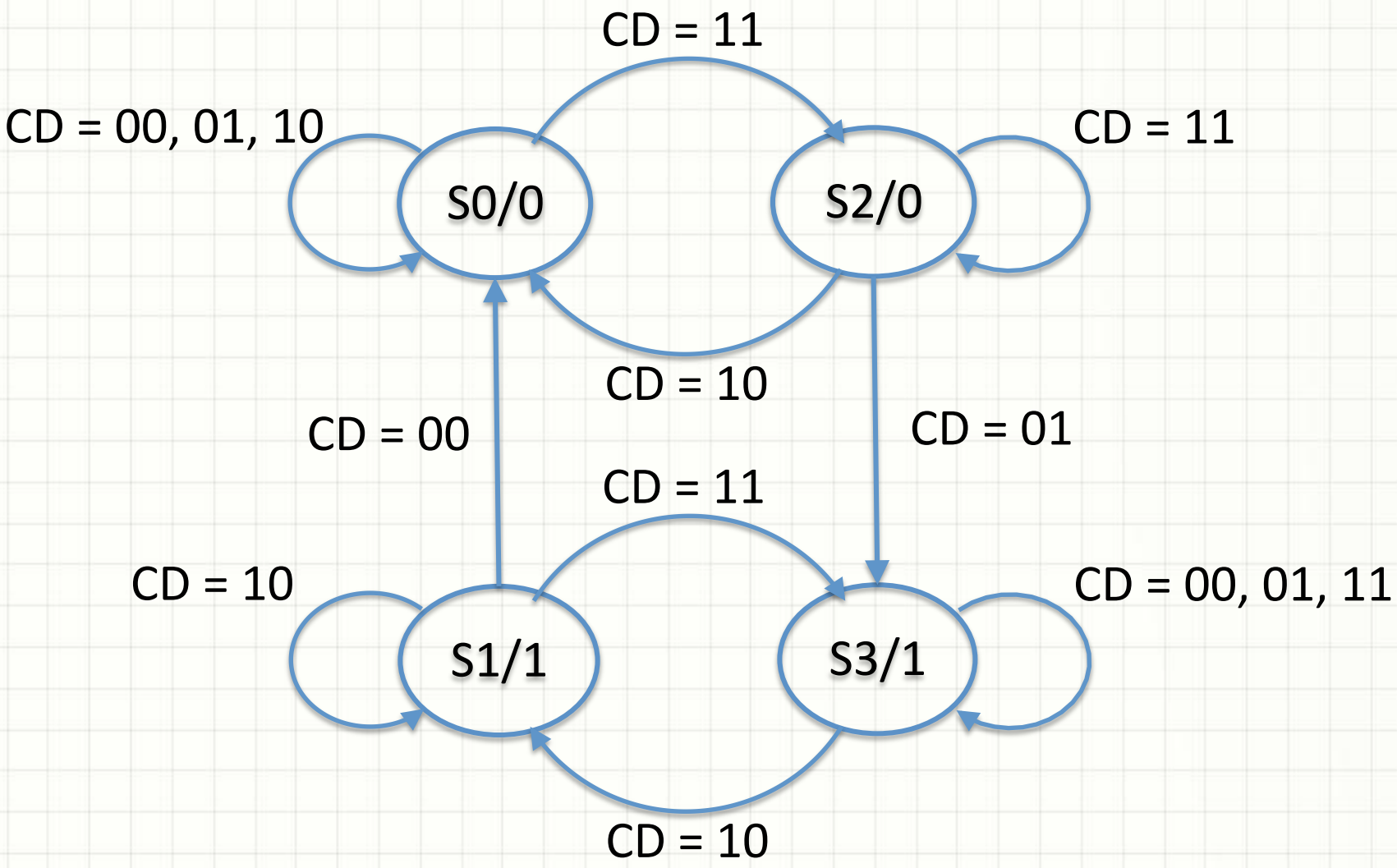
# Flow table

| Present state | Next state | | | | Output Q |
|---|---|---|---|---|---|
| | CD = 00 | CD = 01 | CD = 10 | CD = 11 | |
| S0 | S0 | S0 | S0 | S2 | 0 |
| S1 | S0 | S0 | S1 | S3 | 1 |
| S2 | S3 | S3 | S0 | S2 | 0 |
| S3 | S3 | S3 | S1 | S3 | 1 |

# Flow table with single input change

| Present state | Next state | | | | Output Q |
|---|---|---|---|---|---|
| | CD = 00 | CD = 01 | CD = 10 | CD = 11 | |
| S0 | S0 | S0 | S0 | S2 | 0 |
| S1 | S0 | - | S1 | S3 | 1 |
| S2 | - | S3 | S0 | S2 | 0 |
| S3 | S3 | S3 | S1 | S3 | 1 |

# State transition diagram



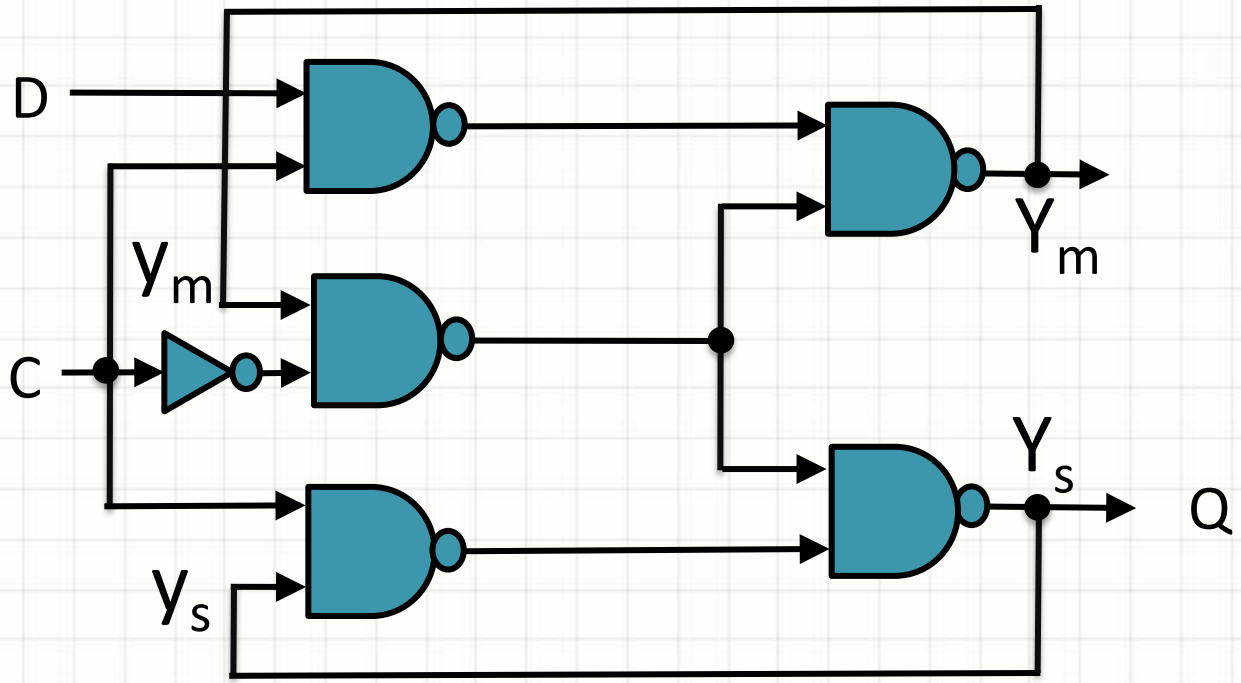
# Excitation table again

$$Y_m = C.D + C'.y_m$$
$$Y_s = C'.y_m + C.y_s$$

| Present state $y_m y_s$ | Next state $Y_m Y_s$ | | | | Output Q |
|---|---|---|---|---|---|
| | CD = 00 | CD = 01 | CD = 10 | CD = 11 | |
| 00 | 00 | 00 | 00 | 10 | 0 |
| 01 | 00 | 00 | 01 | 11 | 1 |
| 10 | 11 | 11 | 00 | 10 | 0 |
| 11 | 11 | 11 | 01 | 11 | 1 |

# M-S DFF circuit from excitation table

$$Y_m = C.D + C'.y_m$$
$$Y_s = C'.y_m + C.y_s$$



# Problems with asynchronous circuits

- Hazards
  - Concurrent changes in signal values can lead to glitches in output
- Races
  - Concurrent changes in state signals can lead to undesired state transitions