COL215 Quiz-2 SetB

SAMARTH AGGARWAL

TOTAL POINTS

3.5 / 5

QUESTION 1

1Q12/3

- + 0 Nothing is correct
- + 1 Only few steps are correct
- √ + 2 Partially correct
 - + 3 Fully correct

QUESTION 2

2 Q2 1.5 / 2

- + 0 Nothing is correct
- + 0.5 Sensitivity list explanation
- √ + 0.5 Sensitivity list example
- \checkmark + 0.5 Clock edge & initialization signal explanation
- √ + 0.5 Clock edge & initialization signal example

SET B

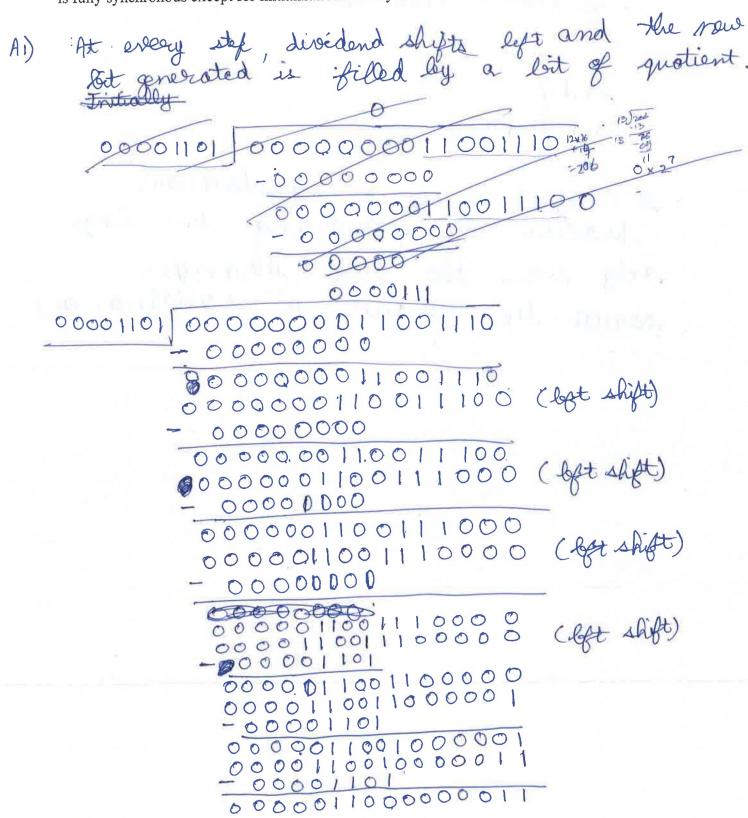
Your Name	Your Entry No.	Right neighbour
Samoethers	2016 CS10395	Upiwal Gupta
	10	Your Name Your Entry No. Samuelle Agranul 2016 CS 10395

COL215 Digital Logic and System Design

Quiz 2

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- Q 1. Show all the steps of binary unsigned division of 11001110 by 00001101 using the method in which dividend and quotient shift together and the divisor does not shift.
- Q 2. While describing a sequential circuit using a process in VHDL, how would you ensure that it is fully synchronous except for initialization? Give your answer with illustrations.



0000110000000111 (bpt shift) -00000000

As) process (clk)

begin if clk= 1) and clk event then

endif end process

process by executing the loop only when the alk changes hence the circuit is synchronous