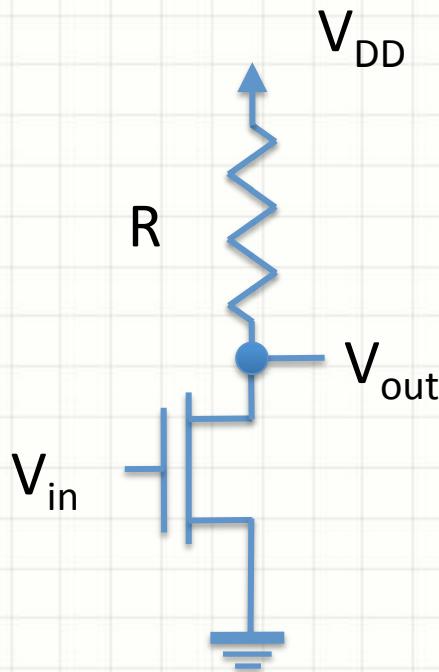




COL215 DIGITAL LOGIC AND SYSTEM DESIGN

Real Circuits :
Transistors and Gates
continued
19 September 2017

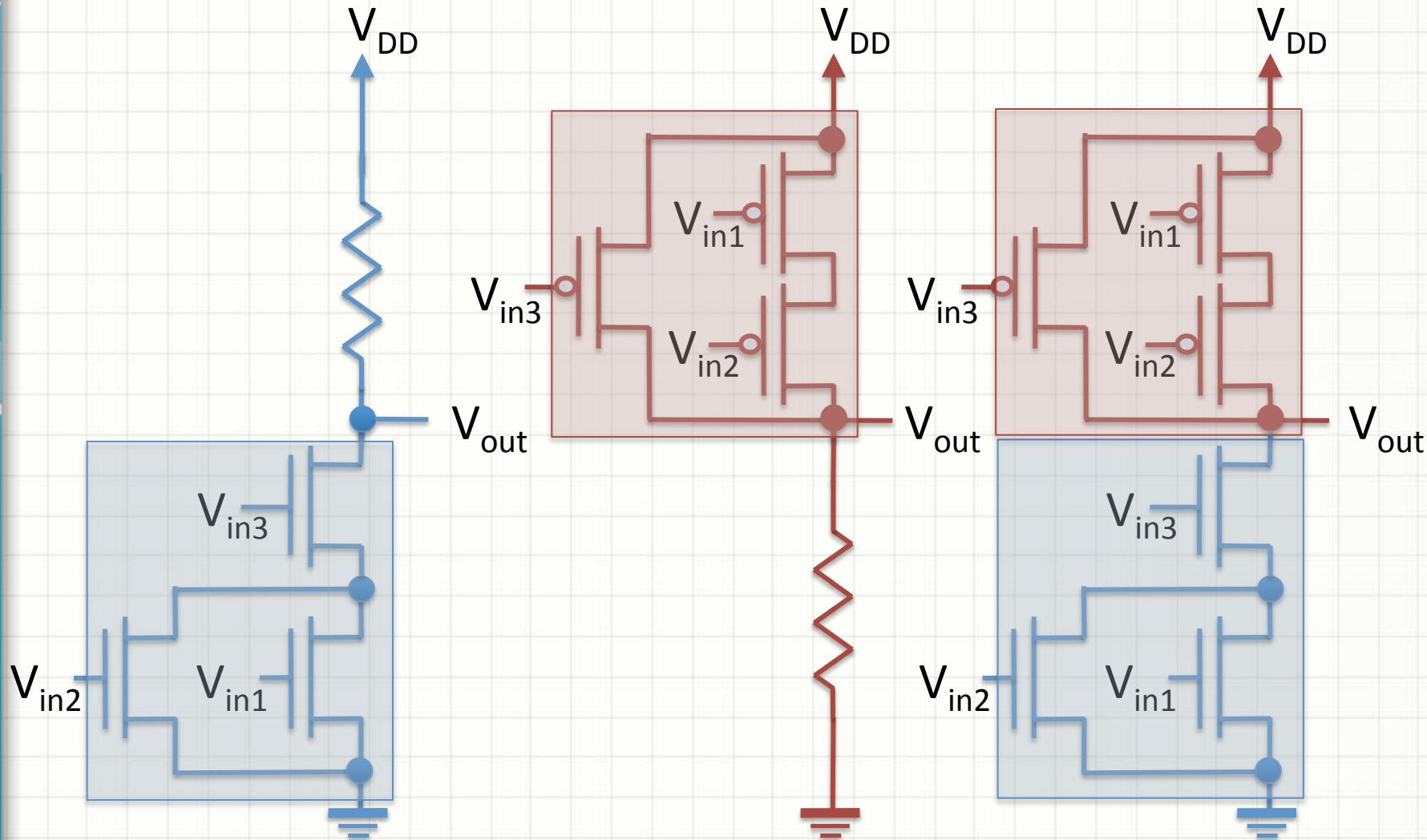
NMOS inverter, pull up options



- Passive
 - Resistor
- Active
 - Depletion mode transistor
 - Takes less silicon space

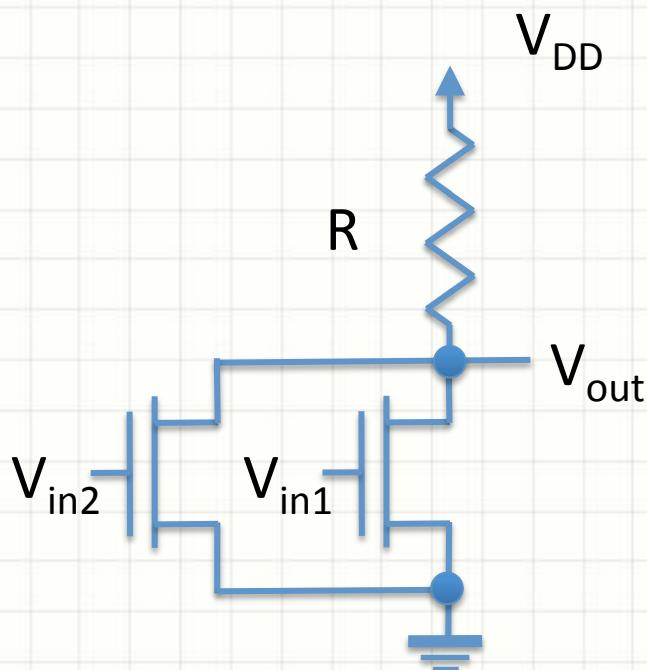


NMOS, PMOS, CMOS PDN and PUN





Positive and negative logic



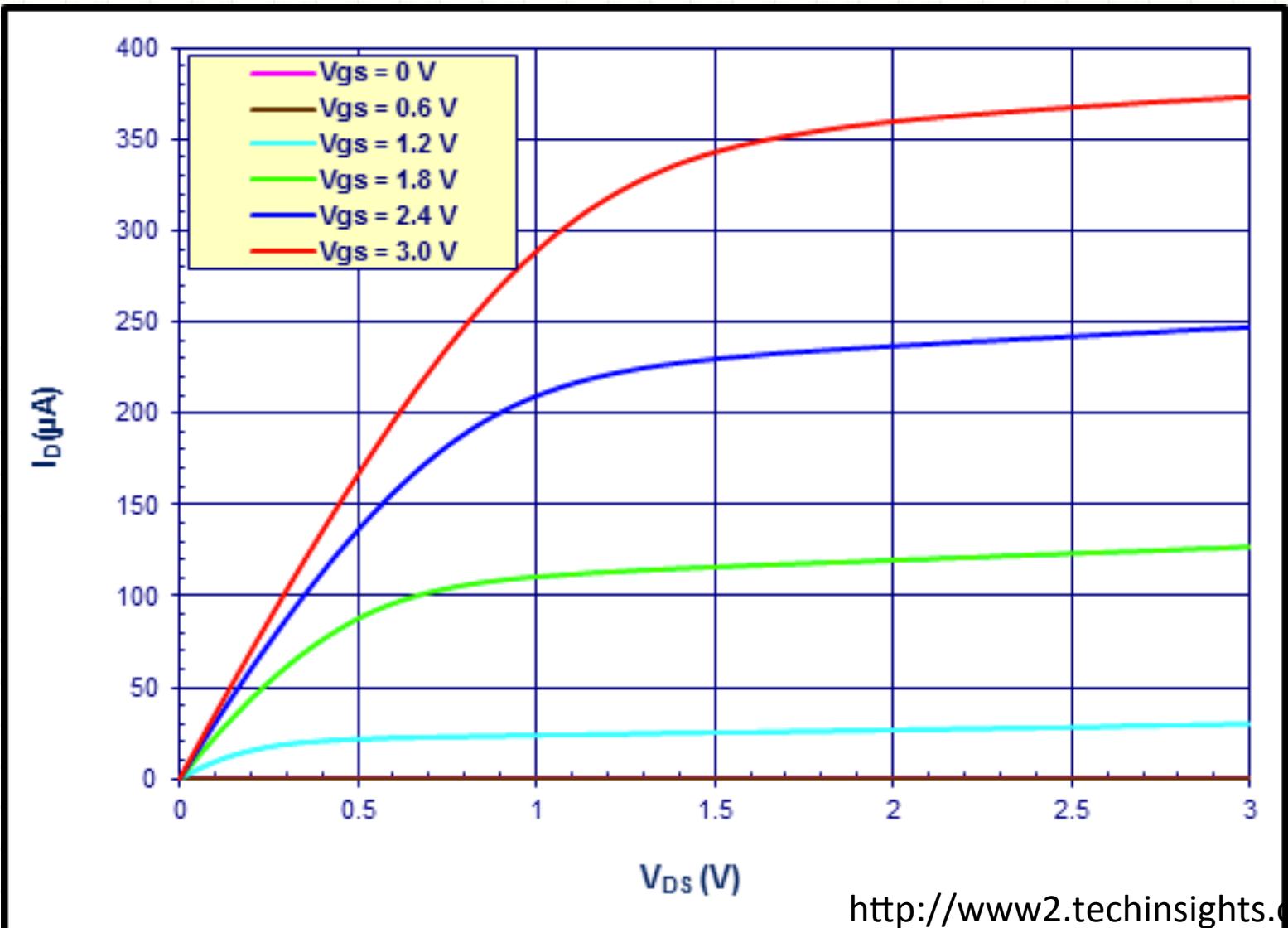
positive logic

V_{in1}	V_{in2}	V_{out}
Lo	Lo	Hi
Lo	Hi	Lo
Hi	Lo	Lo
Hi	Hi	Lo

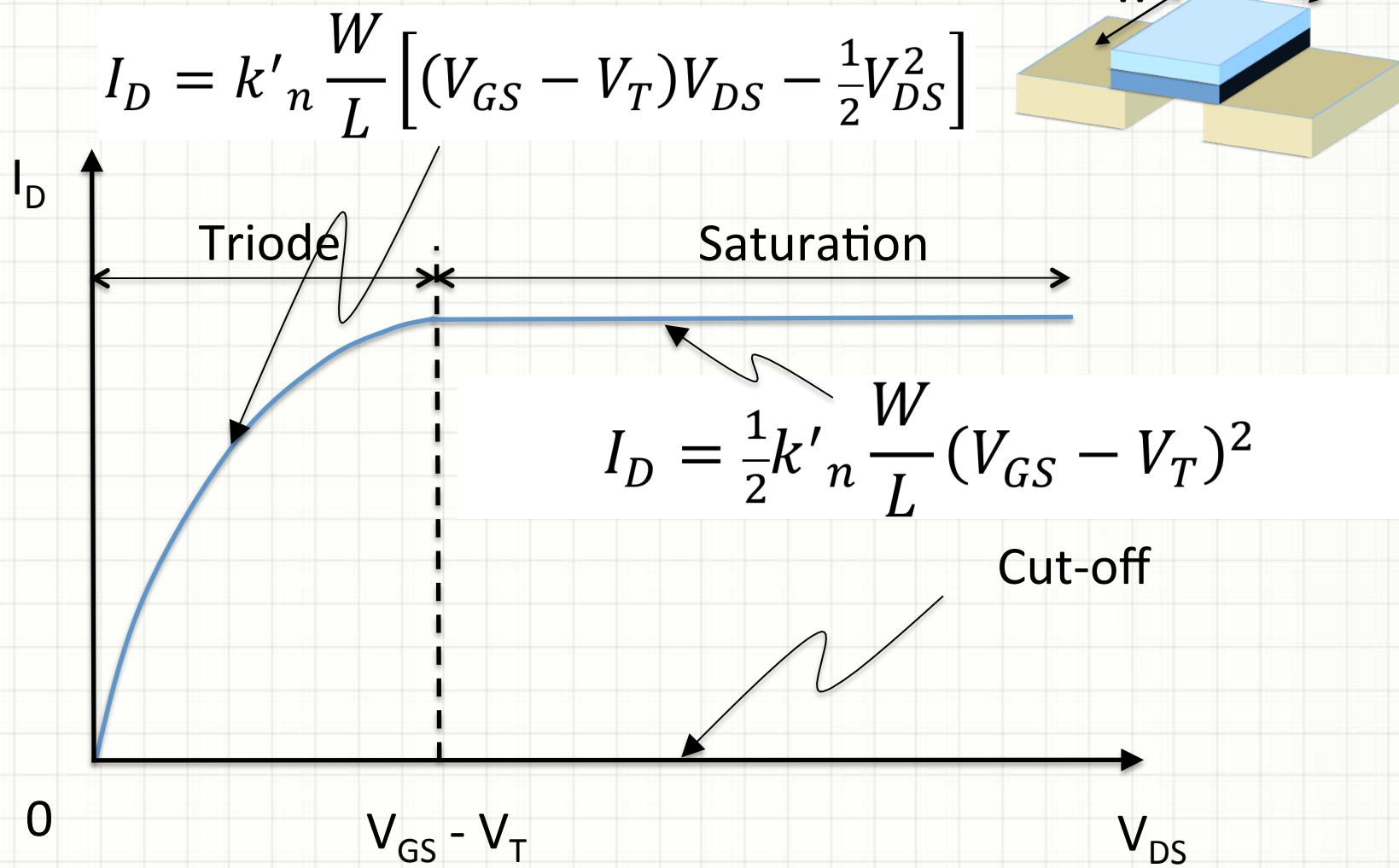
negative logic

V_{in1}	V_{in2}	V_{out}
0	0	1
0	1	0
1	0	0
1	1	0
V_{in1}	V_{in2}	V_{out}
1	1	0
1	0	1
0	1	1
0	0	1

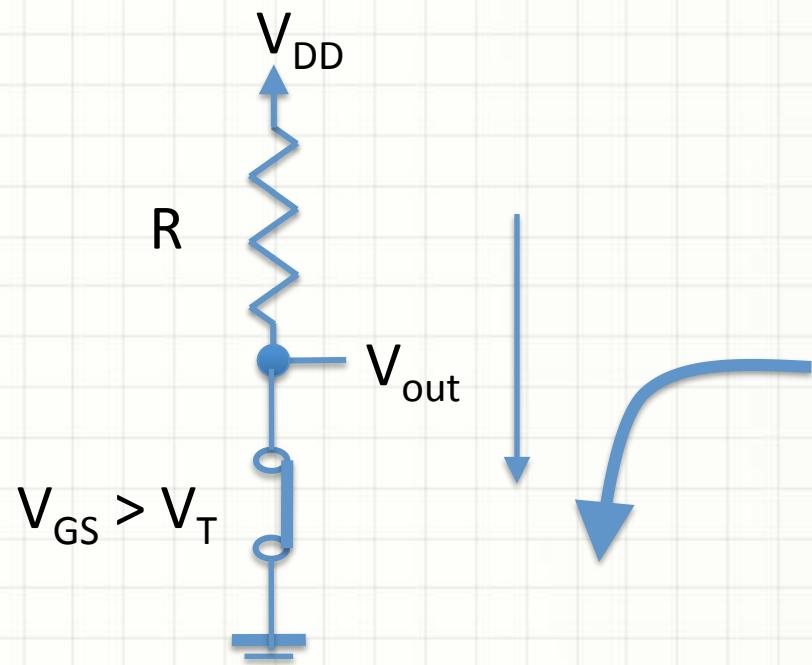
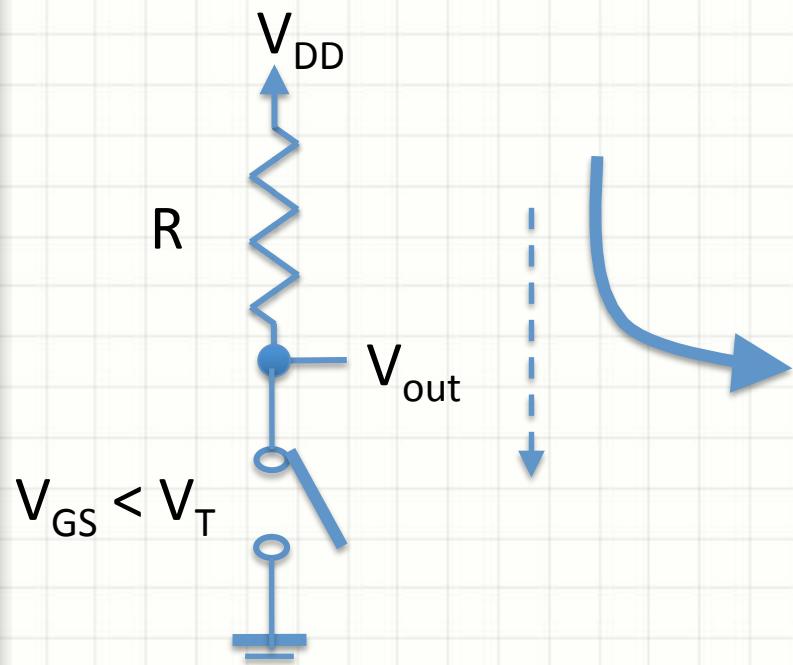
NMOS transistor V – I characteristics



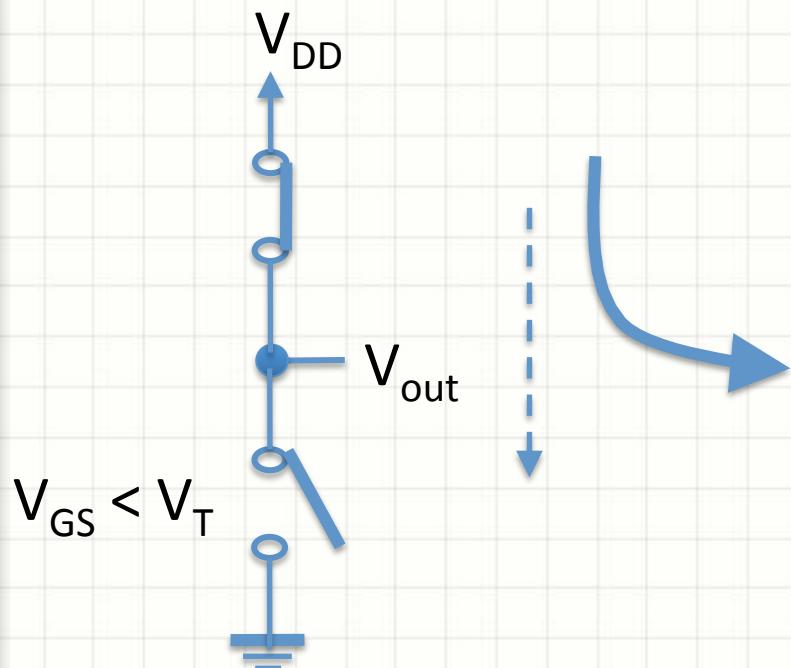
$V - I$ for a fixed V_{GS} (simplified)



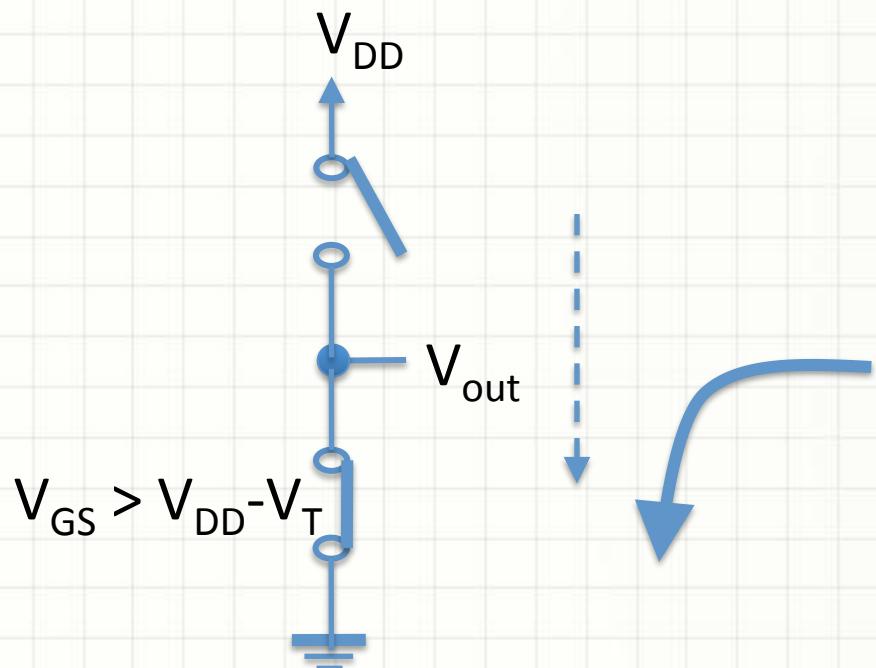
Voltage levels in NMOS inverter



Voltage levels in CMOS inverter



$$V_{OH} = V_{DD}$$



$$V_{OL} = 0$$

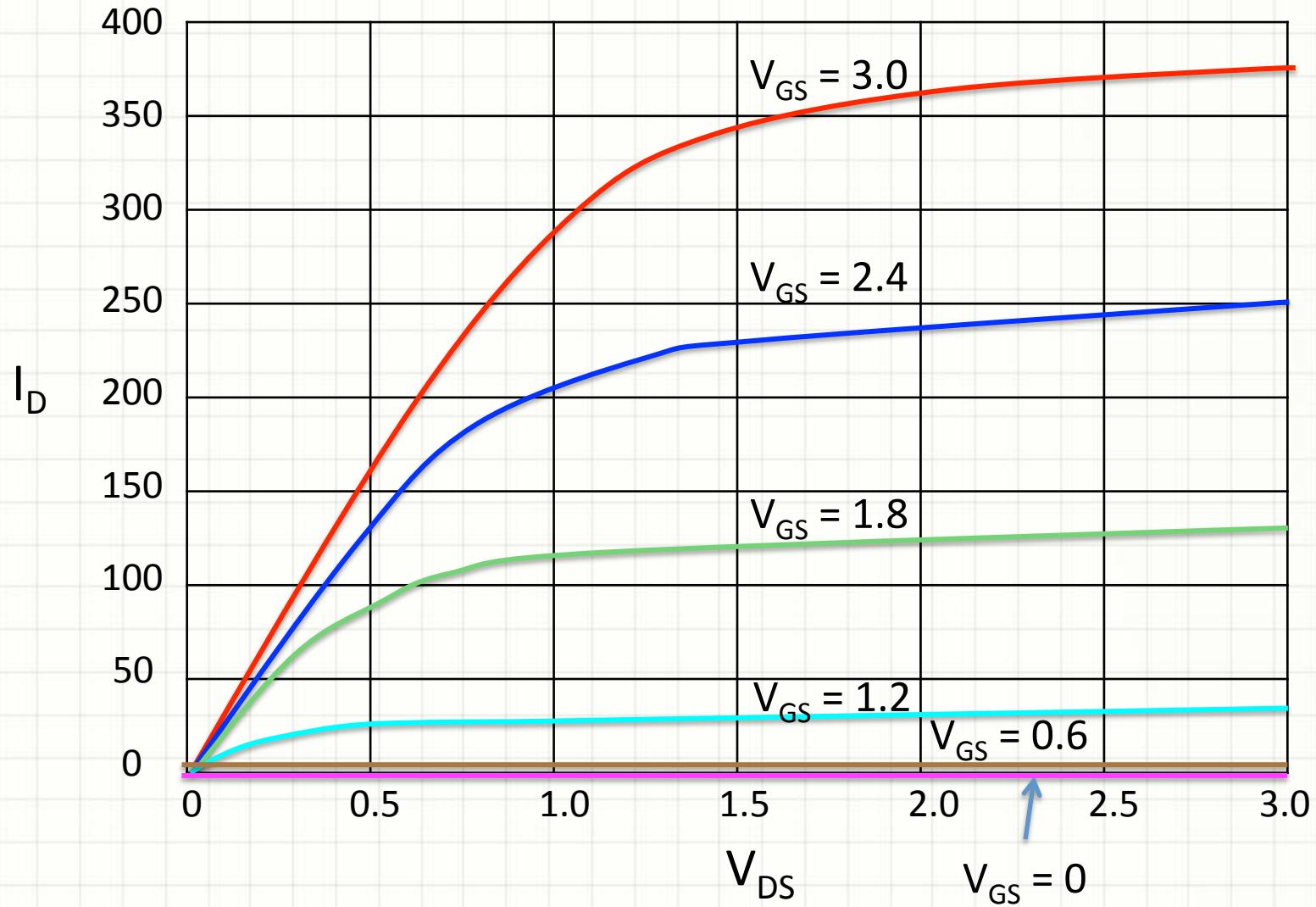
Analyse NMOS inverter

What is the output voltage for

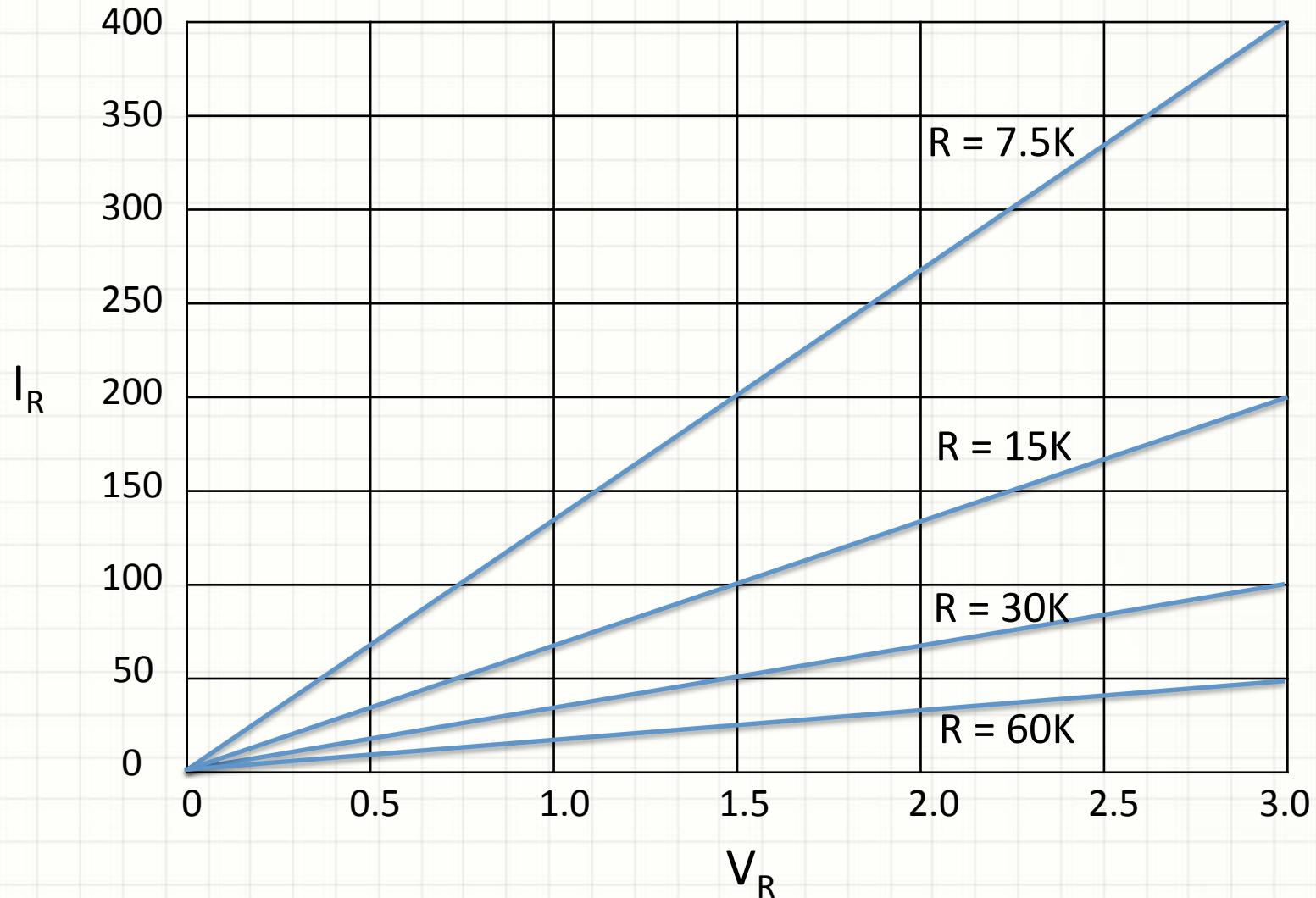
different V_{GS} values

for a given R?

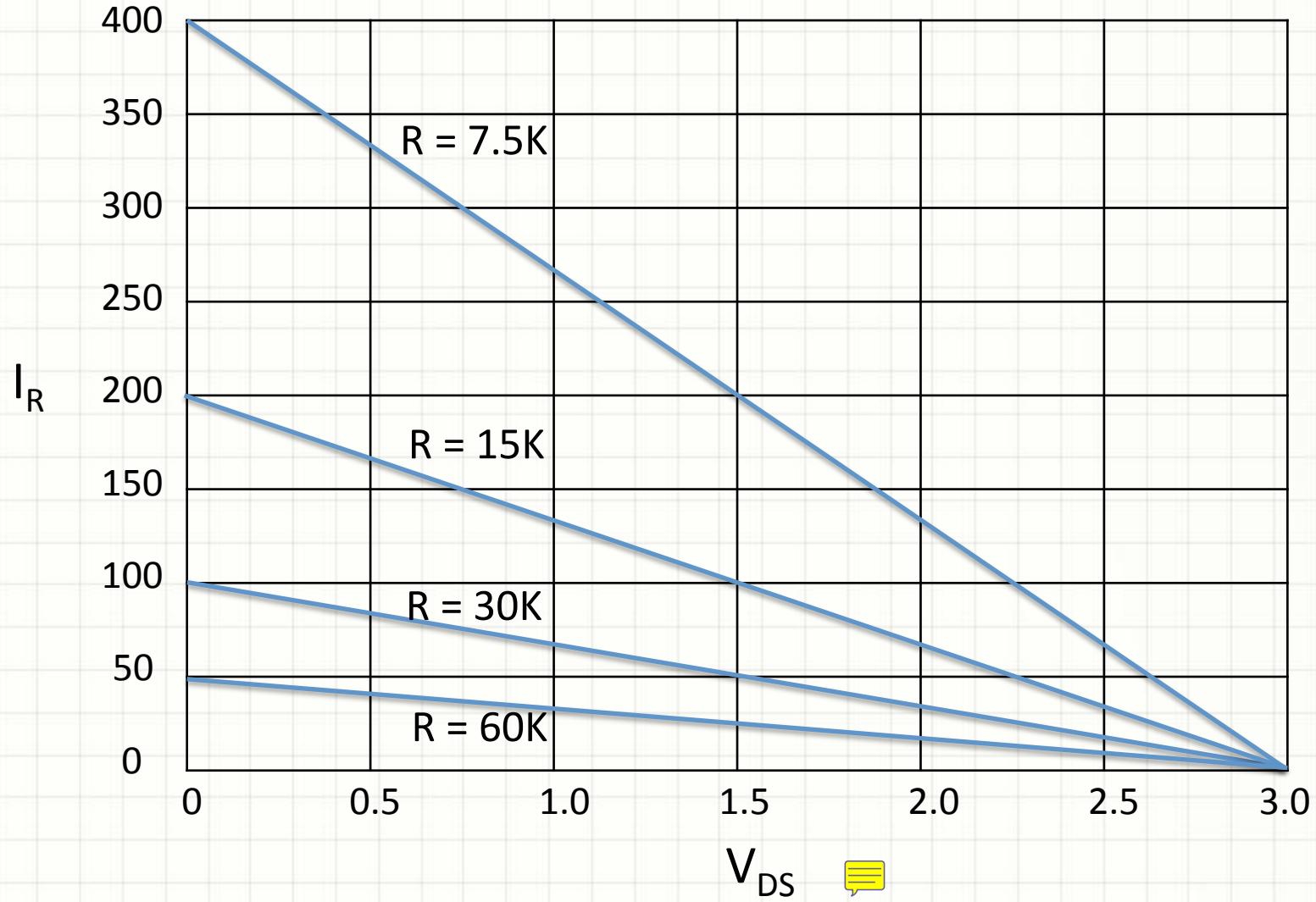
$V - I$ for NMOS Transistor



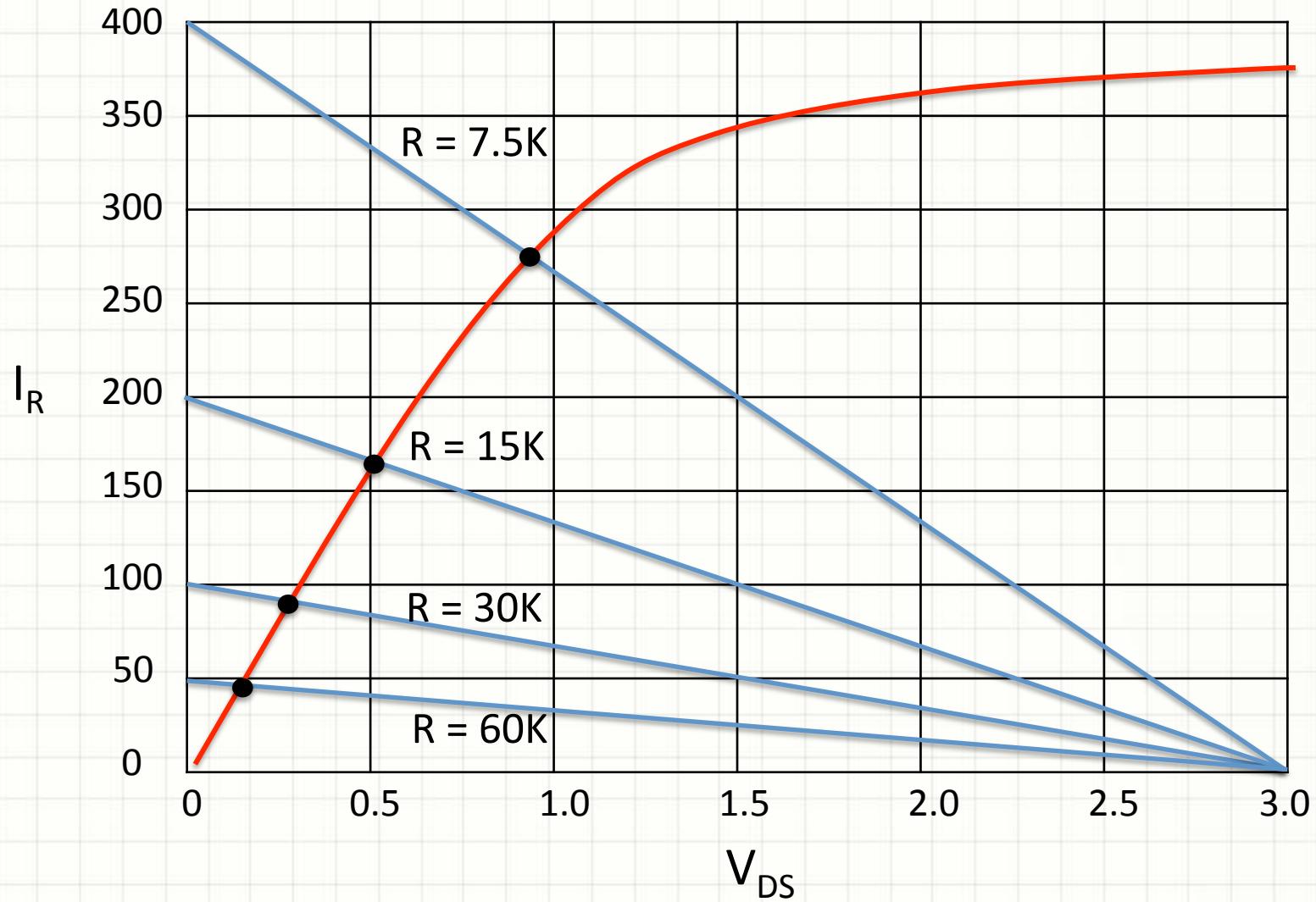
V – I for Resistor



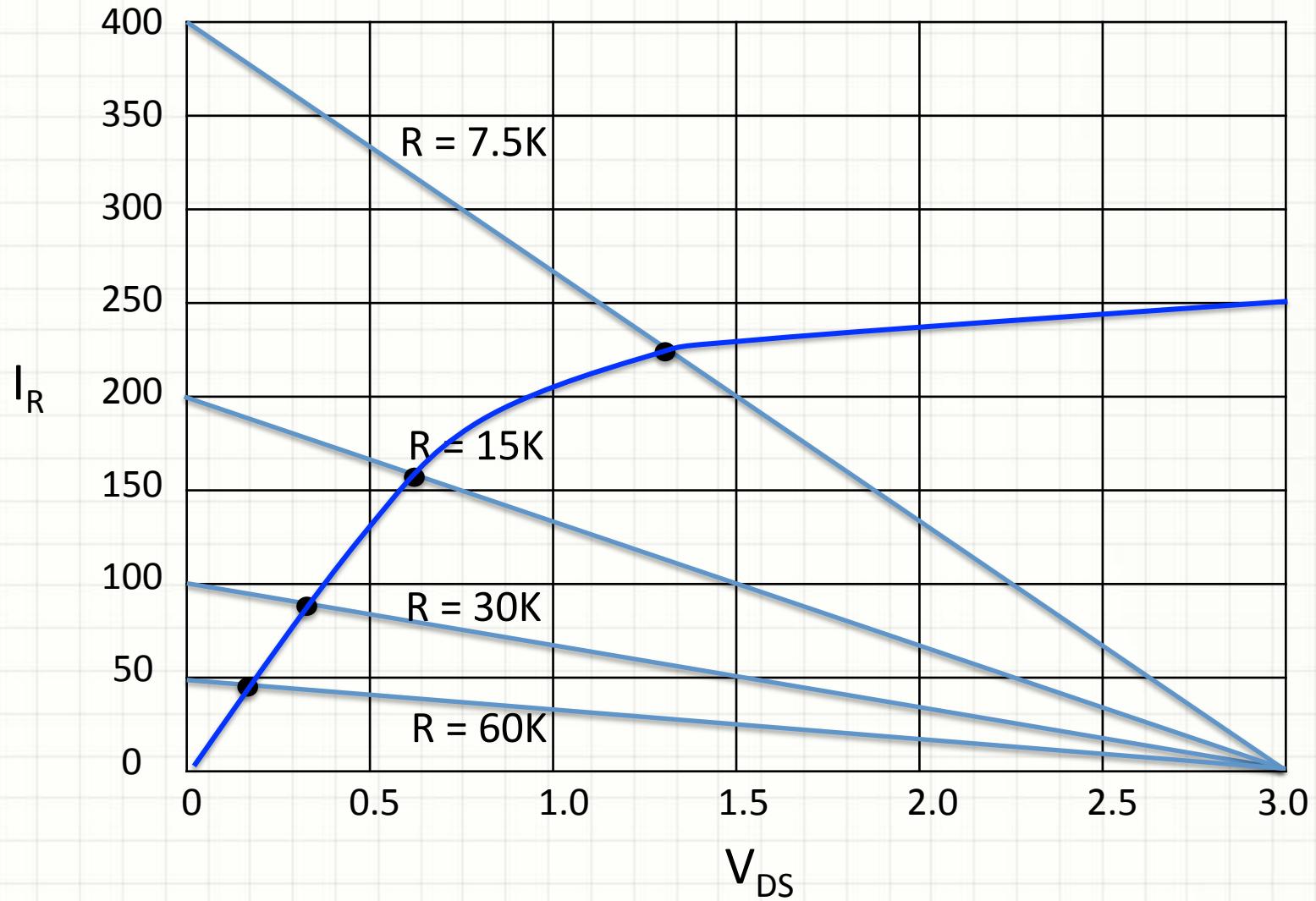
V – I for Resistor



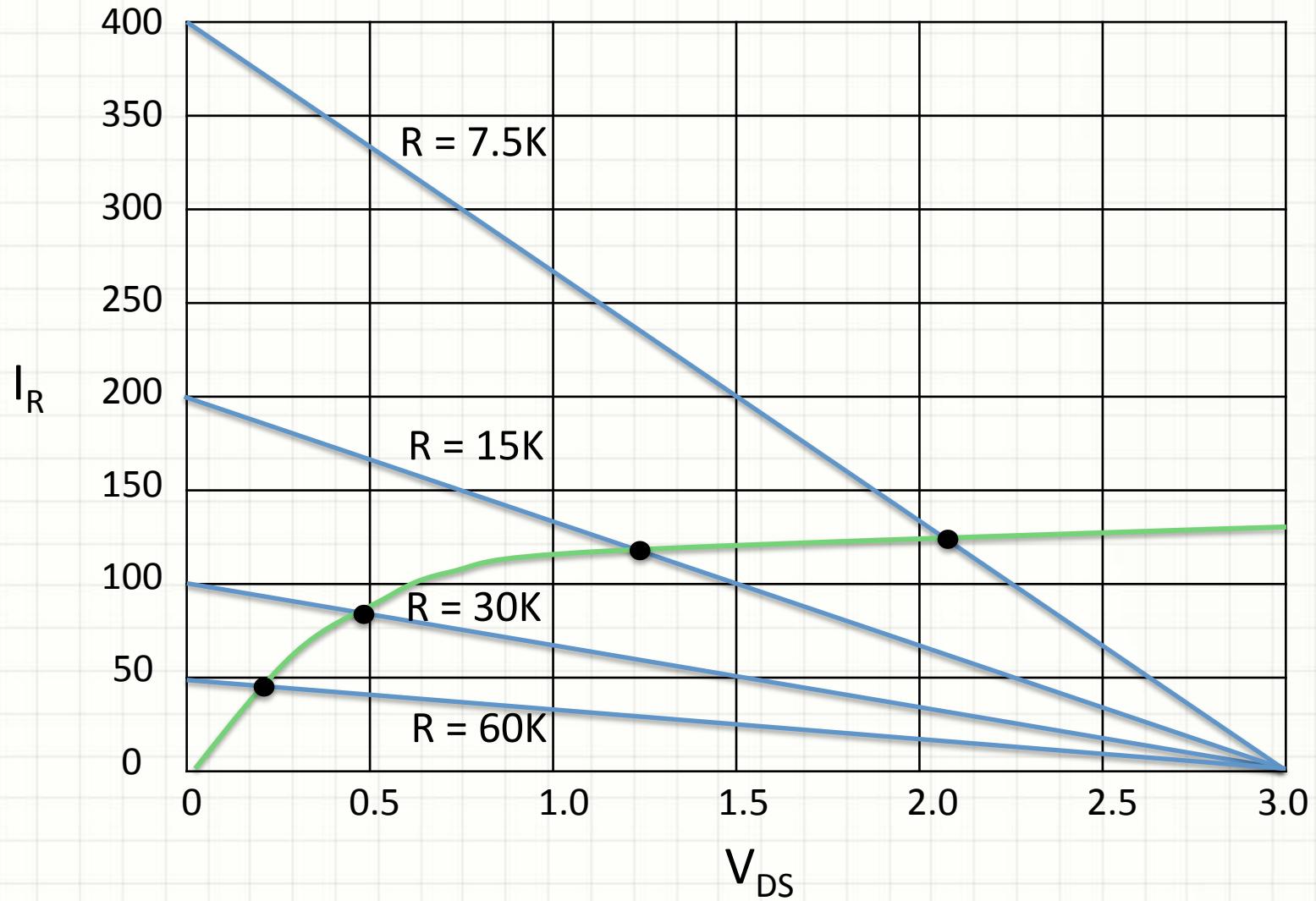
NMOS inverter, vary R, $V_{GS} = 3.0$ V



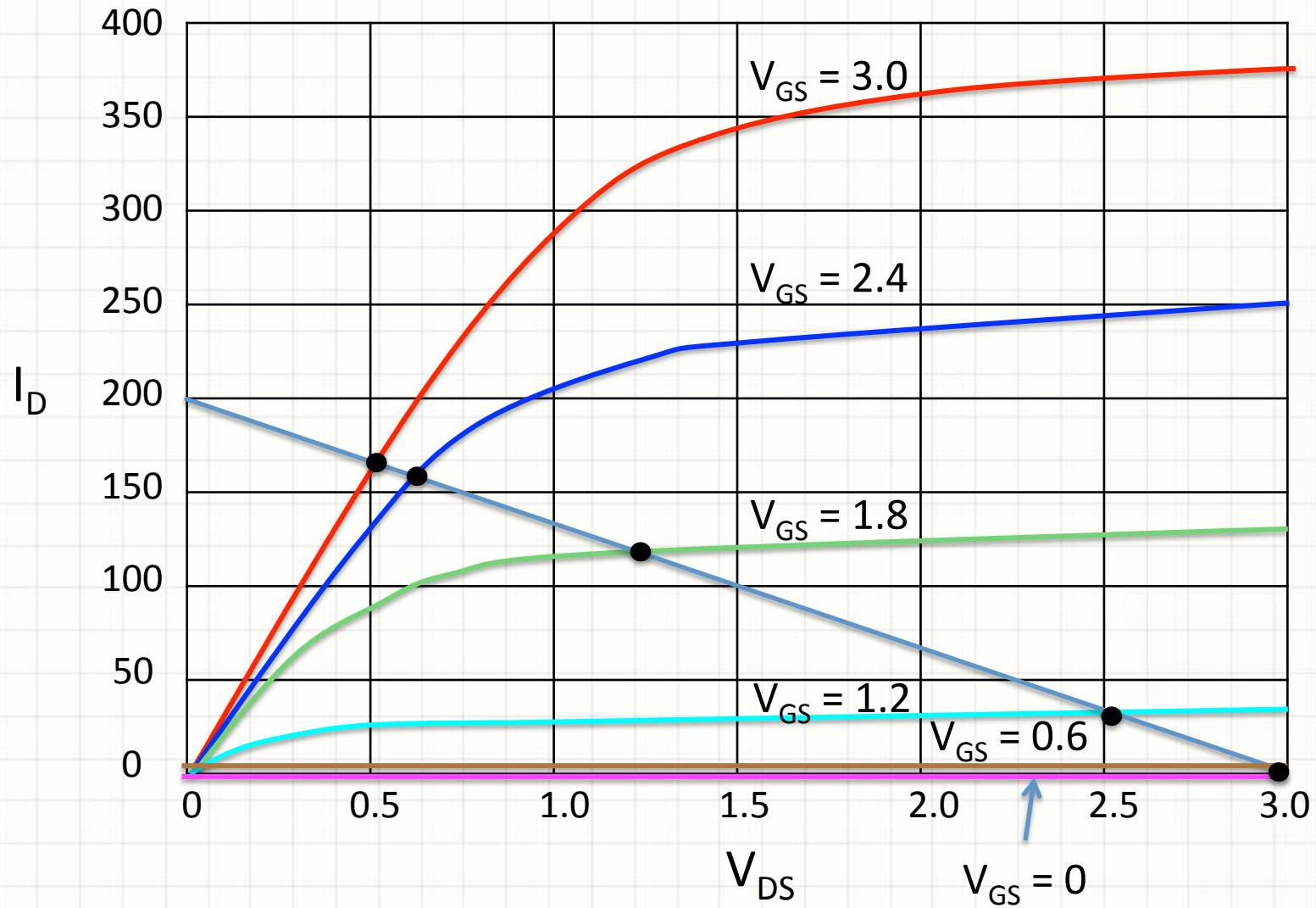
NMOS inverter, vary R, $V_{GS} = 2.4$ V



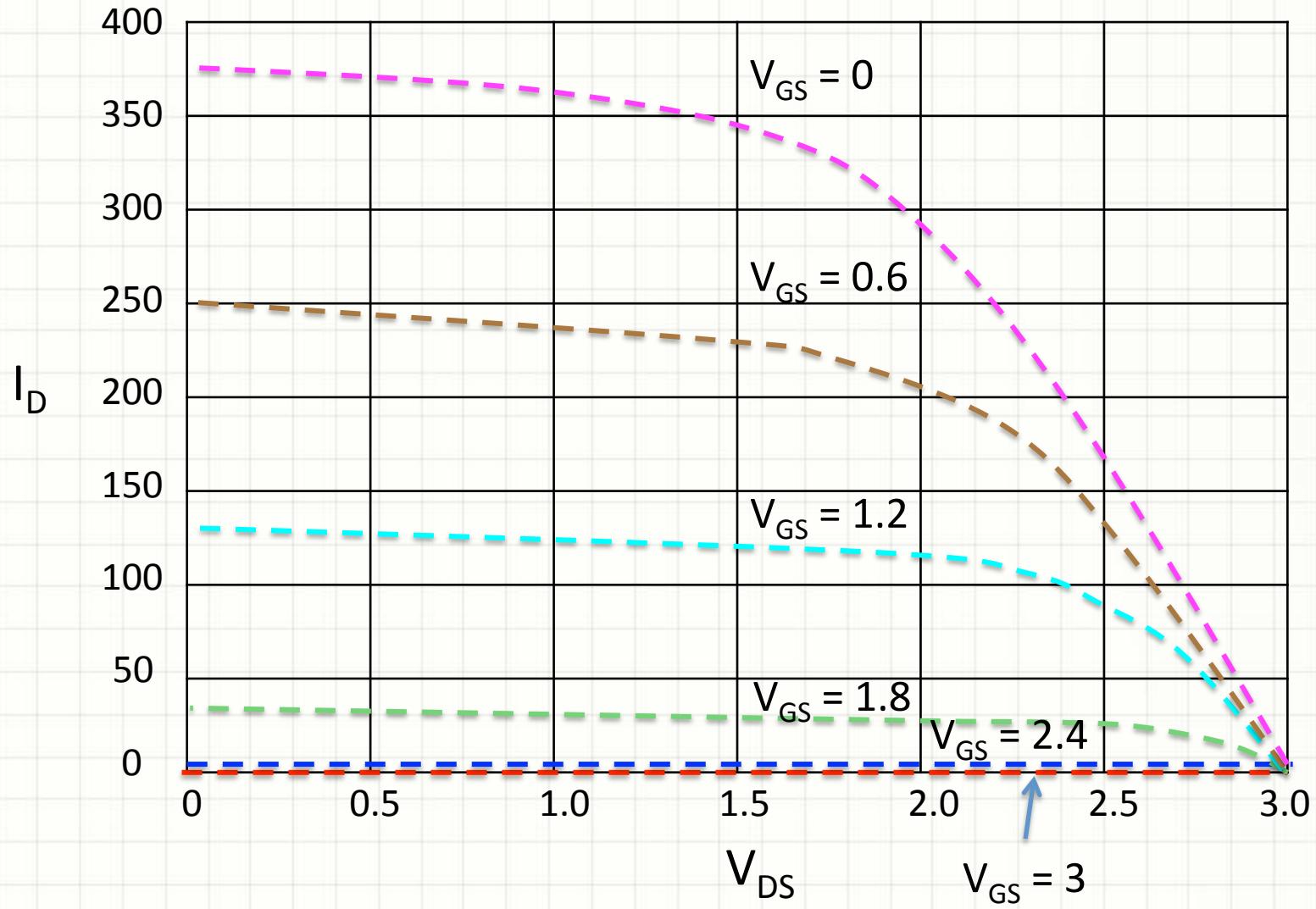
NMOS inverter, vary R, $V_{GS} = 2.4$ V



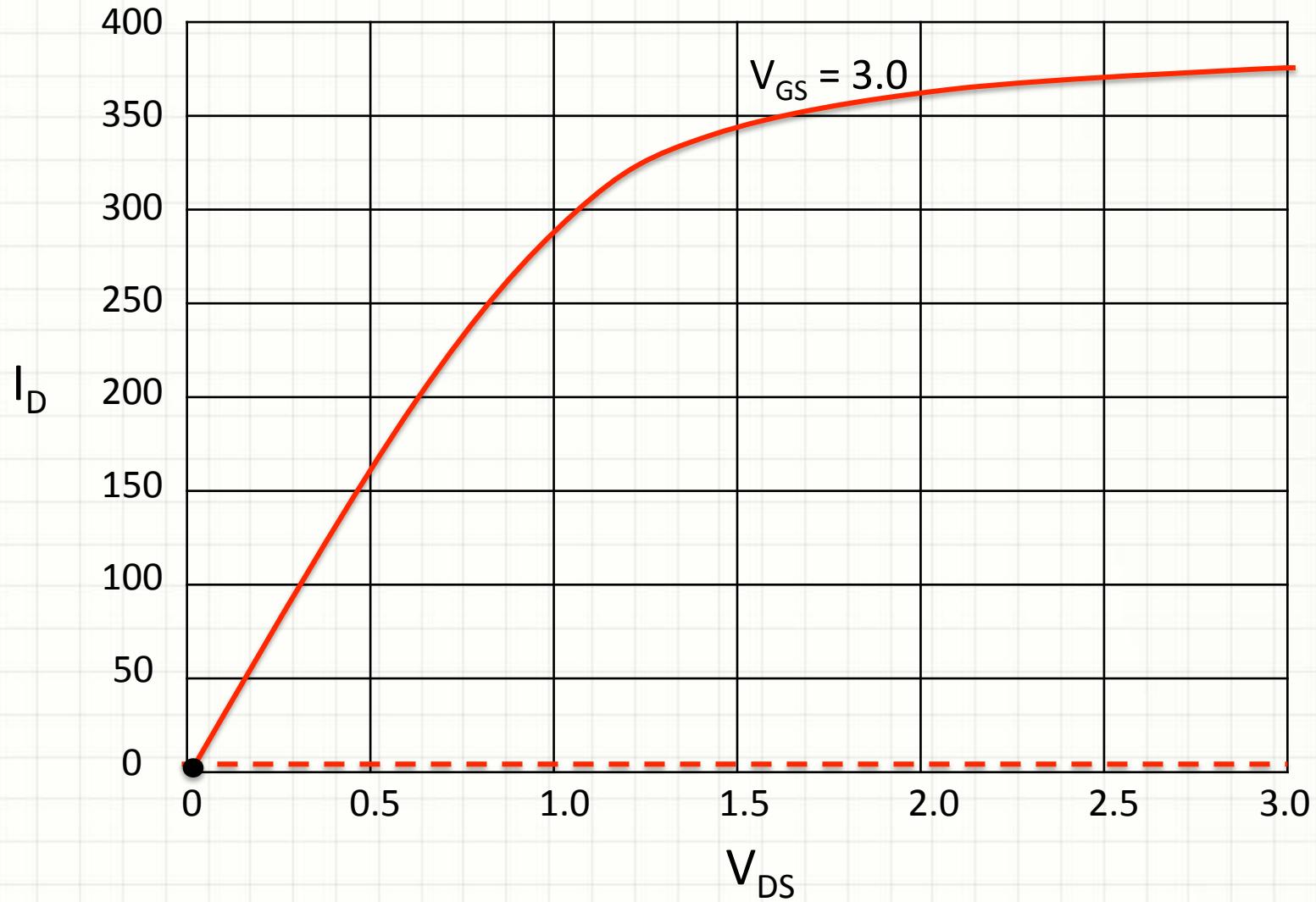
NMOS inverter, vary V_{GS}



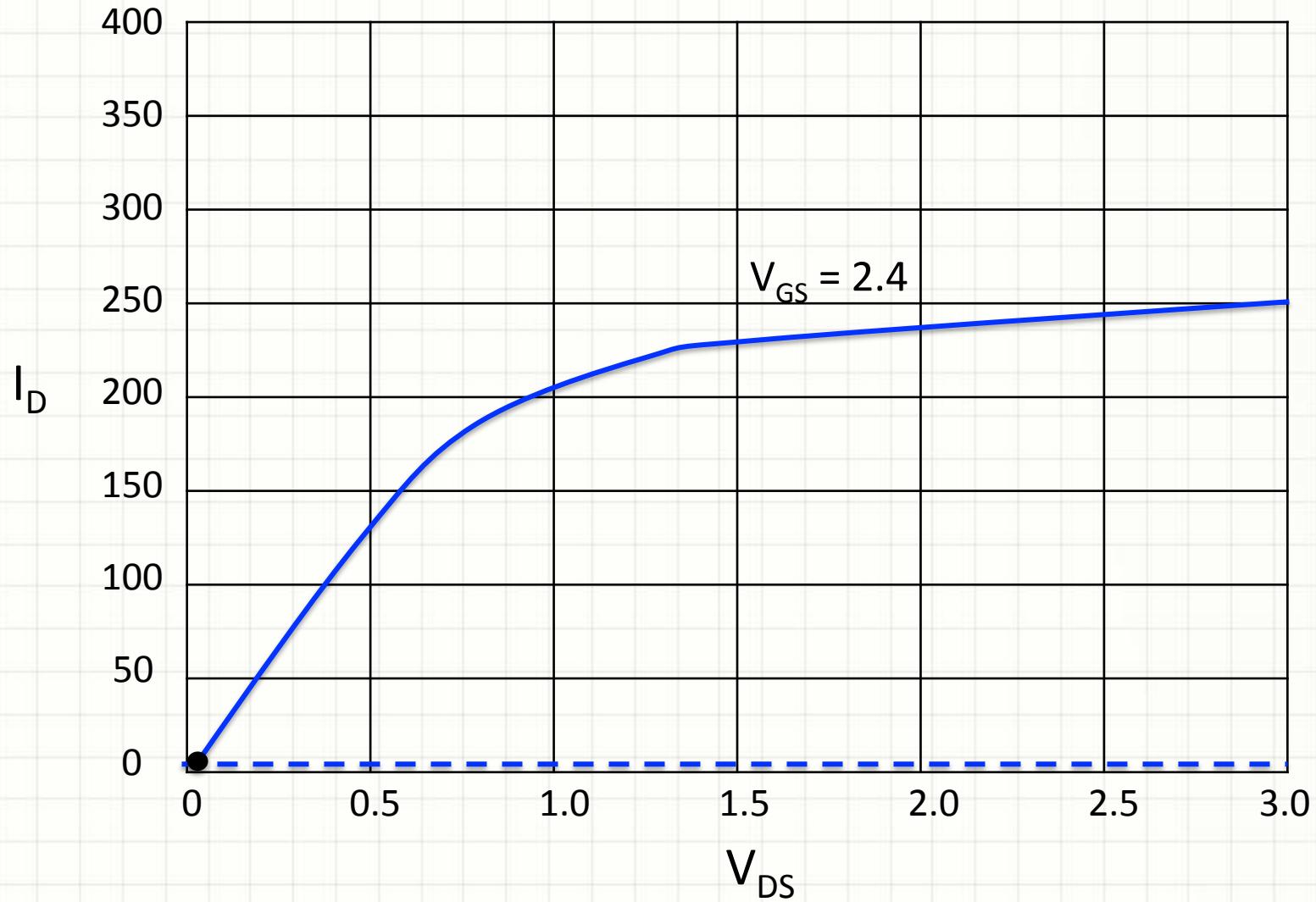
V-I for PMOS Transistor



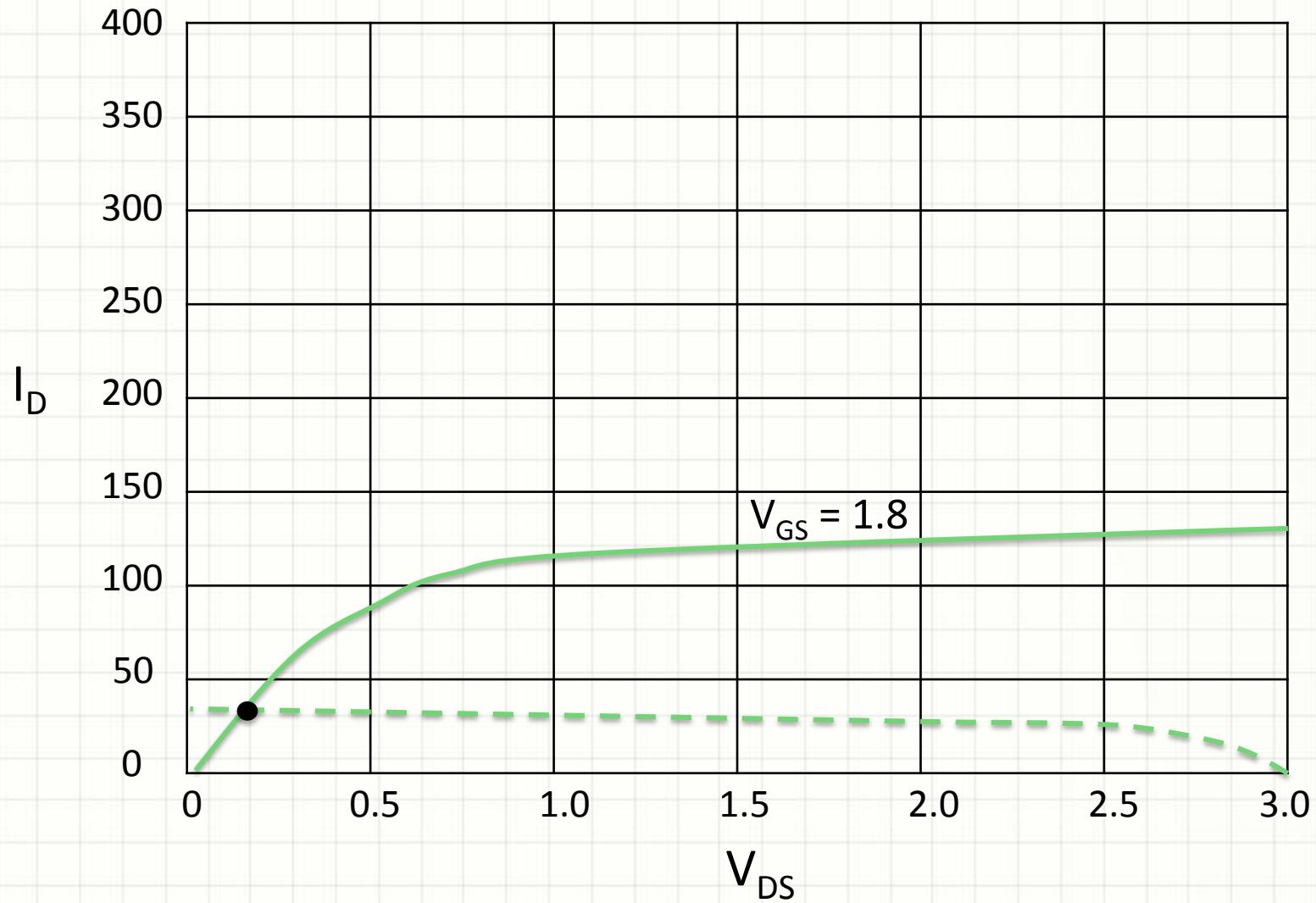
Output for CMOS Inverter



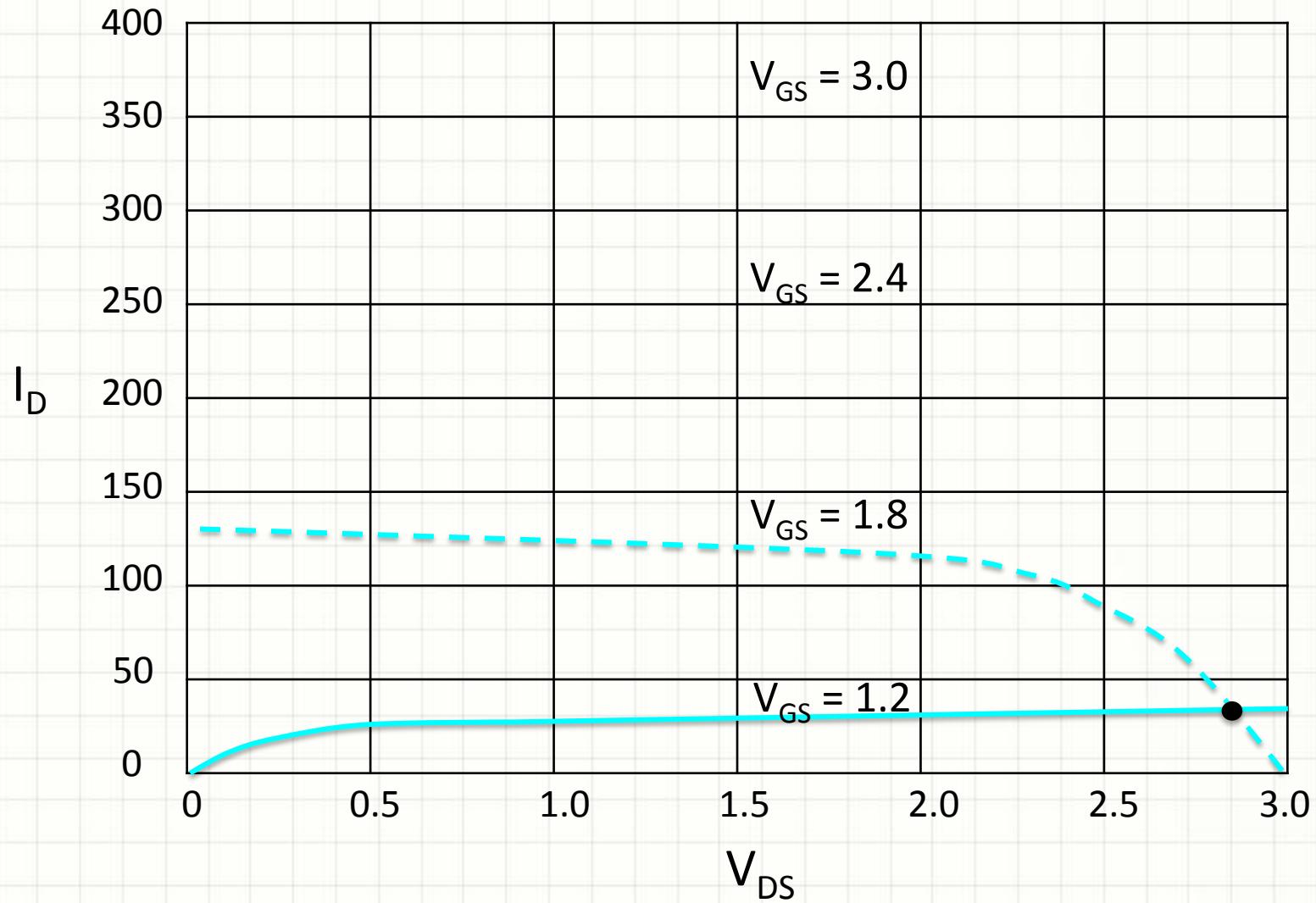
Output for CMOS Inverter



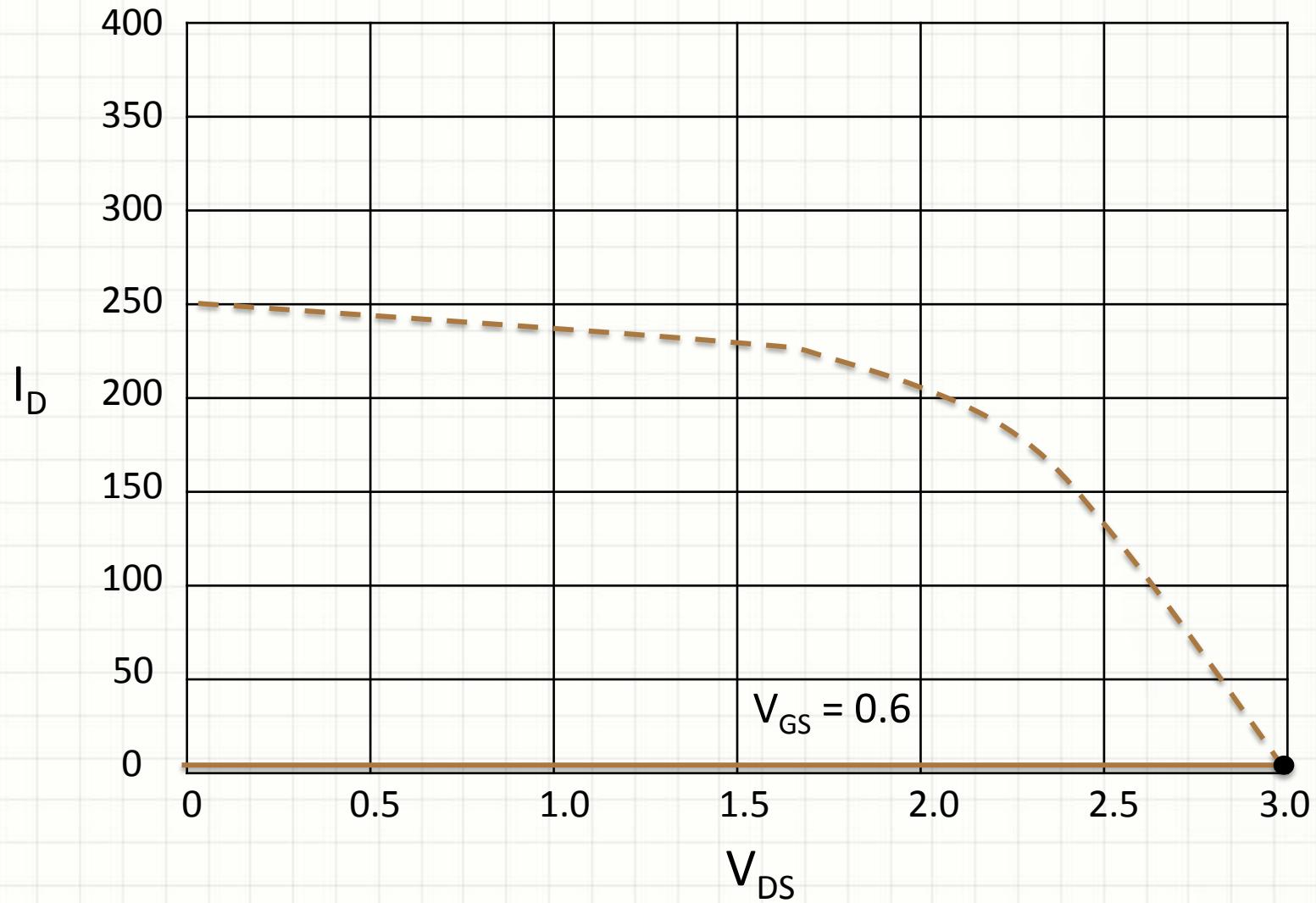
Output for CMOS Inverter



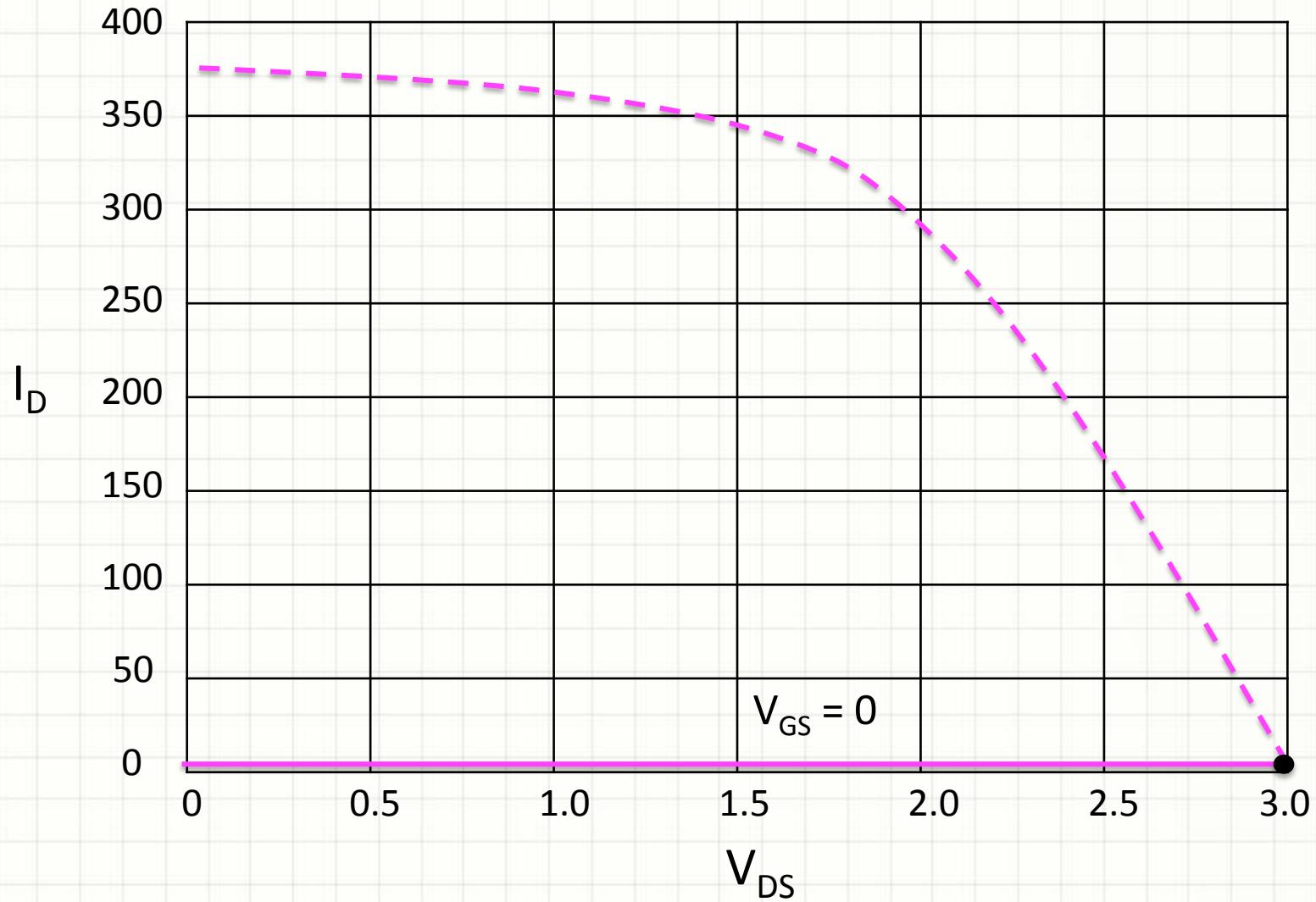
Output for CMOS Inverter



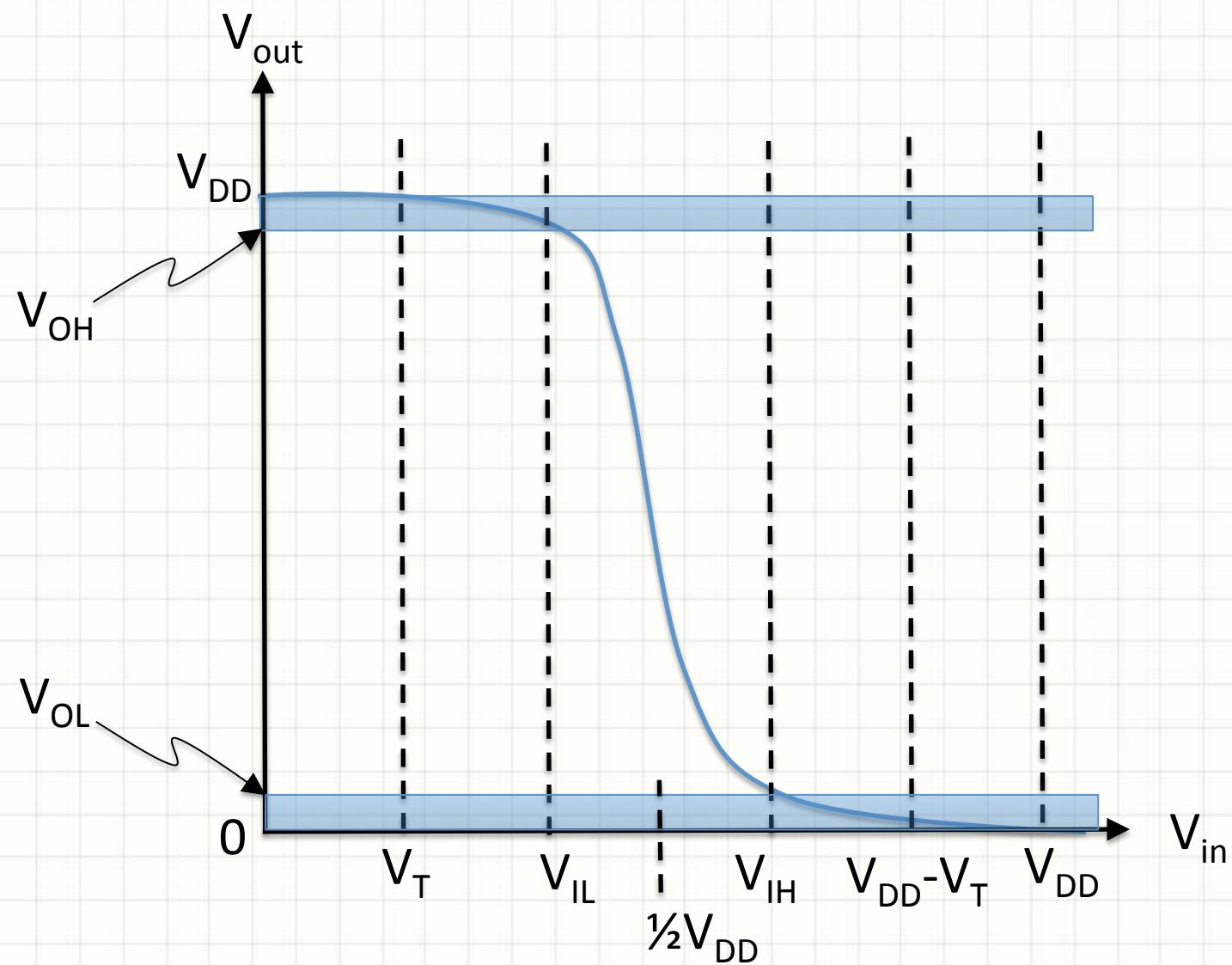
Output for CMOS Inverter



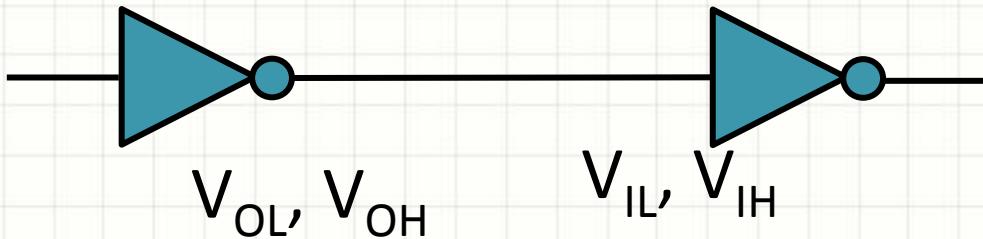
Output for CMOS Inverter



I/O characteristics of CMOS inverter



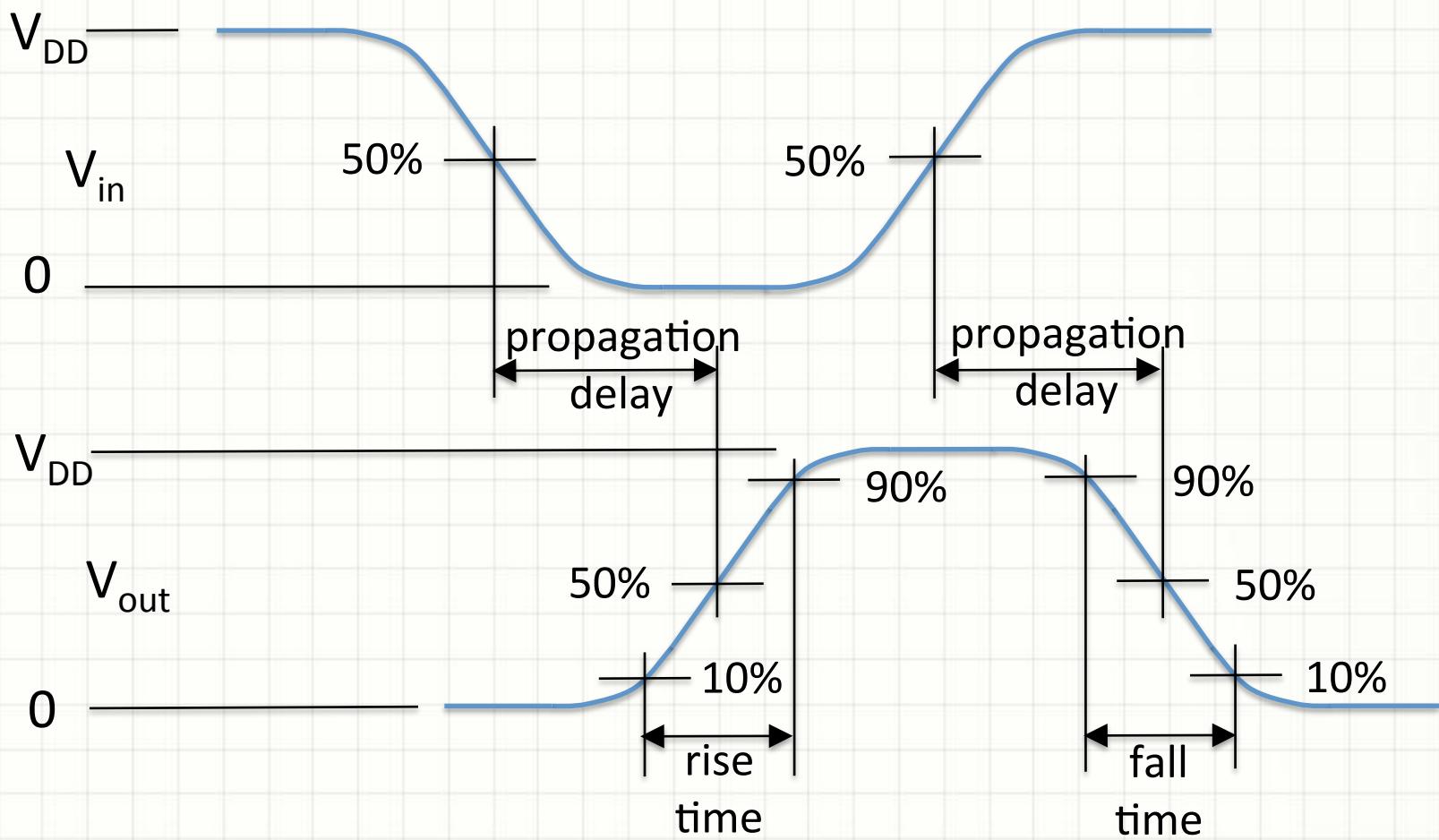
Noise Margin



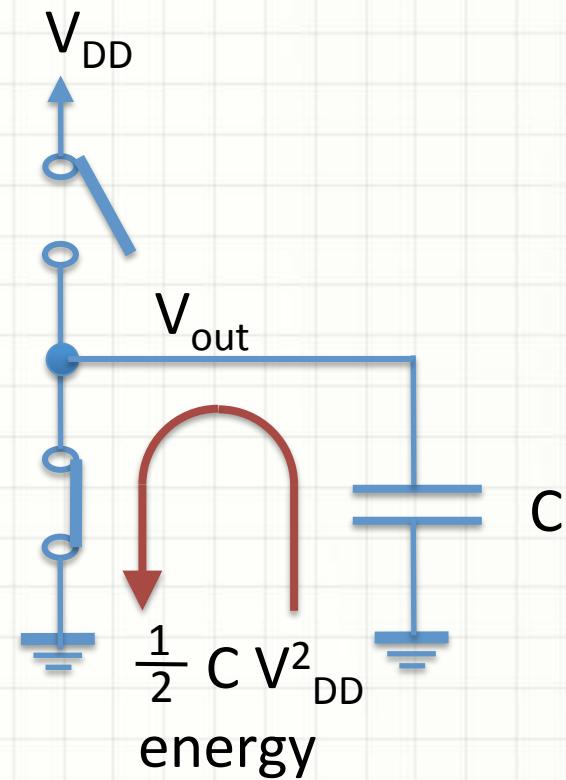
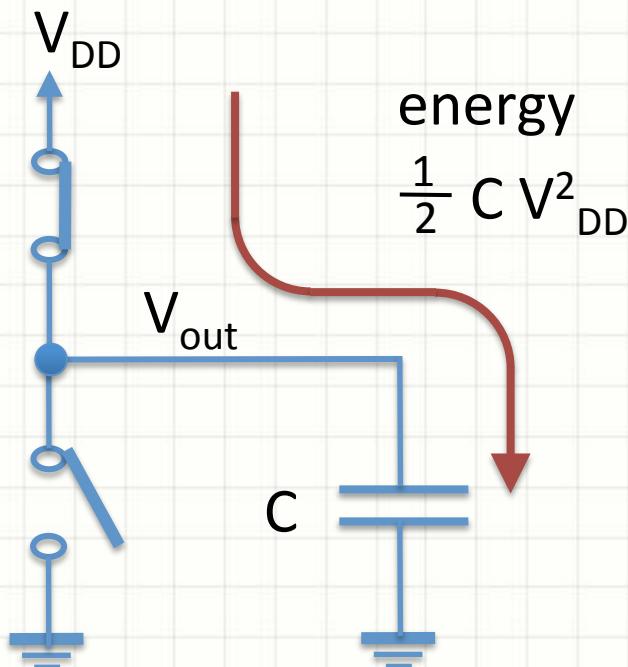
$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

Dynamic operation and delays

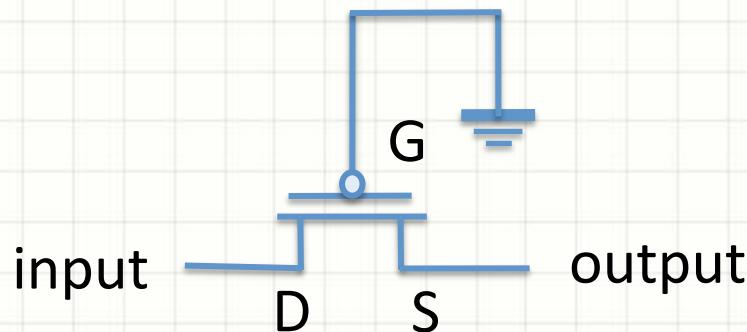
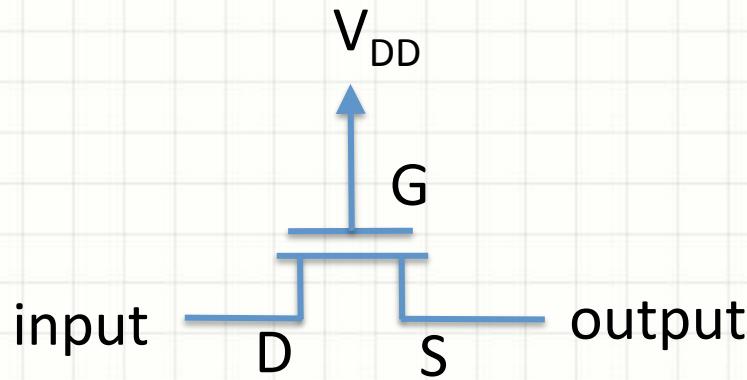


Power dissipation in CMOS inverter

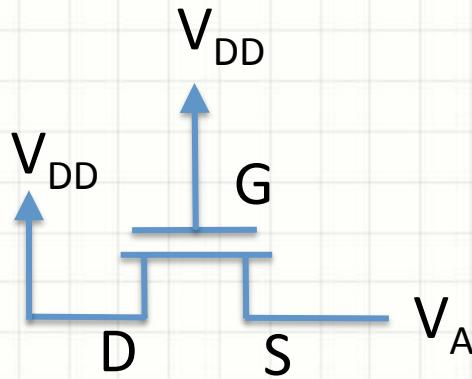


$$\text{power} = f C V^2_{DD}$$

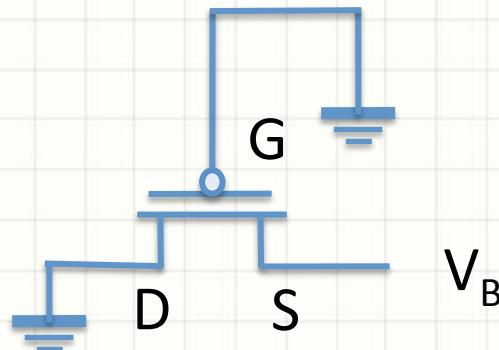
Using NMOS / PMOS transistors as switches



Passing 1's through NMOS switch Passing 0's through PMOS switch



$V_{GS} = V_{DD} - V_A$
Transistor cuts off if
 V_A rises above $V_{DD} - V_T$

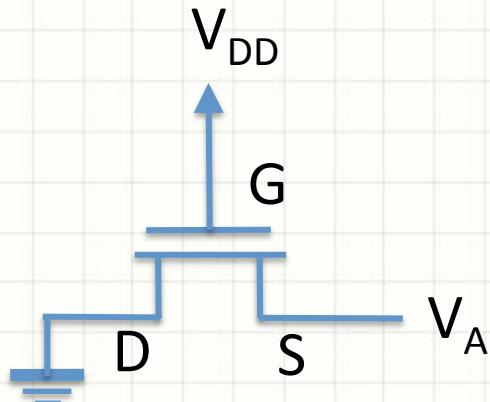


$V_{GS} = 0 - V_B$
Transistor cuts off if
 V_B falls below V_T

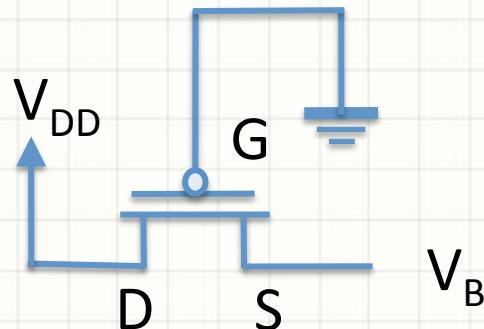


Passing 0's through NMOS switch

Passing 1's through PMOS switch

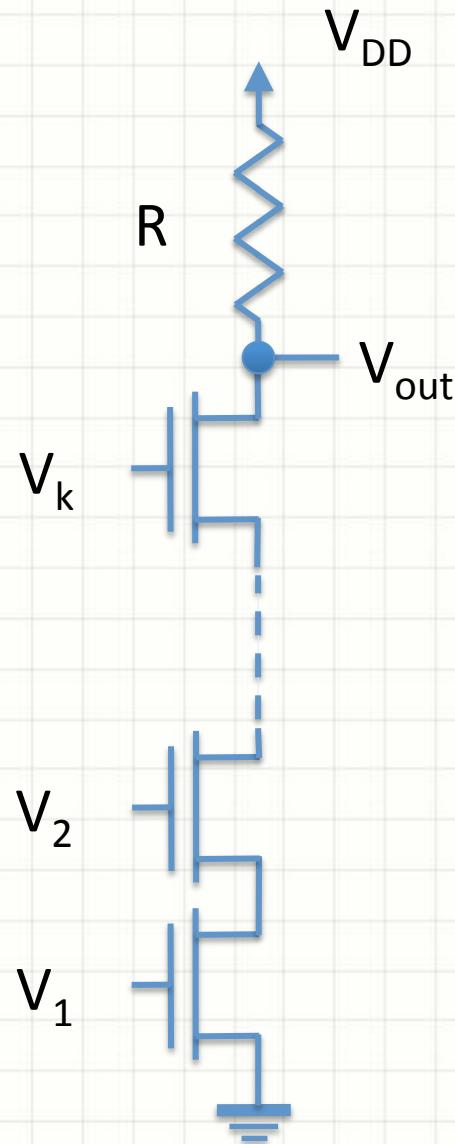


Transistor remains ON
 V_A is 0



Transistor remains ON
 V_B equals V_{DD}

Fan-in limitation



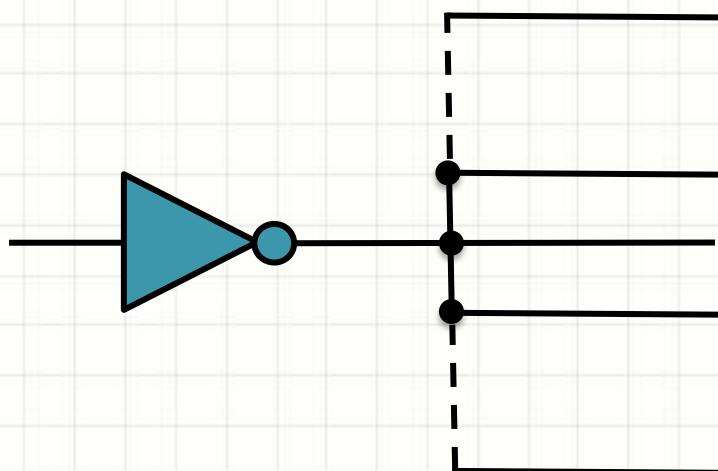
Effective channel length = $k \cdot L$

⇒ increased delay
increased V_{OL}

This limits the fan-in

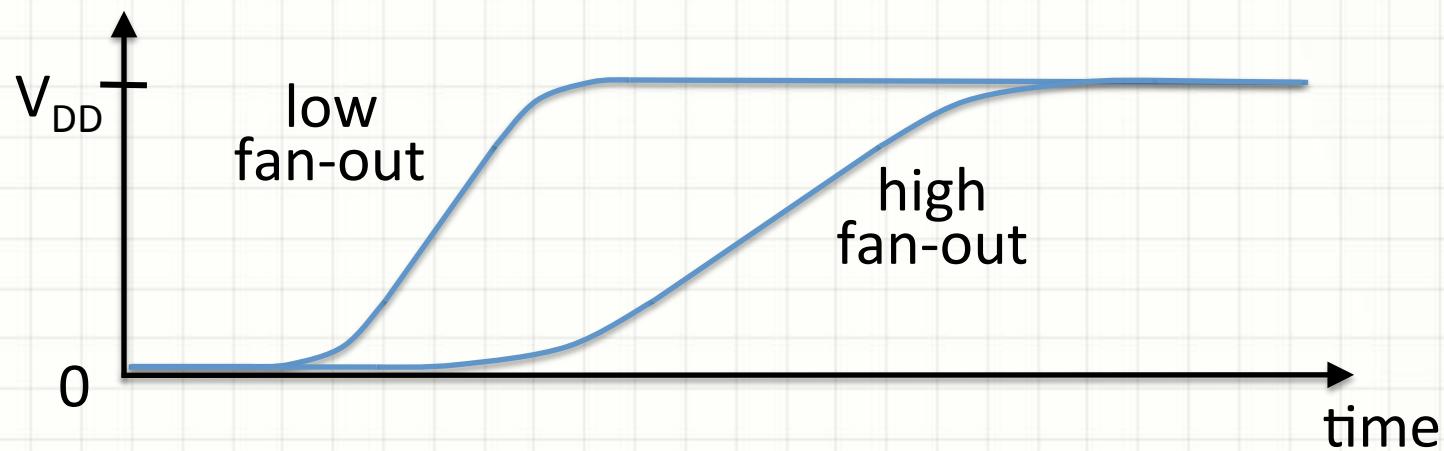
Higher fan-in in CMOS

Fan-out limitation



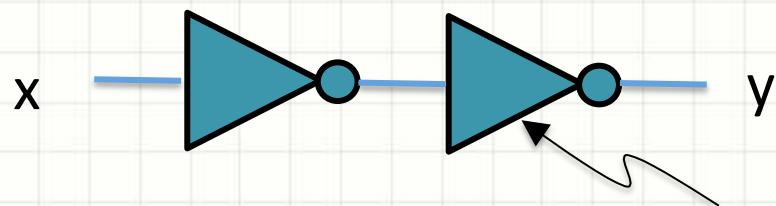
Increased load capacitance

⇒ increased delay
slower rise / fall

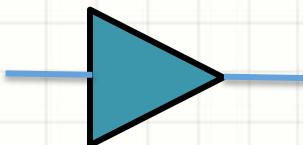


Simple buffer

$$y = x$$



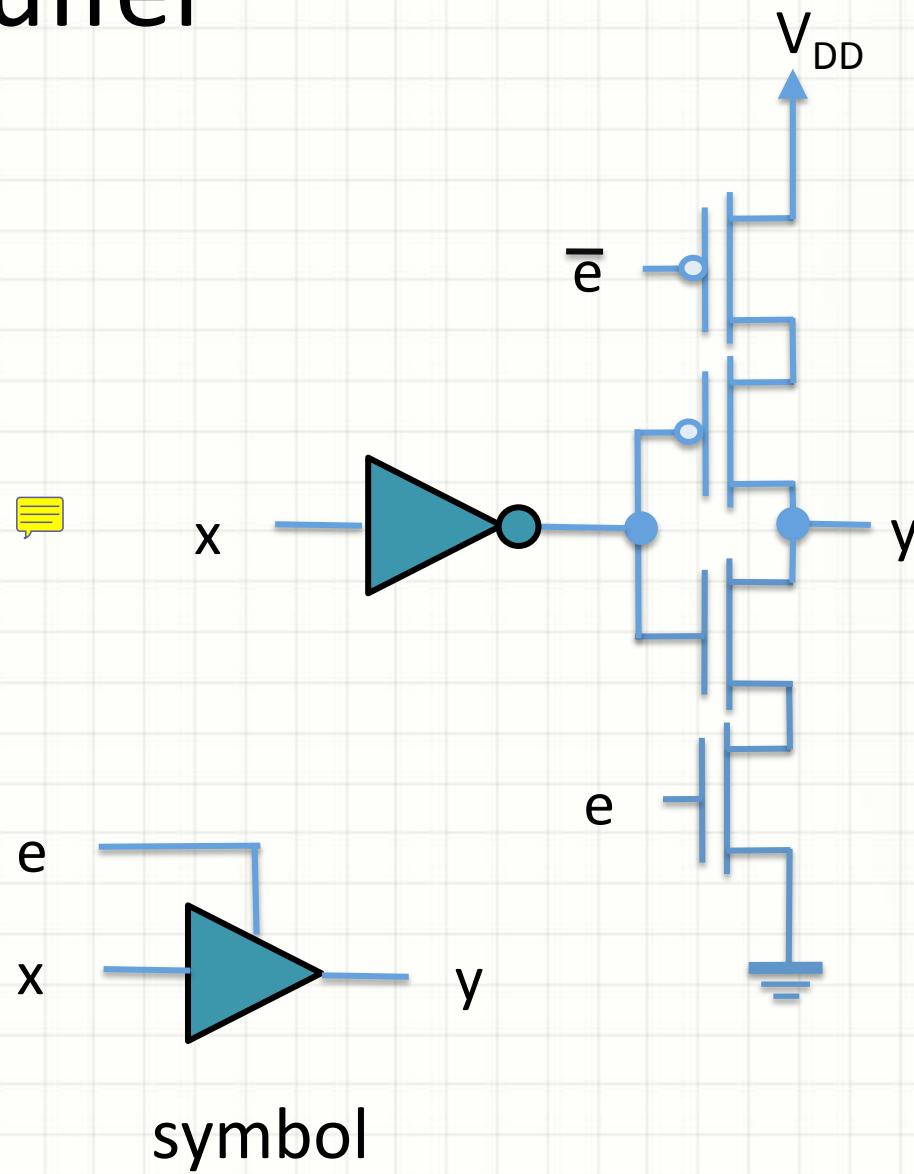
designed to drive
large loads

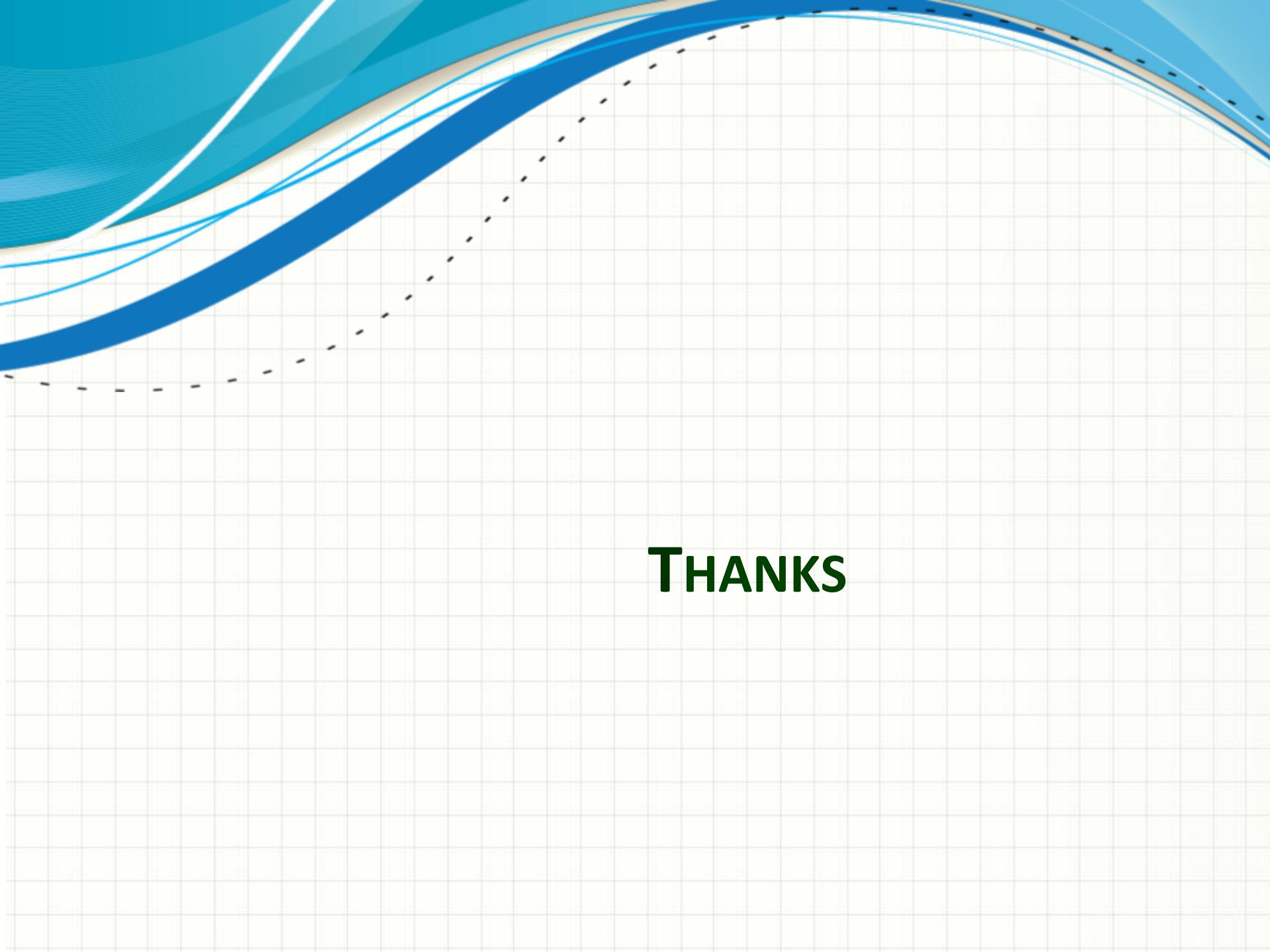


symbol

Tri-state buffer

e	x	y
0	0	Z
0	1	Z
1	0	0
1	1	1



The background features a white grid pattern. Overlaid on the top left is a stylized graphic element consisting of several curved bands in shades of blue and cyan. A prominent thick blue band curves from the bottom left towards the top right. A dashed black line follows a similar path, starting from the bottom left and curving upwards and to the right.

THANKS