# COL215 Digital Logic and System Design

Designing synchronous sequential circuits

23 August 2017

# Design problem

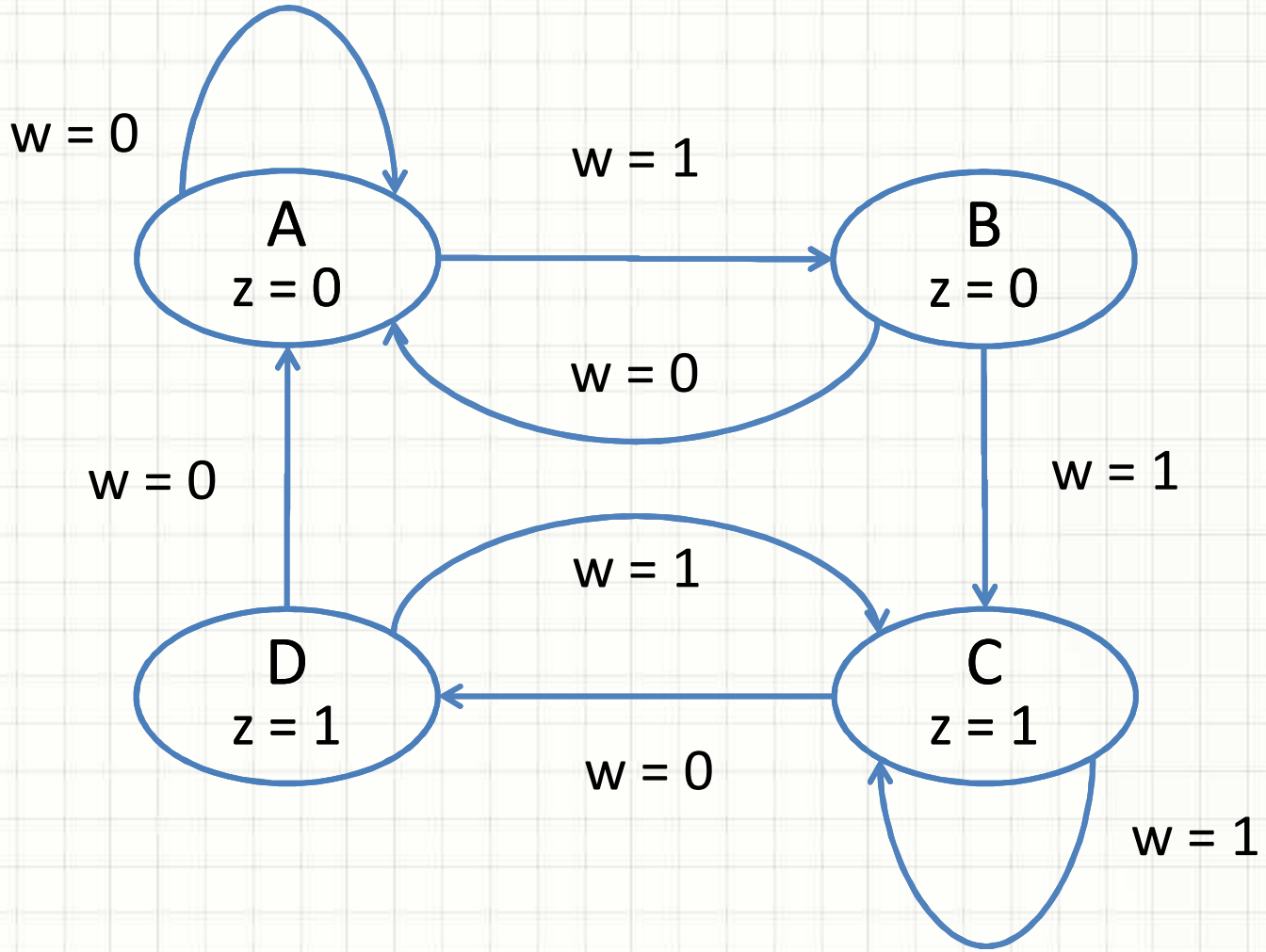
Design a synchronous circuit with the following specifications

- It has one input w and one output z
- Output z becomes 1, if during two immediately preceding clock cycles input w is 1
- Output z becomes 0, if during two immediately preceding clock cycles input w is 0
- Otherwise, output z remains unchanged
- Initially, output z is 0

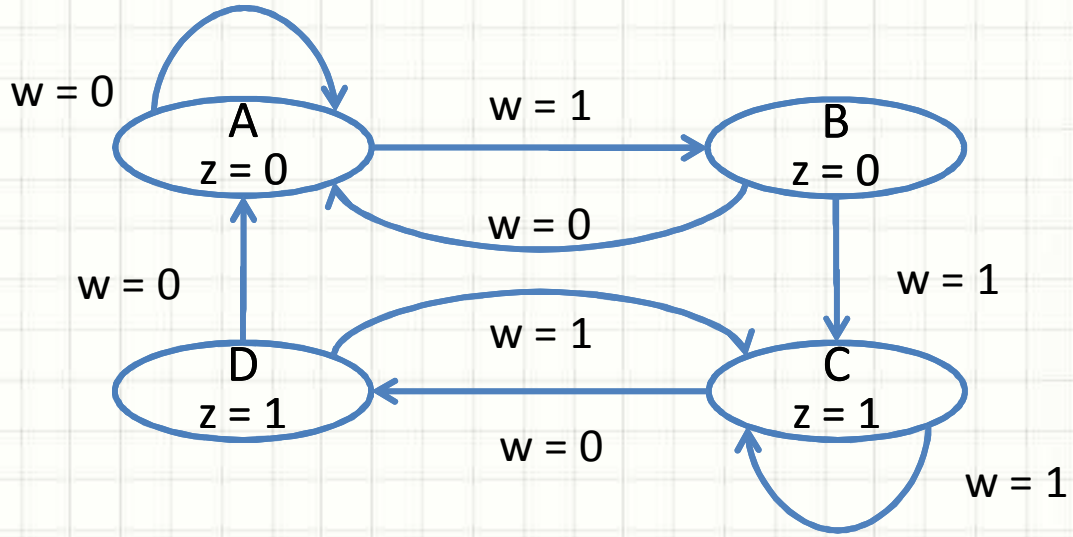
# How to design?

- Identify states
- A state indicates how the past input history influences the output
- When another input gets added to the history, state may change
- ‘States’ and ‘state transitions’ form ‘state transition diagram’

# State transition diagram

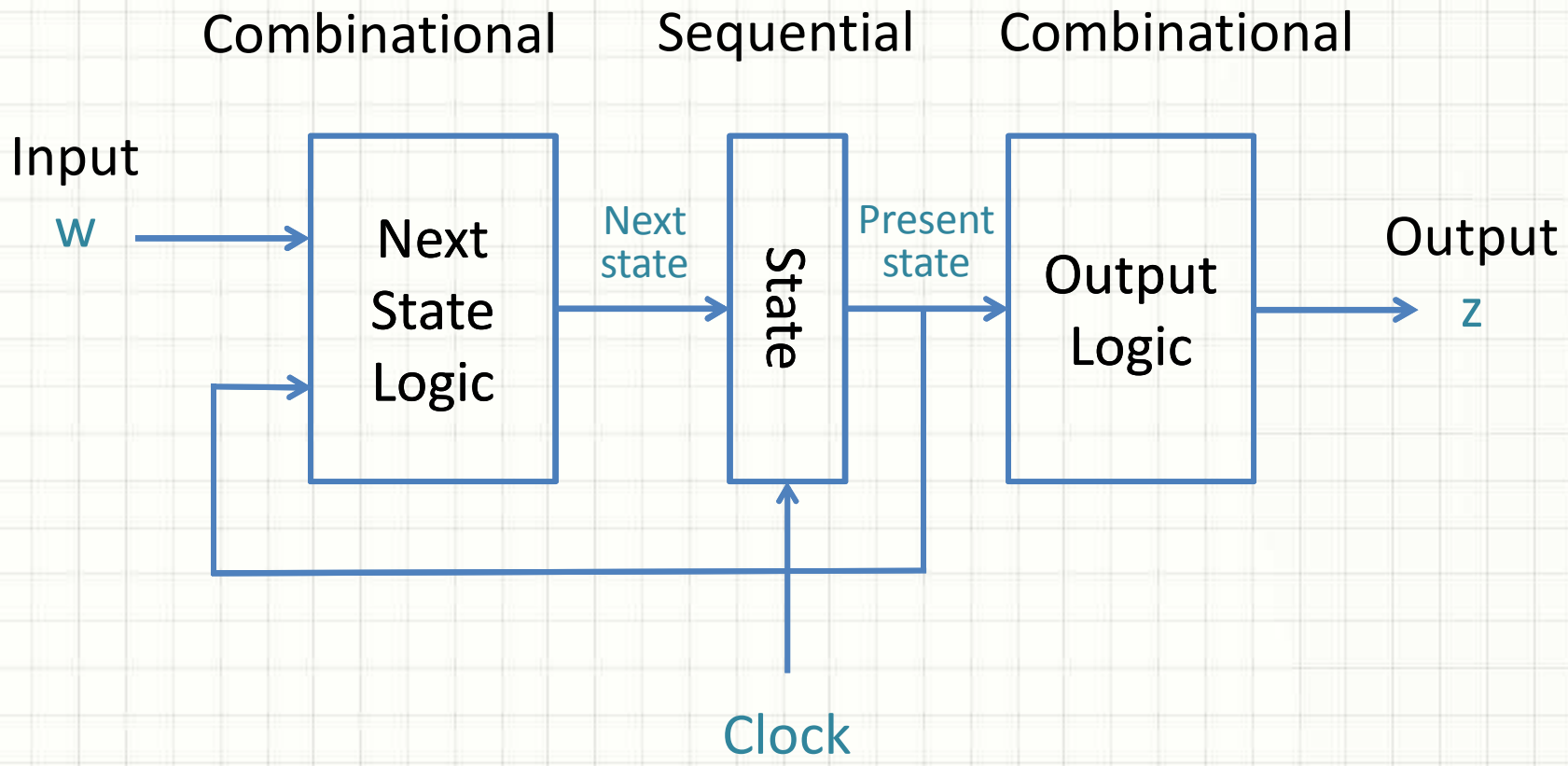


# State transition table




| Present state | Next state | | Output z |
|---|---|---|---|
| | w = 0 | w = 1 | |
| A | A | B | 0 |
| B | A | C | 0 |
| C | D | C | 1 |
| D | A | C | 1 |

# Circuit structure



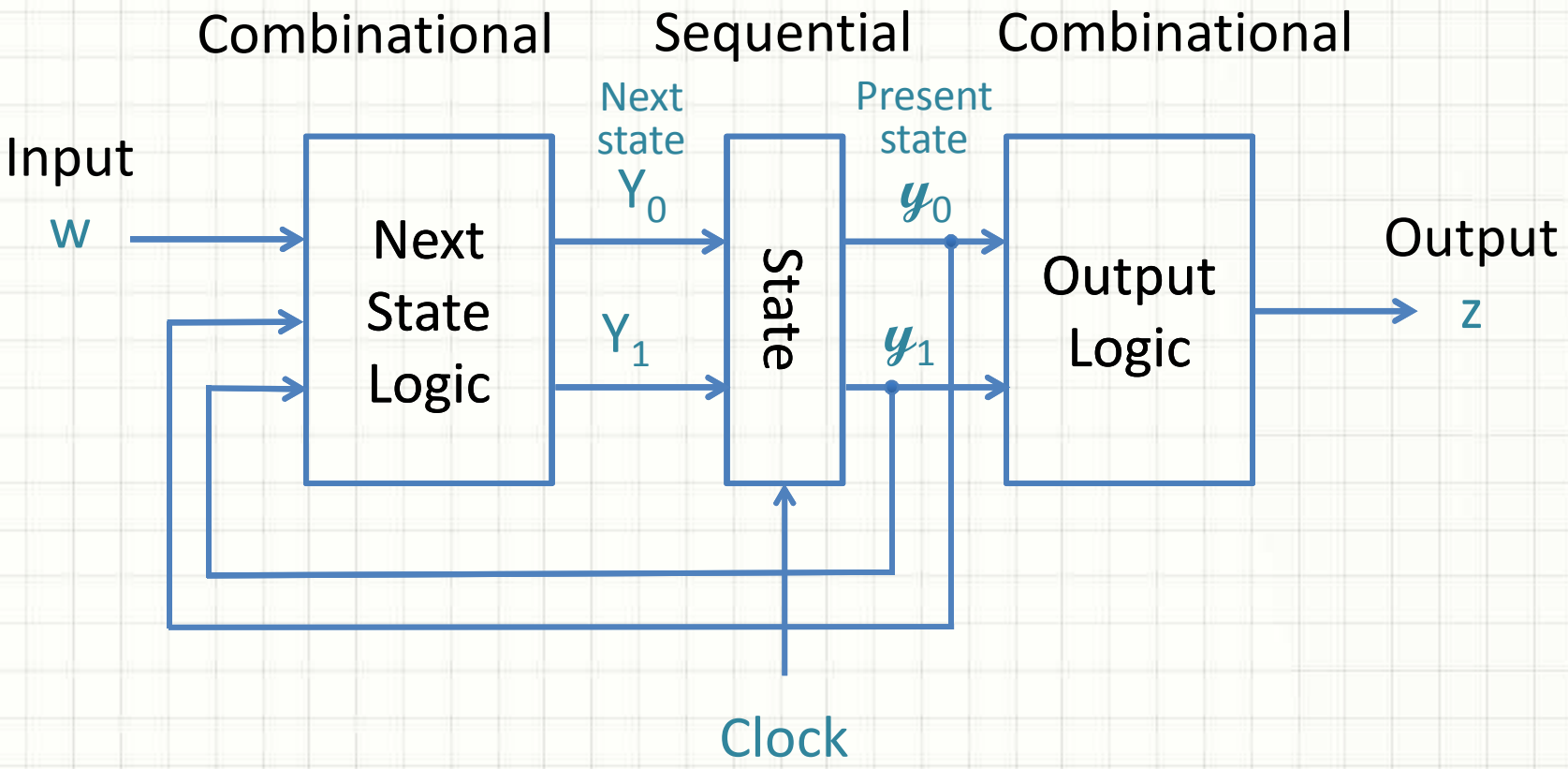
# Representing state

| | $y_1$ $y_0$ |
|---|---|
| A | 0 0 |
| B | 0 1 |
| C | 1 0 |
| D | 1 1 |

Present state: $y_1$ $y_0$

Next state: $Y_1$ $Y_0$

# Circuit structure



# State transition table

| $y_1\ y_0$ | $Y_1\ Y_0$ | | Output z |
|---|---|---|---|
| | w = 0 | w = 1 | |
| 0 0 | 0 0 | 0 1 | 0 |
| 0 1 | 0 0 | 1 0 | 0 |
| 1 0 | 1 1 | 1 0 | 1 |
| 1 1 | 0 0 | 1 0 | 1 |

# Karnaugh maps

| $y_1\ y_0$ | $Y_1\ Y_0$ | |
|---|---|---|
| | w = 0 | w = 1 |
| 0 0 | 0 0 | 0 1 |
| 0 1 | 0 0 | 1 0 |
| 1 0 | 1 1 | 1 0 |
| 1 1 | 0 0 | 1 0 |

| $y_1\ y_0$ | Output z |
|---|---|
| 0 0 | 0 |
| 0 1 | 0 |
| 1 0 | 1 |
| 1 1 | 1 |

# Karnaugh maps

| $y_1\ y_0$ | $Y_1\ Y_0$ | |
|---|---|---|
| | w = 0 | w = 1 |
| 0 0 | 0 0 | 0 1 |
| 0 1 | 0 0 | 1 0 |
| 1 1 | 0 0 | 1 0 |
| 1 0 | 1 1 | 1 0 |

| $y_1\ y_0$ | Output z |
|---|---|
| 0 0 | 0 |
| 0 1 | 0 |
| 1 1 | 1 |
| 1 0 | 1 |

# Karnaugh maps

$Y_1$

| $y_1\ y_0$ | w = 0 | w = 1 |
|---|---|---|
| 0 0 | 0 | 0 |
| 0 1 | 0 | 1 |
| 1 1 | 0 | 1 |
| 1 0 | 1 | 1 |

$Y_0$

| $y_1\ y_0$ | w = 0 | w = 1 |
|---|---|---|
| 0 0 | 0 | 1 |
| 0 1 | 0 | 0 |
| 1 1 | 0 | 0 |
| 1 0 | 1 | 0 |

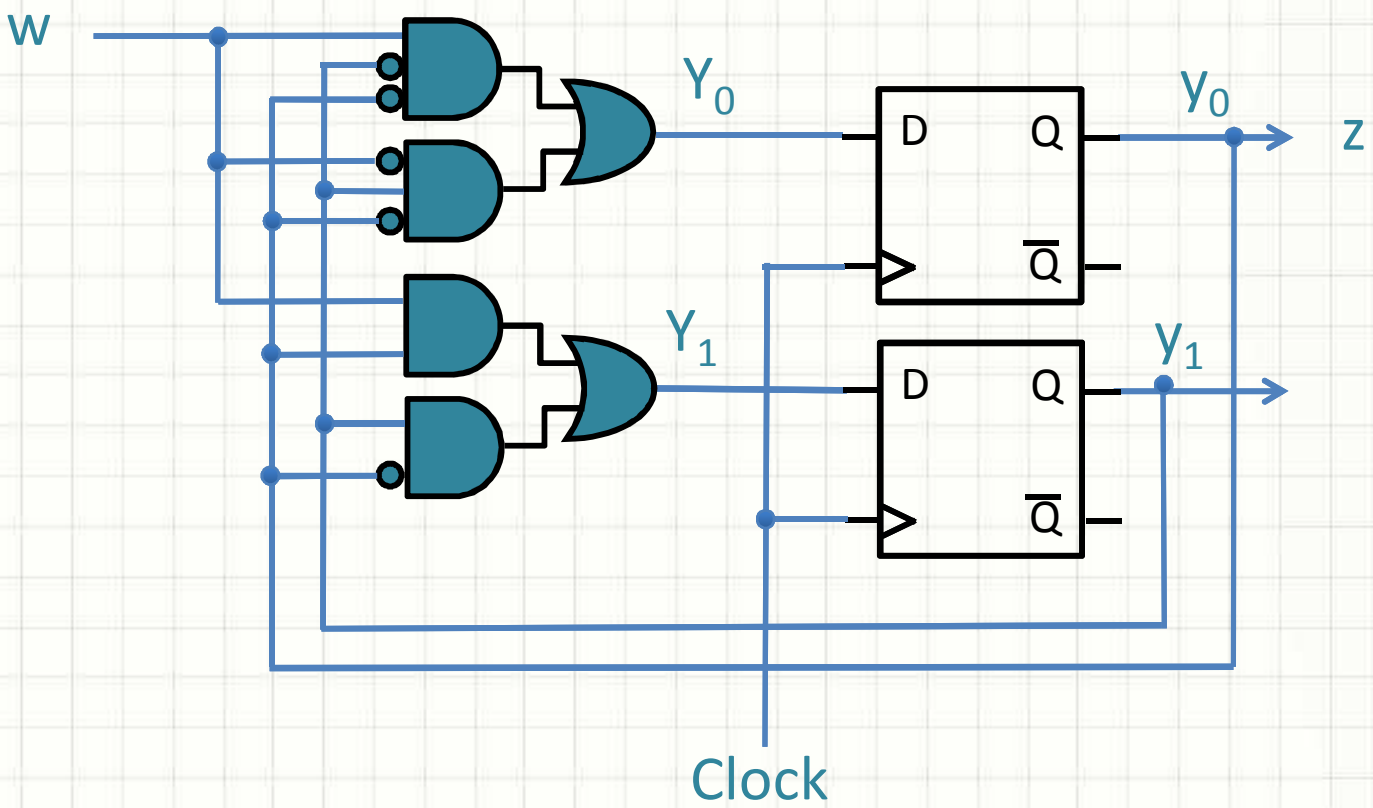
| $y_1\ y_0$ | Output z |
|---|---|
| 0 0 | 0 |
| 0 1 | 0 |
| 1 1 | 1 |
| 1 0 | 1 |

$Y_1 = w.y_0 + y_1.y_0'$

$Y_0 = w.y_1'.y_0' + w'.y_1.y_0'$
$= (w.y_1' + w'.y_1).y_0'$

$z = y_1$

# Complete circuit

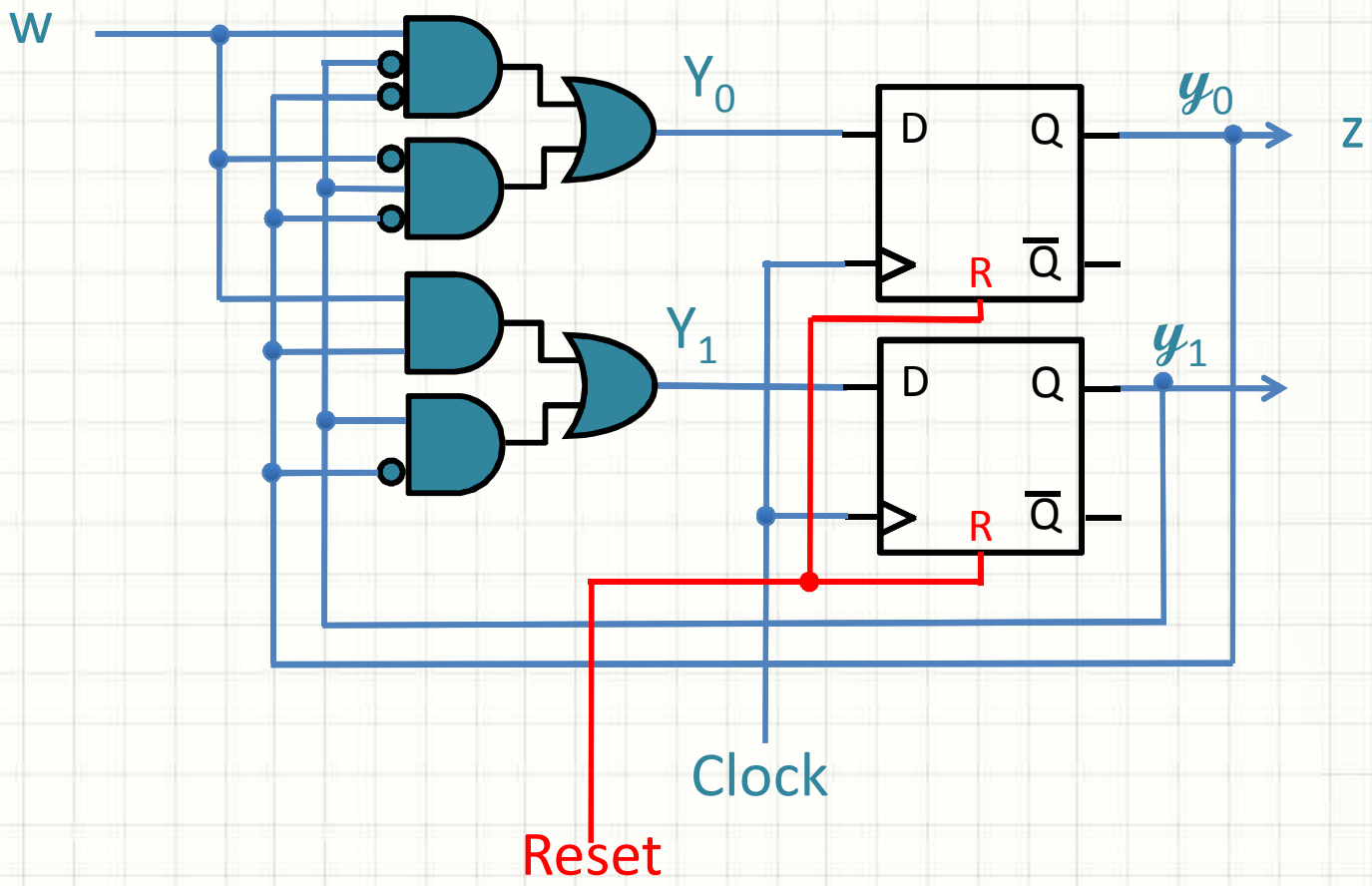



$Y_1 = w.y_0 + y_1.y_0'$

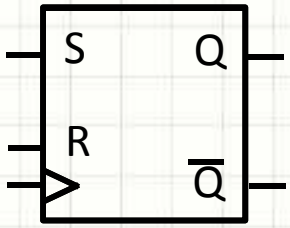
$Y_0 = w.y_1'.y_0' + w'.y_1.y_0'$
$= (w.y_1' + w'.y_1).y_0'$

$z = y_1$

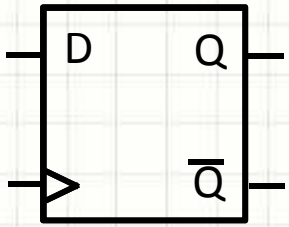
# Complete circuit



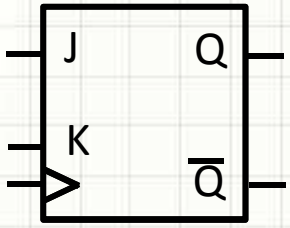
# Can we use J-K flip flops instead of D?




| S | R | Q(t+1) |
|---|---|---|
| 0 | 0 | Q (t) |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | XXX |




| D | Q(t+1) |
|---|---|
| 0 | 0 |
| 1 | 1 |




| J | K | Q(t+1) |
|---|---|---|
| 0 | 0 | Q (t) |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | $\overline{Q}$ (t) |

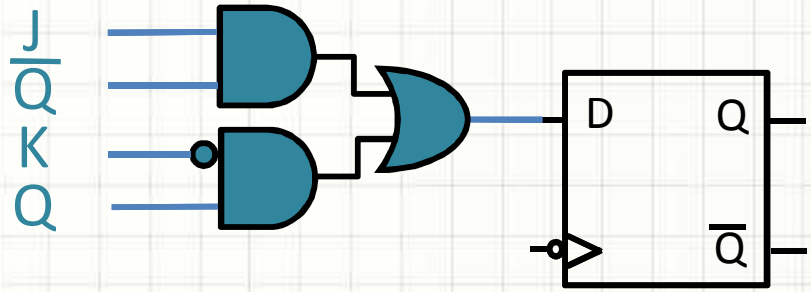
$D = J.\overline{Q} + \overline{K}.Q$

$S = J.\overline{Q}$, $R = K.Q$

# J-K flip flop made using D FF or SR FF

Implementing J-K FF using D FF

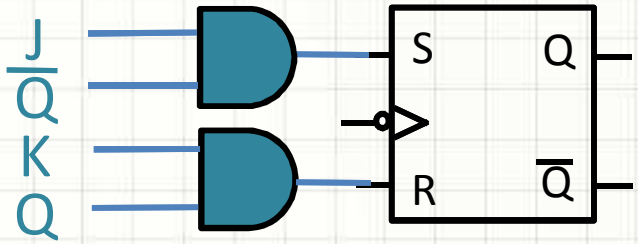
$$D = J \cdot \overline{Q} + \overline{K} \cdot Q$$




Implementing J-K FF using SR FF

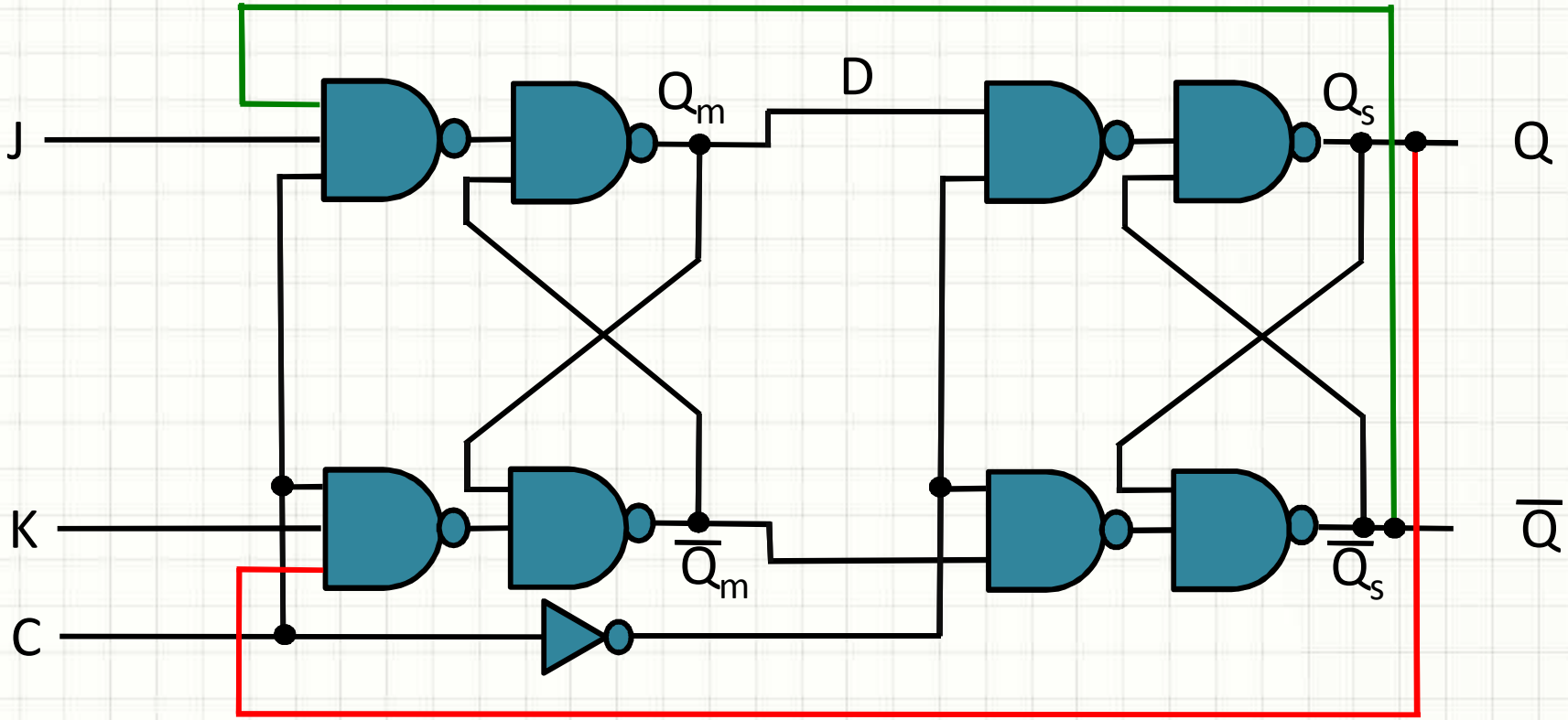
$$S = J \cdot \overline{Q}$$

$$R = K \cdot Q$$



# Direct implementation

Master-Slave J-K Flip-Flop



# Defining J and K inputs

| J | K | Q (t + 1) |
|---|---|---|
| 0 | 0 | Q (t) |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | $\overline{Q}$ (t) |

| Transition | J K |
|---|---|
| 0 => 0 | 0 - |
| 0 => 1 | 1 - |
| 1 => 0 | - 1 |
| 1 => 1 | - 0 |

Task: verify that these two tables are consistent with each other

# Transitions for the current example

$Y_1$

| $y_1\ y_0$ | w = 0 | w = 1 |
|---|---|---|
| 0 0 | 0 (0=>0) | 0 (0=>0) |
| 0 1 | 0 (0=>0) | 1 (0=>1) |
| 1 1 | 0 (1=>0) | 1 (1=>1) |
| 1 0 | 1 (1=>1) | 1 (1=>1) |

$Y_0$

| $y_1\ y_0$ | w = 0 | w = 1 |
|---|---|---|
| 0 0 | 0 (0=>0) | 1 (0=>1) |
| 0 1 | 0 (1=>0) | 0 (1=>0) |
| 1 1 | 0 (1=>0) | 0 (1=>0) |
| 1 0 | 1 (0=>1) | 0 (0=>0) |

These tables are same as those in slide 11 with transitions shown in green

# J K inputs for the current example

J, K values for the required transitions are taken from the table on right and added to the tables below (shown in red)

| Transition | J K |
|---|---|
| 0 => 0 | 0 - |
| 0 => 1 | 1 - |
| 1 => 0 | - 1 |
| 1 => 1 | - 0 |

$J_1$ $K_1$

| $y_1$ $y_0$ | w = 0 | w = 1 |
|---|---|---|
| 0 0 | (0=>0) 0 - | (0=>0) 0 - |
| 0 1 | (0=>0) 0 - | (0=>1) 1 - |
| 1 1 | (1=>0) - 1 | (1=>1) - 0 |
| 1 0 | (1=>1) - 0 | (1=>1) - 0 |

$J_0$ $K_0$

| $y_1$ $y_0$ | w = 0 | w = 1 |
|---|---|---|
| 0 0 | (0=>0) 0 - | (0=>1) 1 - |
| 0 1 | (1=>0) - 1 | (1=>0) - 1 |
| 1 1 | (1=>0) - 1 | (1=>0) - 1 |
| 1 0 | (0=>1) 1 - | (0=>0) 0 - |

# Separating J and K values

$J_1$

| $y_1\ y_0$ | w' | w |
|---|---|---|
| 0 0 | 0 | 0 |
| 0 1 | 0 | 1 |
| 1 1 | - | - |
| 1 0 | - | - |

$K_1$

| $y_1\ y_0$ | w' | w |
|---|---|---|
| 0 0 | - | - |
| 0 1 | - | - |
| 1 1 | 1 | 0 |
| 1 0 | 0 | 0 |

$J_0$

| $y_1\ y_0$ | w' | w |
|---|---|---|
| 0 0 | 0 | 1 |
| 0 1 | - | - |
| 1 1 | - | - |
| 1 0 | 1 | 0 |

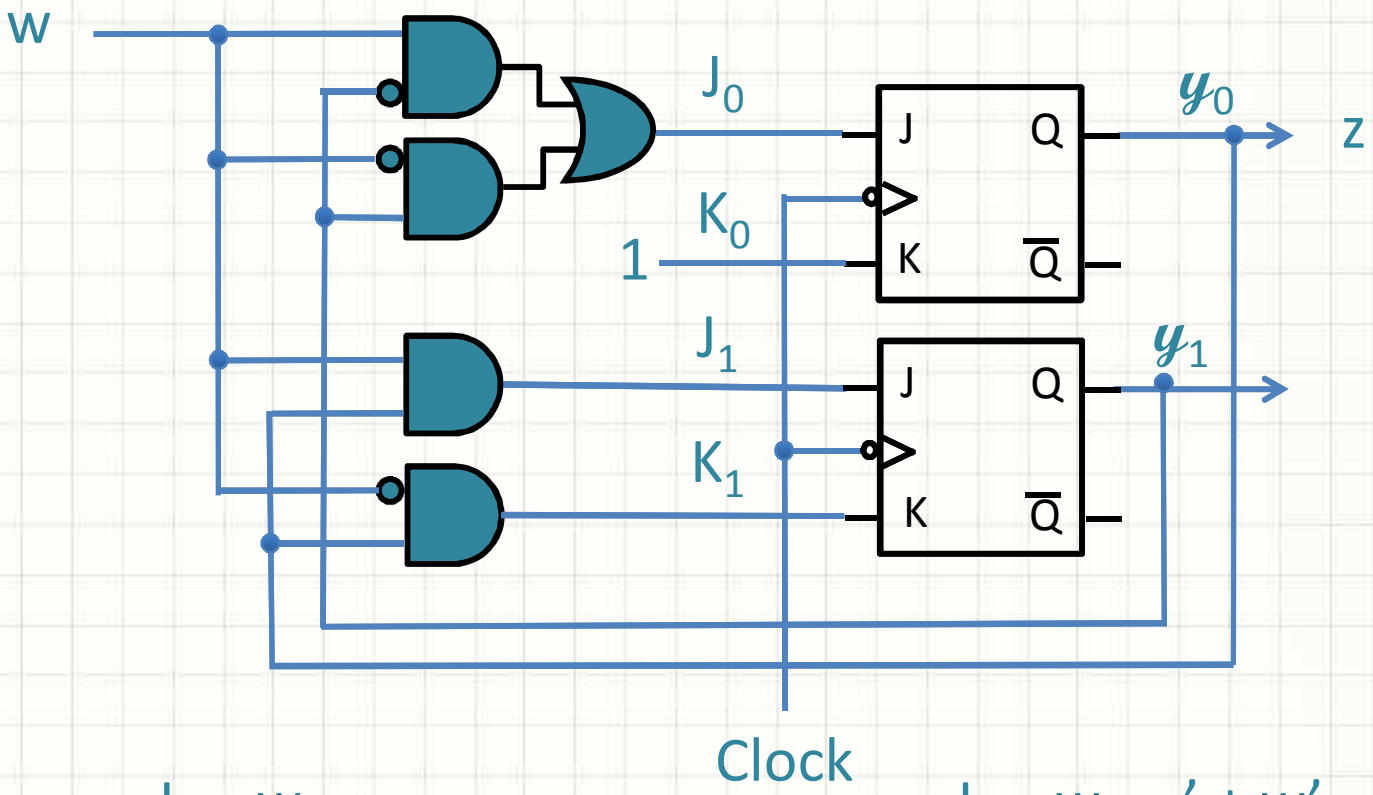
$K_0$

| $y_1\ y_0$ | w' | w |
|---|---|---|
| 0 0 | - | - |
| 0 1 | 1 | 1 |
| 1 1 | 1 | 1 |
| 1 0 | - | - |

$J_1 = w.\ y_0$
$K_1 = w'.\ y_0$

$J_0 = w.\ y_1' + w'.\ y_1$
$K_0 = 1$

# Final circuit




$J_1 = w.\, y_0$
$K_1 = w'.\, y_0$

$J_0 = w.\, y_1' + w'.\, y_1$
$K_0 = 1$

# THANKS