

Audio Amplifier Design

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Abstract—Electrical signals that are processed in systems cannot drive a speaker. They have a very small amplitude and cannot provide the required power to an output load. The Audio Amplifier is a widely used circuit to boost electrical signals and drive speakers, which convert these electrical signals into audio signals that we perceive. It consists of four stages - a pre-amplifier, a gain stage, a filter, and a power amplifier. This document discusses in detail the design of each of the components and provides the simulation and circuit results of an audio amplifier circuit.

I. INTRODUCTION

An audio amplifier is found in every circuit that produces an output through a speaker. The input signal to the circuit is often very small (10mV - 20mV pk-pk) and can easily be corrupted by noise. We amplify this signal in two stages. The first stage, a pre-amplifier which is a differential amplifier, focuses on noise removal primarily and provides a gain to the circuit. The second stage is the gain stage, which is a CE Amplifier, which provides the desired gain. The reason we have used two stages is to have the benefit of noise reduction in the first stage so that we obtain a relatively cleaner signal to work with. The amplified signal is now passed through a band pass filter to remove any frequencies that are not perceivable to humans, i.e., frequencies outside 20 Hz - 20 kHz. The last stage is a power amplifier which primarily provides enough power in the signal to drive a suitable load. The load speaker is connected to the output of the power amplifier. The constraints for the design are given below.

TABLE I: Constraints for design

Constraint	Value
Input Swing	10mV - 20mV
Rails	$\pm 5V$
Gain	≈ 500

It is impossible to obtain a gain of 500 for an input signal of 20mV pk-pk if the rails are $\pm 5V$. We have designed the circuit to get as high a gain as possible. Sections II, III, IV and V detail the design of each of the stages specified above in order. Section VI shows the circuit in simulation and hardware. A table with the values of the components is listed in both. For all the stages, we must ensure that the input impedance is high and the output impedance is low to ensure that no loading occurs. Section VII concludes with all the performance metrics

and figures of merit for the designed circuit. The chapter also discusses further improvements that can be made to improve the performance of the circuit.

II. PRE-AMPLIFIER

The pre-amplifier performs an essential function apart from providing an amplification, the removal of noise. It is characterized by **CMRR**, Common Mode Rejection Ratio. We have a differential amplifier which has two inputs and one output. The output signal of the differential amplifier is proportional to the difference in the input signals. This characteristic makes it useful to remove the presence of any unwanted signal components in both input signals.

The pre-amp stage is required for initial amplification. An ideal preamp will be linear (have a constant gain through its operating range), have high input impedance (requiring only a minimal amount of current to sense the input signal) and a low output impedance (when current is drawn from the output there is minimal change in the output voltage). It is used to boost the signal strength to drive the cable to the main power amplifier without significantly degrading the signal-to-noise ratio (SNR). If the noise performance of a pre-amp is bad, the already weak signal (could be completely overpowered by noise. In summation, the pre-amps main purpose is to provide initial amplification to the signal to send it to the gain stage, while also preventing noise from entering the system.

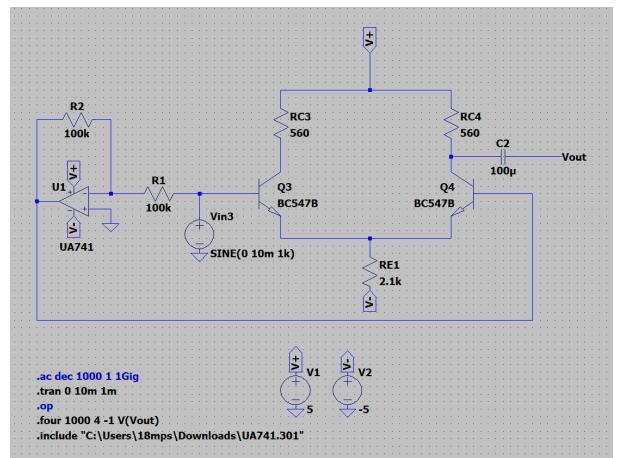


Fig. 1: The circuit of a differential amplifier

Let us quickly go through the gain expression derivation of the circuit to develop an intuitive understanding for the input signal selection.

The desired characteristic, as we will soon see in the derivation, is achieved when the currents in both the branches are equal. When $R_{C_1} = R_{C_2}$, owing to the symmetric nature of the configuration, the currents through R_{C_1} and R_{C_2} are equal. We assume that the BJTs are identical. Same current through the BJTs implies that the value of g_m , r_π is same. We proceed with the small signal analysis of the differential amplifier.

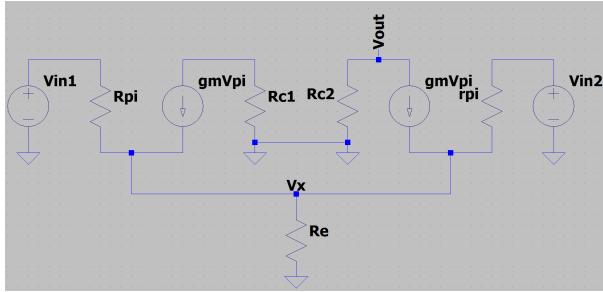


Fig. 2: Small Signal Model of a differential amplifier

Writing the nodal equation at the node voltage V_x , we get the following expression.

$$V_x = \frac{(V_{in_1} + V_{in_2})(g_m r_\pi + 1)}{2(g_m r_\pi + 1) + \frac{r_\pi}{R_E}}$$

Using the I-V relation for R_{C_2} , we obtain an expression for V_{out} .

$$V_{out} = R_{C_2} g_m (V_x - V_{in_2})$$

We make the approximation that $R_E \gg r_\pi$ and solve for V_{out} using these expressions. Thus, the final gain expression is

$$V_{out} = \frac{g_m R_{C_2} (V_{in_1} - V_{in_2})}{2}$$

The input and output impedances are given below.

$$R_{in} = \frac{3}{2} r_\pi, \quad R_{out} = R_{C_2}$$

We must also ensure that the transistors are biased properly in the forward active region.

$$V_{BE} > 0 \rightarrow V_+ > 2I_C R_E$$

$$V_{CE} > V_{BE} \rightarrow V_+ > I_C R_C$$

Where I_C is the current through one of the branches and $R_C = R_{C_1} = R_{C_2}$.

To maximize the gain, we provide an inverted input at the second input terminal. This doubles the gain of the signal and

improves noise performance. The inversion is done using a simple Op Amp inverting amplifier with the gain set to 1.

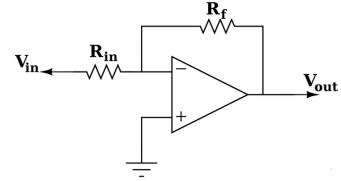


Fig. 3: The circuit of an Op Amp Inverter

It is easy to find the gain expression of the circuit.

$$V_{out} = -\frac{R_f}{R_{in}} V_{in}$$

For strict inversion, we choose the values of the resistances to be equal. The CMRR of the circuit is calculated using the following formula.

$$CMRR = 20 \log \frac{A_d}{A_c}$$

Here, A_d represents the differential mode gain and A_c represents the common mode gain. CMRR is a figure of merit that indicates the quality of the differential amplifier. The simulation results and the circuit results are attached in section VI.

III. GAIN STAGE

The gain stage is a CE amplifier with degeneration.

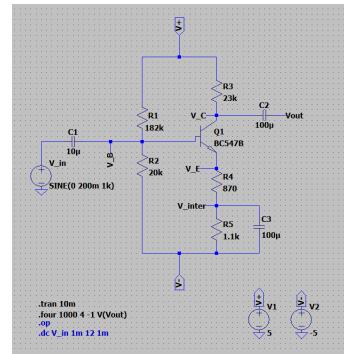


Fig. 4: Gain Stage Circuit

The Small Signal model and the gain expression for this stage are given below.

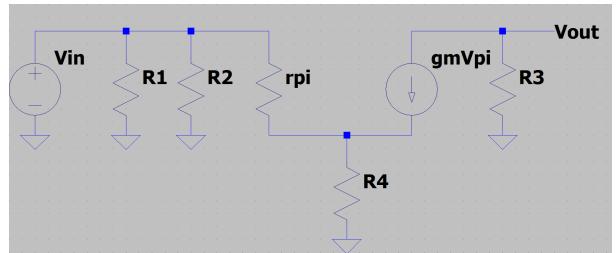


Fig. 5: Small Signal Model of the Gain Stage

The gain expression is

$$gain = -\frac{R_3}{\frac{1}{g_m} + R_4}$$

The input and output impedances are

$$R_{in} = R_1 || R_2 || r_\pi, \quad R_{out} = R_3$$

The simulation results and the circuit results are attached in section VI.

IV. FILTER

We have employed an active band pass filter.

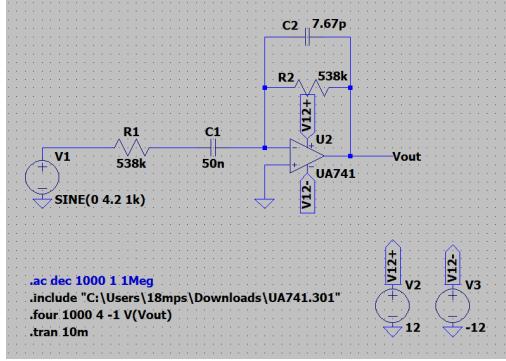


Fig. 6: Active Band Pass Filter Circuit

The transfer function of the filter is

$$-\frac{j\omega R_2 C_1}{(1 + j\omega R_1 C_1)(1 + j\omega R_2 C_2)}$$

For a pass-band gain of 0 dB, we must choose $R_1 = R_2$. Notice that $\omega = \frac{1}{R_1 C_1}$ and $\omega = \frac{1}{R_2 C_2}$ are the poles of the filter and $\omega = 0$ is a zero of the filter. Thus, we have to choose the values of the components so that the first pole is less than 20 Hz and the second pole is greater than 20 kHz.

V. POWER AMPLIFIER

The output at the filter stage does have the desired voltage amplitude, but it cannot be used directly to drive the load speaker. This is because the circuit will not be able to provide the required current. Thus, we need a power amplifier. We use diodes and resistors to bias the transistors in the power amp. This is because we want to maintain constant voltage across the BE junction in the transistors. The value of the resistors is chosen by calculating the estimated voltage drop across the diodes and applying a KVL. The circuit is given below. We add coupling capacitors at the input and output of the circuit.

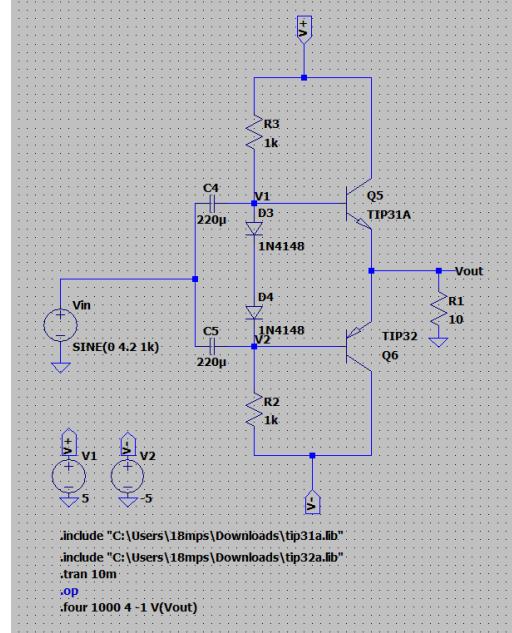


Fig. 7: Class AB Power Amplifier

We have to use Power transistors in place of regular transistors to support the currents. The node between the diodes is supposed to be at 0V, owing to the symmetry of the circuit. Thus, the DC value of the voltage at the base terminal is about 0.7V for Q5. The values for the resistors chosen are explained in section VI.

VI. CIRCUIT DESIGN AND MEASUREMENT

In this section, we discuss the circuit design procedure and the details for each of the components. Firstly, the filter stage uses ±12V rails. Using LM7805 and LM7905 voltage regulators, we convert the ±12V to ±5V and power up the rest of the circuit. We also used heat sinks for the voltage regulators and power transistors in the power amplifier to avoid overheating. However, all these details are abstracted out in the simulations.

A. Pre Amplifier Design

As discussed before, the preamplifier needs differential signals and we are using an op-amp based inverter to generate the inverted signal. For this inverter we use $R_1 = R_2 = 100k\Omega$ which are large enough and provide unity gain inversion. Our goal is to obtain largest gain (product of the gains of the Pre-Amplifier and Gain stages) possible without observing clipping with the constraint of ±5 volts supply. We have designed the preamp for a gain of 20.

We first choose a bias collector current, $I_C = 1mA$ to start off. This is a typical value used for designing analog circuits, however a different value could also be chosen, which would just result in different values for the passive elements viz. Resistors and Capacitors.

$$I_C = 1\text{mA} \quad (1)$$

$$\therefore g_m = \frac{I_C}{V_T} = \frac{1}{26.1} = 38.3 \text{ mS} \quad (2)$$

$$\therefore R_{C2} = R_{C1} = \frac{20}{38.3m} \approx 522\Omega \quad (3)$$

Here the equation (3) is written based on the gain expression derivation done in the second section. Now for calculating R_E , we use the fact that there is drop of **0.634 V** across the B-E junction. Since the DC voltage at the base terminals of the BJTs are 0, the Emitter is operating at **-0.634 V**. Now using the fact that the emitter current, I_E is almost equal to that of I_C , applying simple KCL at the emitter node and ensuring $I_{C1} = I_{C2} = 1\text{mA}$, we have $I_E = 2\text{mA}$. Thus using the emitter voltage and current, applying ohm's law, we get -

$$R_E = 2.18\text{k}\Omega. \quad (4)$$

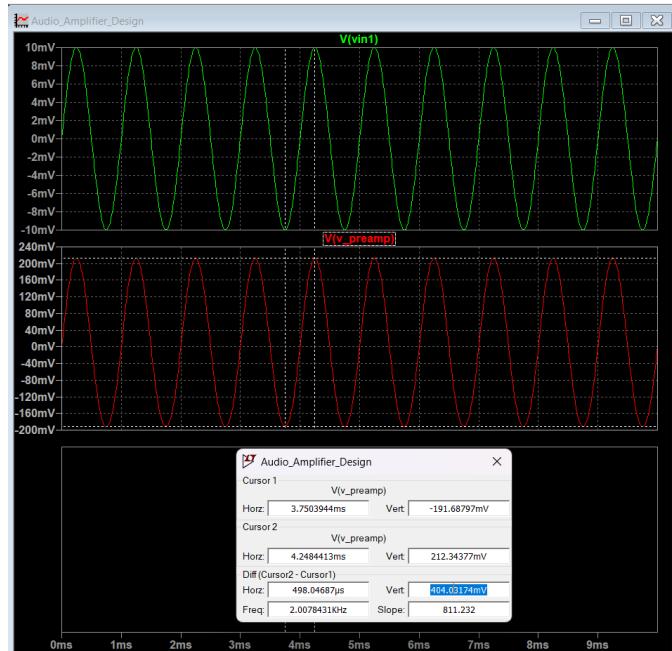


Fig. 8: Preamplifier Simulation Result

Now, simulating the circuit with these values, we first of all see that the bias current is slightly smaller than expected. Thus we reduce R_E to **2.1k** Ω . Then we see that the gain obtained is close to 16 and not 20. This is clearly because of the non-ideal conditions not seen in the simple equations. Thus we iterate R_C slightly to obtain the required gain. We end up with $R_C = 560\Omega$.

The final simulation result is shown in 8. The first pane is the 20mV pk-pk input signal, and the second is the preamp output. The cursor measurement show that the output is a $\approx 400\text{mV}$ pk – pk signal, which is a gain of 20.

Now we simulate the same on hardware and we obtain the following results. WavGen from the oscilloscope is used to

provide the required 20mV pk-pk signal 1k Hz signal. As seen in the measurements, we obtain a gain of 20 as was designed.

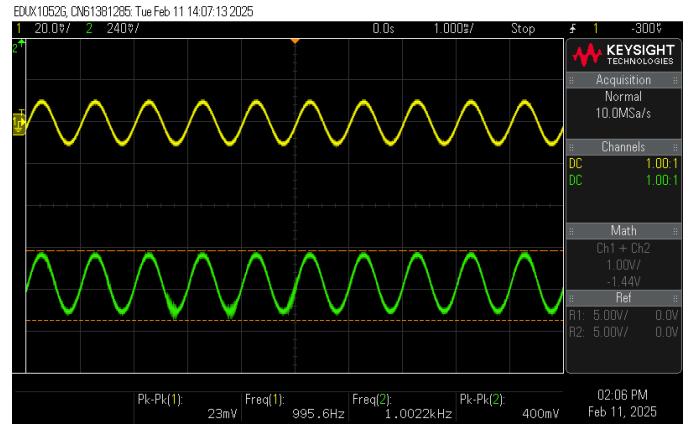


Fig. 9: Preamplifier Hardware Results



Fig. 10: Common Mode Gain

Using the value of common mode voltage gain below, we can calculate the CMRR.

$$CMRR = 20 \log \left(\frac{20}{0.15} \right) = 42.48$$

B. Gain Stage Design

Now we design the gain stage for the desired results. The fact that there is a drop of 0.634 V drop across the B-E junction of the BJTs, this reduces the voltage swing available and thus constraints us from aiming for a gain of 500. Keeping this in mind, we choose a gain of 450, which is an achievable goal. Although moving forward, we will see that the actual gain observed is a bit smaller but still good enough for the circuit's job which is to drive the speaker.

Hence for an overall gain of 450, we need a gain of 22.5 from the gain stage. As before, we start our procedure by choosing the bias collector current. This time, we choose $I_C = 0.2\text{mA}$. This value has been taken after multiple attempts at

designing and each time changing the bias current value so as to get reasonable values for the resistors. Thus we have -

$$I_C = 0.2 \text{ mA} \quad (5)$$

$$\therefore g_m = \frac{I_C}{V_T} = \frac{1}{26.1} = 7.66 \text{ mS} \quad (6)$$

Then, we choose the voltage bias values. Note that we are operating between the rails of $\pm 5V$. We first choose $V_C = 0.5V$. This allows for a $4.5V$ swing at the top and also ensures that the B-C junction stays reversed biased for the BJT to be in Forward Active Mode. Then we choose $V_B = -4V$. This again ensures the forward active condition. Then assuming the $0.634V$ drop across the B-E junction $V_E = -4.634V$. To obtain the biasing for V_B , the circuit uses a resistor divider. Having $-4V$ at the base is a 1:9 division between the rails. To ensure that large current doesn't pass through these resistors, these also have to be significantly large. Hence we choose $R_1 = 180 \text{ k}\Omega$, $R_2 = 20 \text{ k}\Omega$ as these satisfy these conditions. For other components, we have -

$$R_C = \frac{5 - 0.5}{0.2m} = 22.5 \text{ k}\Omega \quad (7)$$

$$\text{Using gain} = -\frac{R_C}{\frac{1}{g_m} + R_4} \text{ and } R_C, g_m : \quad (8)$$

$$R_4 = 870\Omega \quad (9)$$

$$-4.634 - (-5) = (R_4 + R_5) * 0.2m \quad (10)$$

$$\therefore R_5 = 960\Omega \quad (11)$$

Now for the capacitor parallel to R_5 , we need its value such that, for the frequency range of 20-20 kHz, it offers a significantly lower resistance compared to the R_5 . We choose $C_3 = 100\mu\text{F}$ as this satisfies this condition.

One other important condition we also need to take care of is that the input impedance of the gain stage is much larger than that of R_C of the Pre-Amplifier stage so that this stage doesn't load the previous stage and reduce gain. Here the values chose also satisfy this condition as $R_{in} = R_1 || R_2 || r_\pi = 180 \text{ k}\Omega || 20 \text{ k}\Omega || 38.4 \text{ k}\Omega \approx 12 \text{ k}\Omega$. This is almost **25 times larger** than R_C of preamp. Thus no impedance matching is required and loading is minimized.

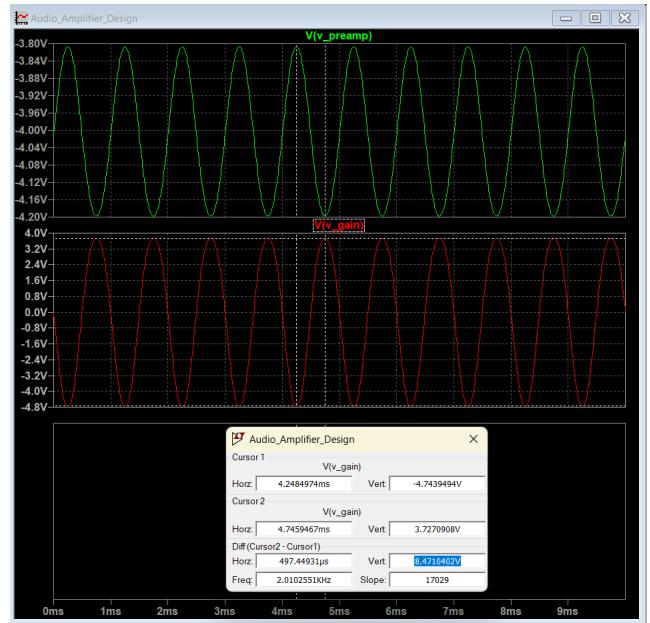


Fig. 11: Gain Stage Simulation Result

When gain stage was simulated with these values, we observed that the output was clipping at the lower end. This means that the B-C is going forward bias at the lower extreme of the collector voltage. Thus to tackle this problem, we need to increase the V_C or decrease I_C . This can be done by increasing the emitter resistor only for the quiescent current. We choose $R_5 = 1.1 \text{ k}\Omega$ which ensures that no clipping occurs. Next, we also observed that the required gain was not achieved. Thus we iterated on the R_C and found that $R_C = 23 \text{ k}\Omega$ gave the best gain possible, above which clipping happens. The actual gain observed was around **21.2** which is bit lesser than 22.5 which was the target. However this is because of the non-ideal and non-linear behavior of the BJT device.

As seen in 11, the output has a **8.47V pk-pk** which translates to a gain of **424**. This is a good enough value and is within **5%** of the gain we were aiming for.

Now we simulate the same on Hardware and as before use the oscilloscope for WavGen and viewing signals. We have the following plot. As seen in the measurement, the output is 8.5V pk-pk, which matches the simulations.

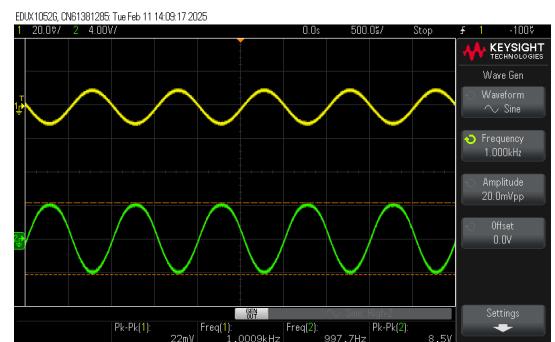


Fig. 12: Gain Stage Hardware Results

VII. FILTER STAGE DESIGN

Next, we design the Bandpass filter, which passes the frequencies between 20 Hz and 20 kHz. In this filter, the lower cutoff of the passband is determined by the product of R_1, C_1 whereas the higher cutoff is determined by the product of R_2, C_2 . To have a unity gain in the filter stage, we also choose the values such that $R_1 = R_2$. One other thing that we must ensure is to take large enough resistors so that this stage doesn't load the gain stage. This eliminates the need for impedance matching.

We choose the lower cutoff to be around **6 Hz** and the higher cutoff to be around **60 kHz**. Corresponding to these values, we have :

$$R_1 = 531 \text{ k}\Omega, C_1 = 50 \text{ nF} \quad (12)$$

$$R_2 = 531 \text{ k}\Omega, C_2 = 5 \text{ pF} \quad (13)$$

Simulating this, we have the following Bode Plot showing the filter characteristics. The two cursors are at 20 Hz and 20 kHz and, as seen from the measurements, the amplitude is within **0.5 dB** of the passband gain, and the plot rolls off for higher and lower frequencies than these cut-offs.

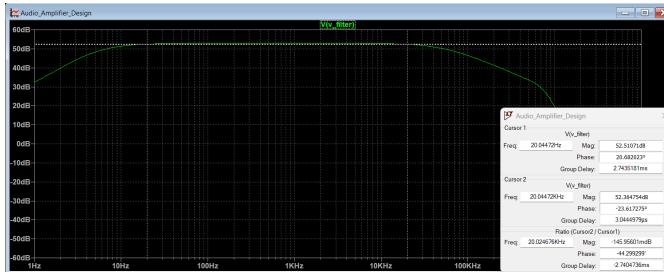


Fig. 13: Filter Stage Bode Plot

Now making the same circuit on hardware, we slightly change the values so as to attenuate much higher frequencies than 20 kHz. We now choose the higher cutoff to be **38.5 kHz**. And for this, we have the new values as follows :

$$R_1 = 538 \text{ k}\Omega, C_1 = 50 \text{ nF} \quad (14)$$

$$R_2 = 538 \text{ k}\Omega, C_2 = 7.67 \text{ pF} \quad (15)$$

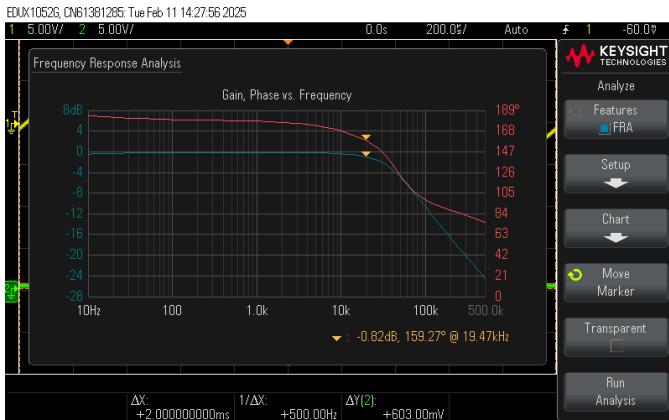


Fig. 14: Filter Stage Hardware Results

We have the above Bode plot taken on the hardware circuit. The cursor is currently on the 20 kHz mark and this due to a smaller higher cutoff, we see an earlier roll off. This ensures that unwanted high frequency noise is attenuated.

The final stage is the power amplifier. We consider the drop across the diodes to be 0.634 V each. Thus, the voltage across each of the resistors can be calculated. This is because the circuit is symmetric and the same current flows through both the resistors.

$$I = \frac{10 - 2 \cdot 0.634}{2 \cdot R}$$

$$R = \frac{4.366}{I} \Omega$$

We have a power constraint as well. Typically our voice signals have an amplitude of 10mV, which when passed through our amplifier, gives a signal of amplitude 5V. The speaker also needs a power of 0.5W to produce the output. Thus, the peak current must be 0.4 mA. We are observing a current of 0.37 mA in the simulations. The base current is $\frac{0.37mA}{\beta}$. From the data sheet, the value of β is 208. Thus, the base current is 1.9mA. The current I through the resistors must be much larger than the base current. Assume that it is 10 times larger. We obtain the value of each resistor as 218Ω. However, we observe that this causes a loading effect on the previous stage and after iteration, we have used a resistance of 500 Ω in the simulation and used a resistance of 1kΩ in the hardware.

Putting all these blocks together, the final circuit and results are attached below.

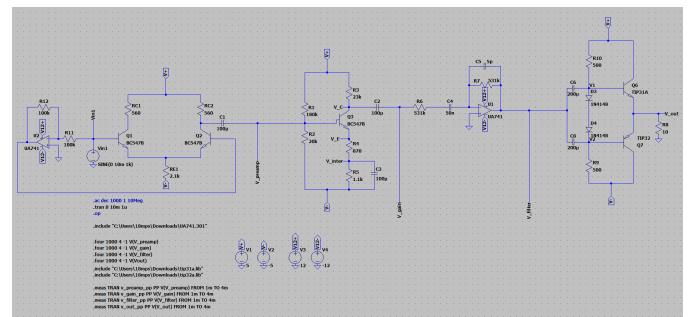


Fig. 15: Simulation Circuit

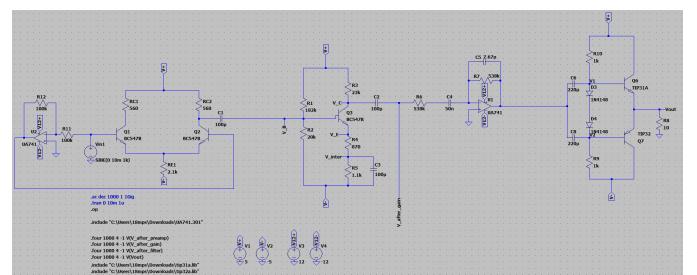


Fig. 16: Hardware values

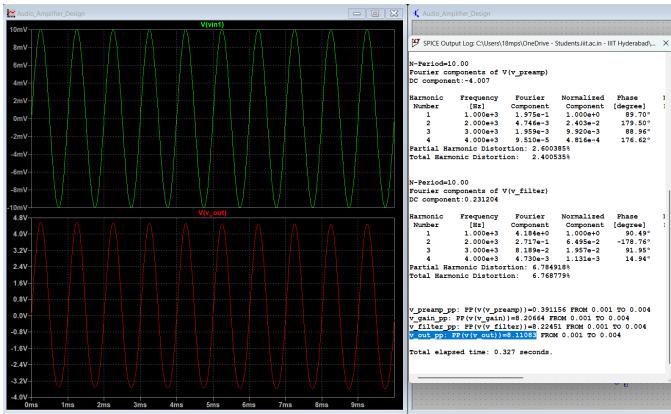


Fig. 17: Simulation result

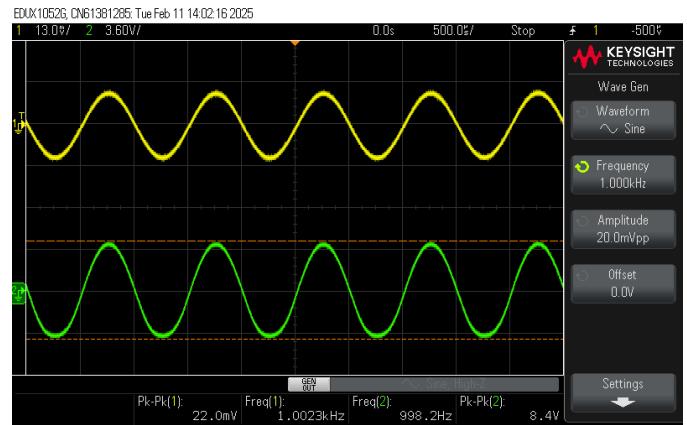


Fig. 20: Hardware Result

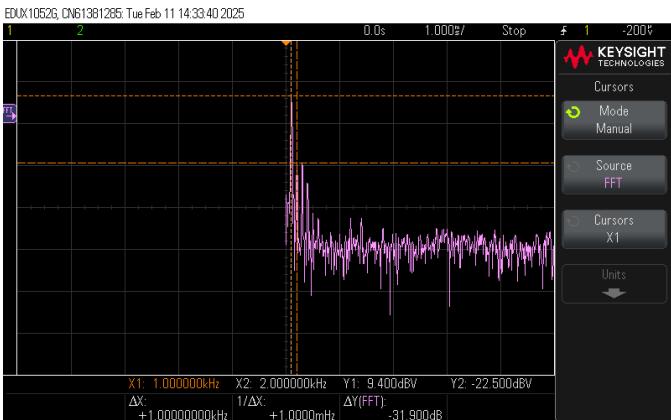


Fig. 18: Hardware circuit THD analysis



Fig. 21: Hardware Frequency Response - Midband Gain

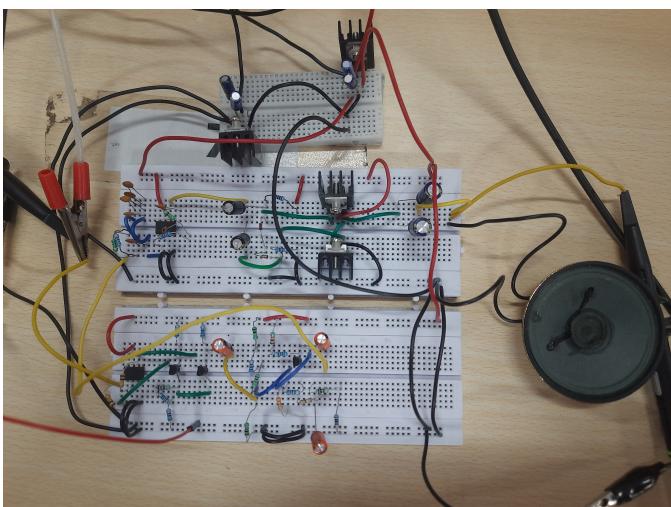


Fig. 19: Hardware Circuit



Fig. 22: Hardware Frequency Response - Higher Cutoff

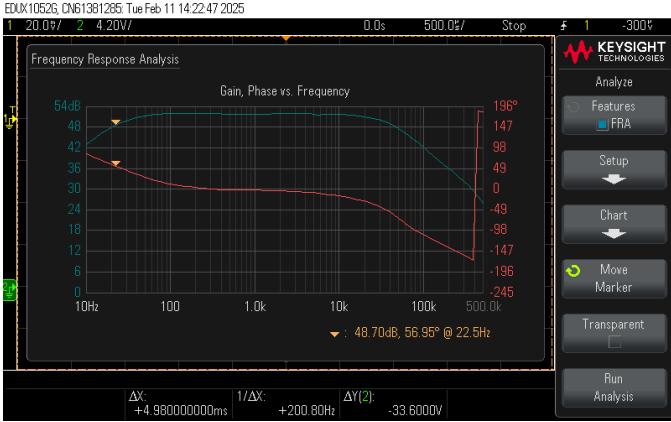


Fig. 23: Hardware Frequency Response - Lower Cutoff

Parameter	Simulation	Hardware
Gain	406	420

TABLE II: Comparison of Gain in Simulation and Hardware for the Audio Amplifier. All the values are recorded for an input voltage of 20mV pk-pk

VIII. PERFORMANCE PARAMETERS

Now to characterize the performance of the circuit, we look at three parameters.

A. Distortion Analysis (THD)

Distortion Analysis is done to determine the amount of unwanted harmonic content in the frequency content of a signal. It can further elaborate on the behavior of the circuit at different frequencies. THD quantifies how much a circuit distorts an input signal by measuring the relative power of harmonics (multiples of the input frequency) to the fundamental frequency. It is a key parameter for evaluating the linearity and signal fidelity of analog circuits. It is calculated as follows.

$$THD = \sqrt{\frac{\sum_{n=2}^{\infty} V_n^2}{V_f^2}} = 6.82\%$$

In Spice, we calculate THD by running **.four 1000 4 -1 V(V_Signal)**. Running the same for signal at the output of Pre-amp, Gain Stage, Filter Stage and the final output, we get the following in the Spice Output Log.

As seen below, the THD of the final output is around **6.82%**. This is less than 10% and therefore is a good value for THD. The difference between the fundamental frequency and the harmonic with the highest gain is at least **24dB**. This means that the most significant harmonic is **attenuated at least 16 times**.

N-Period=10.00 Fourier components of V(vout) DC component: 0.216222					
Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	1.000e+3	4.120e+0	1.000e+0	90.37°	0.00°
2	2.000e+3	2.705e-1	6.767e-2	-178.91°	-269.44°
3	3.000e+3	7.689e-2	1.842e-2	95.12°	85.75°
4	4.000e+3	4.582e-3	1.112e-3	16.66°	-73.71°
Partial Harmonic Distortion: 6.827396% Total Harmonic Distortion: 6.834711%					
N-Period=10.00 Fourier components of V(v_gain) DC component: -0.252368					
Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	1.000e+3	4.182e+0	1.000e+0	-90.36°	0.00°
2	2.000e+3	2.721e-1	6.595e-2	-0.70°	89.65°
3	3.000e+3	8.127e-2	1.943e-2	-91.24°	-0.88°
4	4.000e+3	4.547e-3	1.087e-3	-177.63°	-87.27°
Partial Harmonic Distortion: 6.789864% Total Harmonic Distortion: 6.718764%					
N-Period=10.00 Fourier components of V(v_preamp) DC component: -4.007					
Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	1.000e+3	1.975e-1	1.000e+0	89.70°	0.00°
2	2.000e+3	4.746e-3	2.403e-2	179.50°	89.80°
3	3.000e+3	1.959e-3	9.920e-3	88.96°	-0.74°
4	4.000e+3	9.510e-5	4.816e-4	176.62°	86.92°
Partial Harmonic Distortion: 2.600385% Total Harmonic Distortion: 2.400535%					
N-Period=10.00 Fourier components of V(v_filter) DC component: 0.231204					
Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	1.000e+3	4.184e+0	1.000e+0	90.49°	0.00°
2	2.000e+3	2.717e-1	6.495e-2	-178.76°	-269.25°
3	3.000e+3	8.189e-2	1.957e-2	91.95°	1.46°
4	4.000e+3	4.730e-3	1.131e-3	14.94°	-75.54°
Partial Harmonic Distortion: 6.784918% Total Harmonic Distortion: 6.768779%					

Fig. 24: THD for various signals

B. Common Mode Rejection Ratio (CMRR)

CMRR is a key parameter in differential amplifier circuits. It quantifies the amplifier's ability to reject common-mode signals (same phase) while amplifying the differential signal (the difference between inputs).

Using the value of common mode voltage gain below, we can calculate the CMRR. This value of **42.48dB** is considered pretty good for the audio amplifiers. Although using better BJTs, the noise performance can be improved drastically to obtain a much better CMRR.

$$CMRR = 20 \log \left(\frac{20}{0.15} \right) = 42.48dB$$



Fig. 25: Common Mode Gain

C. Slew Rate (SR)

Slew rate defines how quickly an amplifier can respond to a rapid change in the input signal. It is a measure of the maximum rate of change of the output voltage over time. Plotting this trace in the simulation, we get -

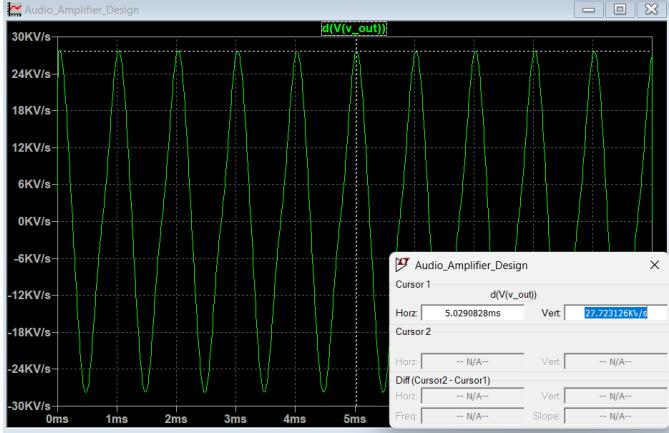


Fig. 26: Slew Rate Plot

From the above plot, we have the following. This is a good value as this means it can handle **880kHz** at 5V peak. This easily exceeds the audio frequency range of 20 kHz, making it more than sufficient for high-fidelity audio applications.

$$S.R. = \max\left(\frac{\delta V_{out}}{\delta t}\right) = 27.7 \text{ kV/s}$$

D. Temperature Variations (Stability Factor)

The stability factor (S) measures how sensitive the collector current (I_C) is to changes in the reverse leakage current (I_{CBO}). This is important because temperature variations affect I_{CBO} , and excessive dependence on it can lead to thermal runaway in BJTs. The following is the derivation of the formula:

The collector current (I_C) in a BJT amplifier is given by:

$$I_C = \beta I_B + (\beta + 1) I_{CBO} \quad (16)$$

Differentiating with respect to I_{CBO} :

$$\delta I_C = \beta \delta I_B + (\beta + 1) \delta I_{CBO} \quad (17)$$

Dividing both sides by δI_{CBO} :

$$S = \frac{\delta I_C}{\delta I_{CBO}} = \beta \left(\frac{\delta I_B}{\delta I_C} \right) + (\beta + 1) \quad (18)$$

If feedback is present (e.g., through emitter degeneration), we modify the expression to:

$$S = \frac{\beta + 1}{1 - \beta \left(\frac{\delta I_B}{\delta I_C} \right)} \quad (19)$$

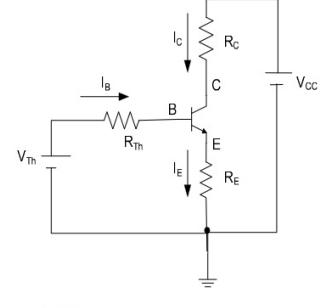


Fig. 27: Circuit for Stability equation derivation

From the above image, writing KVL equation, we have-

$$V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0 \quad (20)$$

$$V_{Th} = I_B R_{Th} - V_{BE} - (I_B + I_C) R_E \quad (21)$$

Differentiating Equation (21) w.r.t I_C :

$$0 = R_{Th} \left(\frac{dI_B}{dI_C} \right) + (1 + \frac{dI_B}{dI_C}) R_E \quad (22)$$

Solving for $\frac{dI_B}{dI_C}$:

$$\frac{dI_B}{dI_C} = - \frac{R_E}{R_{Th} + R_E} \quad (23)$$

Expression for Stability Factor S

We substitute $\frac{dI_B}{dI_C}$ into the stability factor equation:

$$S = (\beta + 1) \left(\frac{R_{Th} + R_E}{R_E(\beta + 1) + R_{Th}} \right) \quad (24)$$

Alternatively, this can be rewritten as:

$$S = (\beta + 1) \left(\frac{1 + \frac{R_{Th}}{R_E}}{(\beta + 1) + \frac{R_{Th}}{R_E}} \right)$$

Substituting, $R_E = 1.97k\Omega$, $\beta = 294.3$ and $R_{TH} = 12.3k\Omega$, we get - **7.07**. This is a fairly good value for stability and our circuit can handle a fair amount of temperature variations, hence our circuit it is not prone to thermal runaway.

IX. CONCLUSION

A few recordings of the project are provided [here](#) where we played songs with diverse beats and recorded the speaker output.

In this document, we have discussed the procedure to design an audio amplifier and went through the details of different stages in the audio amplifier. There is a huge scope for improvement. For instance, the band pass filter implemented was a first-order active filter. A higher order filter with a sharper roll off will result in a better output. One method to do this is to stack two first order filters but there are other configurations like the Butterworth filter or a Chebyshev filter which offer better performance. The current circuit also faces issues with thermal runaway. In a taped out circuit, this issue can be addressed by placing the diode right next to the transistor. However, it is not possible to fully address this issue with off-the-shelf components and heating up of components starts to degrade the performance of the circuit. As we are pushing our design to perform very closely with the limit of the technology, heating up will show irregularities in performance. One can come up with a solution to this issue.

REFERENCES

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- [4] Professor Fiore's videos on Power Amplifiers, <https://www.youtube.com/watch?v=0akOGTXwJWYt=5s>