Quadrature Down Converter

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***Abstract*—The Quadrature Down Converter, widely known as QDC, is a vital component in modern communication systems. The working principle revolves around bringing down a signal from the higher frequencies to the base band. As the name implies, the process is carried out by combining the input with two signals that have a phase difference of 90°. Can you imagine demodulating any signal just using 2 sinusoidal waves out of phase by 90° ?! The various blocks of a down converter have been detailed along with circuits, simulations and practical results. The Quadrature Down Converter is commonly used in modern day wireless receivers (RX) such as Bluetooth, Wi-Fi and WLAN.**

I. Essence of Quadrature Operation

Oscillators are a vital part of the communication, without which Down Conversion and Up Conversion of the signals at the receiving end and at transmitting end respectively, would not have been possible. Thus, having a reliable oscillator is a key part of designing reliable communication systems.

We are implementing a Superheterodyne Down Converter which converts the received signal to intermediate frequency levels. This signal is processed further by subsequent stages of filtering, amplification, and demodulation to obtain the base band message signal intended to be received. There are other types of Down Converters, namely the Direct Down Converters which directly convert the pass band signals to base band without the intermediate stage. The difference between them is that Direct Down conversion is a much simpler architecture and is, thus, power and cost efficient. The main drawback is the weak reliability of the operation and relatively poor performance. Superheterodyne converters, on the other hand, are much superior in performance and reliability. The process of Modulation and Demodulation is visualized on the spectrum as shown in Fig 1.

Why Quadrature Signals? I-Q signals as they are called (In-Phase and Quadrature Phase) in the receiver end is a fundamental aspect of many digital communication systems, especially those employing quadrature modulation schemes such as QPSK (Quadrature Phase Shift Keying) or QAM (Quadrature Amplitude Modulation). Since these signals are quadrature in nature, they are orthogonal to each other. Hence, the operation of one is completely independent of the other ensuring that the noise and other fluctuations in one channel has no effect on the other channel, ensuring discretion among the two channels. We are building a Quadrature Down Converter at the receiver end, which receives a Quadrature Modulated signal and converts it into an intermediate frequency. We are generating the quadrature signals of the same amplitude, thus, this is **QPSK Down Conversion**. We can vary the amplitudes, essentially using different states of the I-Q signals which leads us to **QAM Down Conversion** (Fig 3). Thus, using quadrature schemes allow us to transmit the data at higher rates.

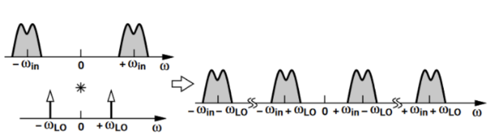

Fig. 1: Credits: RF Microelectronics, Behzad Razavi

In QAM, both Phase and Amplitude are varied allowing for a larger number of symbol states in comparison to QPSK. QAM can represent higher bits per symbol leading up to a higher data whereas the data rate in QPSK in much lower. The tradeoff between QAM and QPSK lies in the noise susceptibility. QAM is much more susceptible to noise, intuitively because this scheme uses multiple states and QPSK performs better in this aspect. The Signal-to-Noise ratio (SNR) of QPSK is higher than that of QAM. Depending on the applications where the modulation and demodulation schemes are used, QAM and QPSK can be selected based on the requirement.

As an example QAM is used in Wireless Lan (Wi-Fi), Television and video broadcasting, where high data rates are prioritised. On the other hand QPSK is used in Satellite and Mobile comm. where reliable data transfer is the priority.

II. Quadrature Oscillator Design

Oscillator is an autonomous circuit which produces a sinusoidal output. Omnipresent noise is picked up by the circuit and a certain frequency component resonates in the loop. To build up to the final oscillator design, we elaborate on the multiple components put together. A limiter connected to a Wien Bridge Oscillator followed by a Second Order RC Phase Shifter network. A buffer has been used to prevent loading and an amplifier has been used to scale the amplitude.

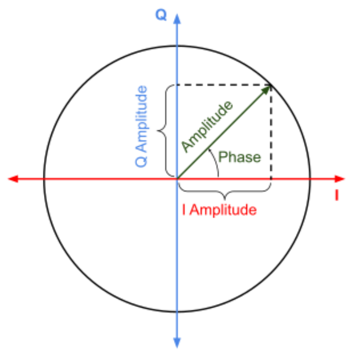

Fig. 2: Credits: commons.wikimedia.org/wiki/User:Vigneshdm1990

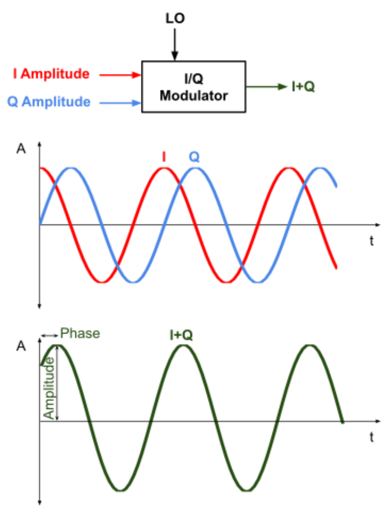

Fig. 3: Credits: commons.wikimedia.org/wiki/User:Vigneshdm19

A. Wien Bridge Oscillator

The Wien Bridge oscillator is the primary source of signal generation in our down converter design. Fig 4 shows the circuit of a Wien Bridge Oscillator. The frequency is selected by the feedback network which must satisfy the Barkhausen conditions for oscillations to occur. The Barkhausen conditions are (a) $A\beta \geq 1$ where A is the gain provided by the non-inverting amplifier and β is the feedback factor and (b) the overall phase shift of the loop must be $0°$ depicted in Fig 5.

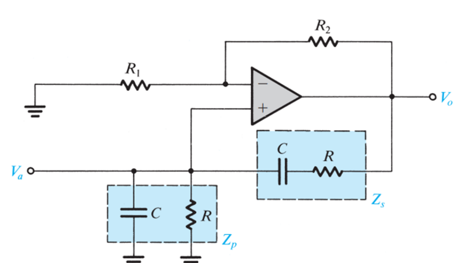

Fig. 4: Credits: Microelectronic circuits, Sedra and Smith

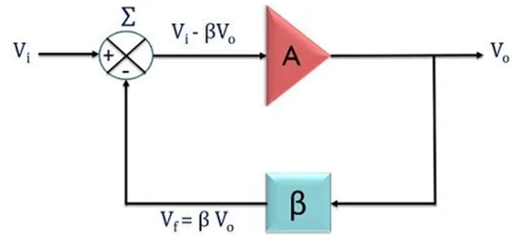

Fig. 5: Credits: electronicsdesk.com

The transfer function of a Wien bridge oscillator is computed as follows.

$$
\begin{aligned}
A\beta &= \left(1+\frac{R_2}{R_1}\right)\left(\frac{Z_p}{Z_s+Z_p}\right) \\
&= \left(1+\frac{R_2}{R_1}\right)\left(\frac{R \mid\mid \frac{1}{SC}}{R+\frac{1}{SC}+R \mid\mid \frac{1}{SC}}\right) \\
&= \frac{1+R_2/R_1}{3+1/SCR} \\
&= \frac{1+R_2/R_1}{3+SRC+1/SCR}
\end{aligned}
$$

$$
A\beta = \frac{1+R_2/R_1}{3+j\left(\omega RC-1/\omega RC\right)} \tag{1}
$$

For no phase shift, $\boxed{\omega = \frac{1}{RC}}$ To satisfy the unity loop gain condition, $\boxed{\frac{R_2}{R_1} \geq 2}$

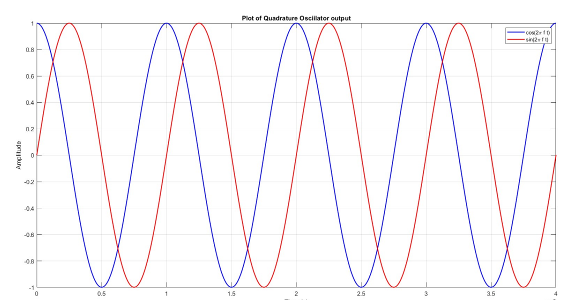

Fig. 6: Theoretical Oscillator Output Plotted on Matlab

Fig 6 shows the theoretical output plotted on Matlab. The wave in blue is the In-Phase signal, and the other in red, which is at a phase of 90 with respect to the In-Phase wave is the Quadrature-Phase wave.

B. Limiter

Amplitude control in oscillators is imperative owing to the saturation occurring in positive feedback. A non-linear amplitude control, soft limiting, design has been employed as opposed to the traditional clipper circuit, hard limiting, in order to preserve the sinusoidal nature of the output waveform.

Fig 7 shows the circuit of a limiter on the Wien bridge oscillator. Assuming a constant voltage model for the diodes, the equations pertaining to the circuit are given below.

In the circuit, when we are in the linear region,

$$v_1 = v_0 \frac{R_1}{R_1 + R_2}$$

. Conserving current at node A, we get

$$\frac{v_b - V}{R_6} = \frac{v_0 - v_b}{R_5}$$

$$v_b \left(\frac{R_6 + R_5}{R_5 R_6} \right) = \frac{v_0}{R_5} + \frac{V}{R_6}$$

$$v_b = \frac{v_0 R_6 + V R_5}{R_5 + R_6}$$

Similarly, $v_a = \frac{v_0 R_3 + V R_4}{R_3 + R_4}$

Consider the point where the diode D_1 just turns ON, $v_1 - v_a = V_{Diode}$

$$v_0 \frac{R_1}{R_1 + R_2} = V_{Diode} + \frac{v_0 R_3 + V R_4}{R_3 + R_4}$$

Similarly,

$$v_0 \frac{R_1}{R_1 + R_2} = \frac{v_0 R_6 + V R_5}{R_5 + R_6} - V_{Diode}$$

C. Poly phase RC Shifter

To produce the quadrature component of the oscillator, we have employed an RC phase shifter network. A second order network has been chosen to provide a phase shift of $90°$. Evidently, there will be an attenuation in the output. To compensate, a non-inverting amplifier has been used with the desired gain.

D. Buffer

The input impedance of the Phase Shifter must be high so as to not load the Wien Bridge oscillator. However, a high resistance implies a low capacitance. A very small value of capacitance would be affected significantly by the parasitic capacitance of the amplifier connected at the output. Thus, we notice this bottleneck and use a buffer between the Oscillator

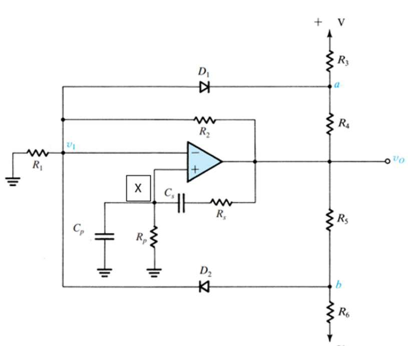

Fig. 7: Credits: Microelectronic circuits, Sedra and Smith

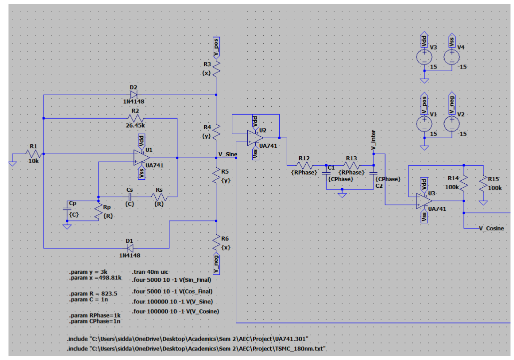

Fig. 8: LTspice schematic of Oscillator circuit

and the Phase Shifter.

We must choose the value of R_4 = R_5, R_3 = R_6, R_S = R_P and C_S = C_P. The first two to maintain symmetric limiting of the sinusoid and the latter two to select a particular frequency component. The cut-in voltage of the diode has been extracted to be 420 mV in simulations. We choose R_1 = 10 kΩ, R_2 = 20.3 kΩ $>$ 2 R_1 to start oscillations but found to be 26.45 kΩ. this error is due to the non ideality of the Op-Amp and the approximation of the diode model. The design is for V = $\pm$15 V to allow a good headroom for tweaking values. To select the frequency of 100 kHz, capacitance of 1 nF is taken and the theoretical value of resistance is found to be 1.59 kΩ by equating the -3 dB frequency to 100 kHz. However, this resistance does not yield the right frequency. A possible reason is the performance of the Op Amp at high frequencies is hindered by parasitic capacitors. 822 Ω was found to be optimal through iterations.

Upon plugging in the values in the equation of the limiter configuration, we obtain the ratio of R5 and R6 to be 166.27. For practical simplicity, the values chosen are 3 kΩ and 498.81 kΩ. To shift the phase, a polyphase (second order) shifter has been employed, each shifting the phase by $45°$. The capacitor is chosen to be 1 nF and resistor has to be $<$ 1.59 kΩ but practically, good values were obtained at 1 kΩ. The attenuated output is amplified using a traditional non-inverting amplifier. Since we require a gain of 2, the resistances were chosen to be equal to 100 kΩ.

Figures from Fig 8 to 12 show relevant simulations.

III. Switch (Mixer) Design

A MOSFET can be used to build a Switch serving the purpose of shifting the pass band signal to the base band. The MOSFET operates in the Triode region and the CUTOFF region, controlled by the oscillator input to the GATE. The gate is biased at a DC level equal to the Threshold of the MOSFET. This is to directly control the “Switch” using the sinusoidal oscillator input. The input signal is applied to the source of the MOSFET.

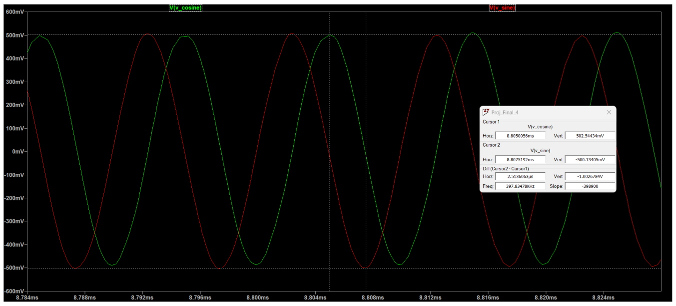

Fig. 9: Transient response of the Oscillator circuit

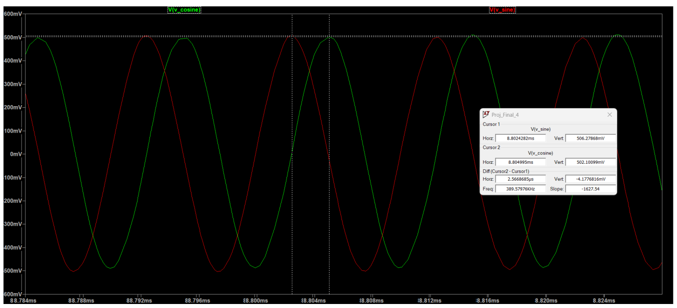

Fig. 10: Calculated phase from the cursors gives us 92.41°

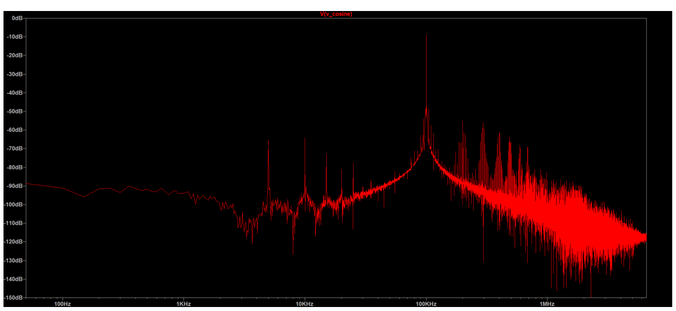

Fig. 11: FFT of the In Phase Wave

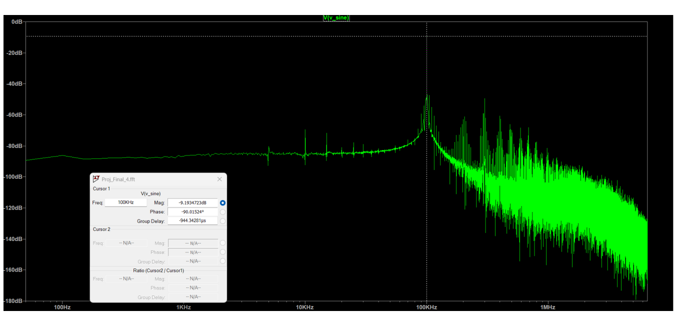

Fig. 12: FFT of the Quadrature Wave

$$v_{IF_I} = v_{in} \times v_{OSC_I} = \frac{A_1 A_2}{2}\left(cos(\omega_{in}t - \omega_{OSC}t) + cos(\omega_{in}t + \omega_{OSC}t)\right)$$

$$v_{IF_Q} = v_{in} \times v_{OSC_Q} = \frac{A_1 A_2}{2}\left(sin(\omega_{in}t + \omega_{OSC}t) - sin(\omega_{in}t - \omega_{OSC}t)\right)$$

Fig. 13: Credits: AEC Course Project Manual

INTUITION : Whenever the MOSFET is ON, the voltage at the source is seen at the Drain and when it is OFF, the output is shorted. At high frequencies, this can be modelled as a multiplication operation of the input signal in the time domain with an Impulse Train. Multiplication in the time domain corresponds to a convolution in the frequency domain and an Impulse train transforms to an Impulse train itself. Thus, we are convolving a pass band signal with an impulse train.

For example, let us consider a 95 kHz sinusoidal wave as the input signal. The spectrum of this signal consists of two impulses at frequencies 95 kHz and -95 kHz. Sampling it at 100 kHz would produce impulses at ..., -195 kHz and -5kHz, -95 kHz and 95 kHz, 5 kHz and 195 kHz, 105 kHz and 295 kHz, ... Had the input signal also had a message signal bandwidth, the spectrum of the message signal would have manifested itself at these impulses.

Fig 13 captures the mathematical equations that govern the mixer operation and Figures 16 to 17 show the simulations.

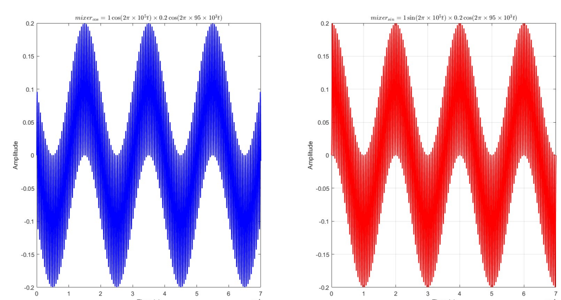

Fig. 14: Theoretical Mixer Output Plotted on Matlab

Fig 14 shows the expected theoretical output of the mixer. This has been plotted on Matlab. The plot on the left is the mixer output of I (In-Phase) signal and the one on the right is of Q (Quadrature-Phase) signal.

To set the value of V_{BIAS}, we follow the extraction procedure for the threshold voltage of the MOSFET. Fix the value of V_{DS} to a small value such that the device operates in the Triode region. Vary V_{GS} and using the acquire mode, plot the I_D vs V_{GS} curve. The maximum slope was found to be in between points 1 and 2 given below.

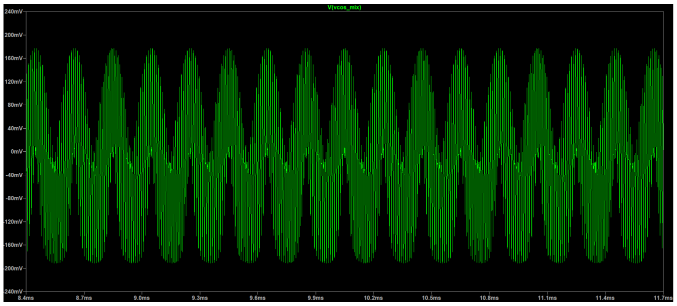

Fig. 15: Output of the Mixer for input of 95 kHz

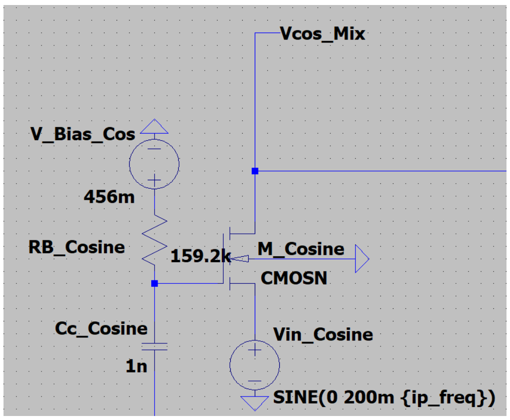

Fig. 16: Mixer Circuit

$$V_{DS} = 0.1\ V \qquad V_{GS_1} = 1.23\ V$$
$$V_{GS_2} = 1.2425\ V \qquad V_{o_1} = -48.125\ mV$$
$$V_{o_2} = -51.875\ mV \qquad I_{D_1} = 48.125\ \mu A$$
$$I_{D_2} = 51.875\ \mu A$$

Thus, $\Delta V_{GS} = 0.0125\ V$ and $\Delta I_D = 3.75\ \mu A$

The maximum slope of I_D vs V_{GS} is $0.3\ \times\ 10^{-3}\ \frac{A}{V}$

The tangent line drawn at point 1 is

$$I_D = 0.3\ \times 10^{-3}\ V_{GS}\ +\ c$$

Substituting the point, we get, $c\ =\ -3.20875\ \times\ 10^{-4}\ A$
Substituting $I_D\ =\ 0$, $\boxed{V_T\ =\ 1.0695\ V}$

In the simulations, the value of the threshold voltage was extracted to be 456 mV, which is based on the TSMC file utilised.

From the data sheet of the MOSFET IC CD4007, the Width and Length of the MOSFET has been set to 170μm and 10μm respectively. Rest of the values like perimeter have been chosen based on the standard design parameter (λ) values.

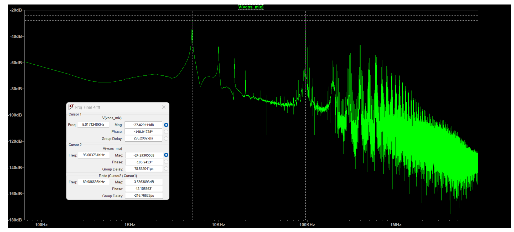

Fig. 17: FFT of the Mixer output with peaks at 5 kHz and 95 kHz for an input wave of 95 kHz

The values of the coupling capacitor and the bias resistance are chosen according to the high pass filter configuration conditions. The input frequency 100 kHz must lie in the mid band range of the high pass configuration. Choosing the capacitance to be 1 nF,

$$f = \frac{1}{2\pi\ RC}$$
$$RC = 1.5924\mu s$$
$$Choosing\ the\ value\ of\ C\ to\ be\ 1\ nF$$
$$R = 1.59k\Omega$$

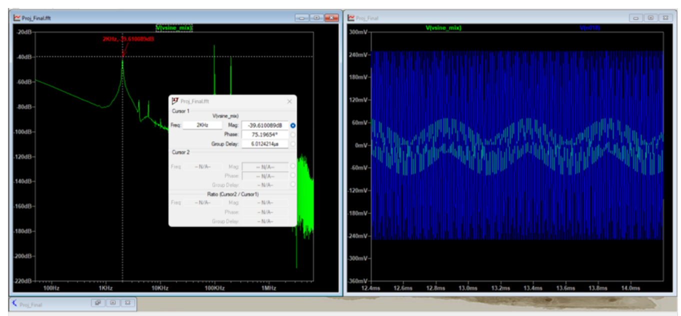

Fig. 18: Transient ans FFT plots of v_{in} and v_{IF} with f_{in} = 98kHz

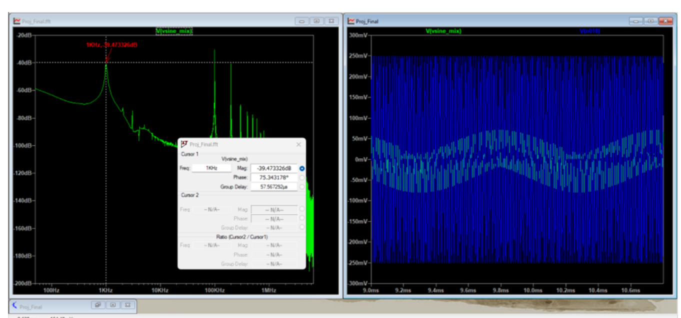

Fig. 19: Transient ans FFT plots of v_{in} and v_{IF} with f_{in} = 99kHz

To have the frequency of concern in the mid band comfortably, we choose a larger bias resistance (say 100x). Thus $R_{BIAS} = 160k\Omega$.

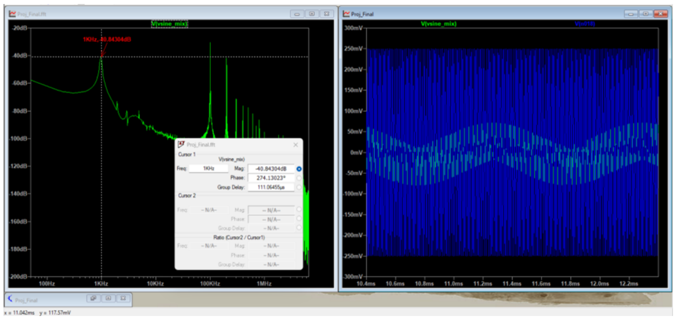

Fig. 20: Transient ans FFT plots of v_{in} and v_{IF} with f_{in} = 101kHz

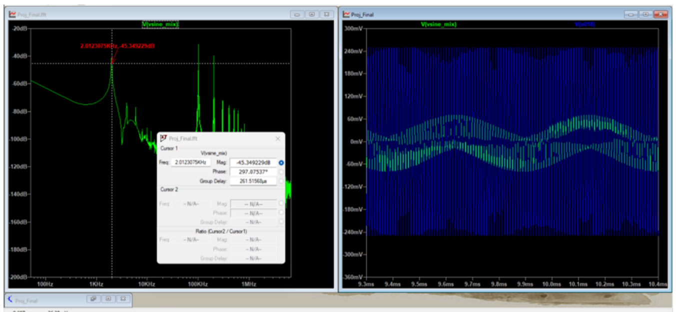

Fig. 21: Transient ans FFT plots of v_{in} and v_{IF} with f_{in} = 102kHz

The output of the mixer has multiple harmonics out of which the bandwidth of concern to us is the base band. Thus, this must be passed through a low pass filter to obtain the final base band signal.

IV. Low Pass Filter

As elaborated above, unwanted high frequency components are present in the output of the Mixer. To get rid of these components, we must pass it through a Low Pass filter. We deploy a second order RC low pass filter for this purpose. The cutoff frequency of the network was chosen as follows.

$$f_L = \frac{1}{2\pi\ RC}$$
$$RC = 79.58\mu s$$
$$Choosing\ the\ value\ of\ C\ to\ be\ 1\ nF$$
$$R = 79.58k\Omega$$

Again, for the frequency to lie in the Mid-band region, we shift the poles to the right by decreasing the resistance. A decent amplitude was observed at the resistance of $10k\Omega$, operating at a cutoff frequency of 15.923 kHz.

Due to a mismatch in the bias voltage to the Mixer and the Threshold voltage of the MOSFET, we observe that there exists an offset in the output of the Mixer. So we use a high pass filter with a relatively low cutoff frequency to eliminate the DC offset. The cutoff frequency of this is chosen to be

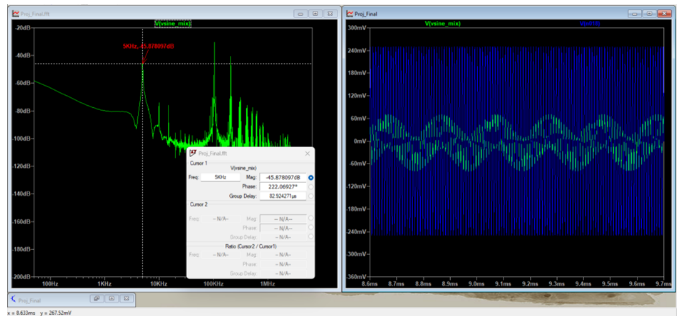

Fig. 22: Transient ans FFT plots of v_{in} and v_{IF} with f_{in} = 105kHz

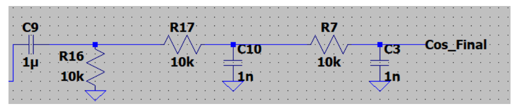

Fig. 23: Filter Circuit

lower than the expected output frequency but high enough to eliminate the DC components, thus, about 1000 times smaller than the low pass configuration which brings our capacitor value to 1 μF if we keep the resistance the same as 10 kΩ. Ultimately, the output of the Low Pass Filter block is the base band signal!

Figures 23 to 25 show the relevant simulations.

We can clearly see the low pass filtering action from the difference in Figures 17 and 25.

Here Fig 26 shows the corresponding -3dB frequency to be around 15.9kHz, which was the expected value. But Fig 27 shows the corresponding -3dB frequency to be around 5.4kHz because the filter stages are loading each other, thus having a different equivalent resistance and capacitance across the filter. This can simply be avoided by using a buffer, but would lead to increased hardware complexity. As 5.4kHz is provides a midband range for most part of our analysis, we proceed further with this.

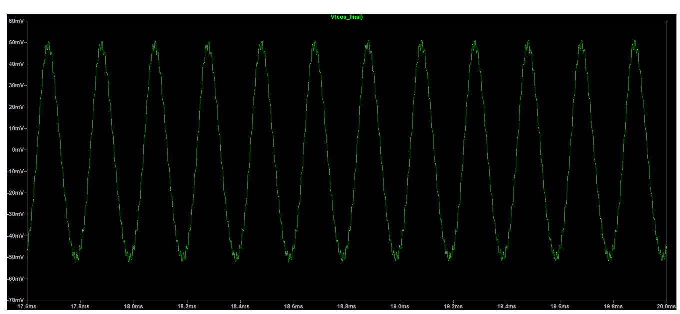

Fig. 24: Filter Output

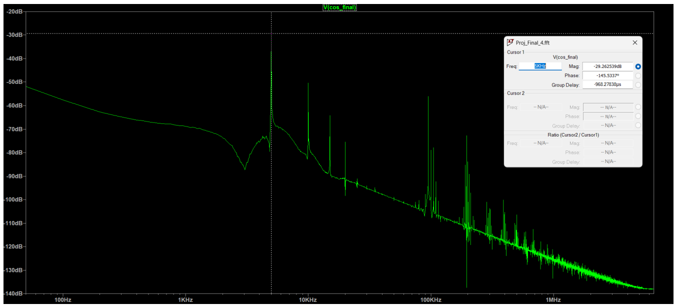

Fig. 25: FFT of the output

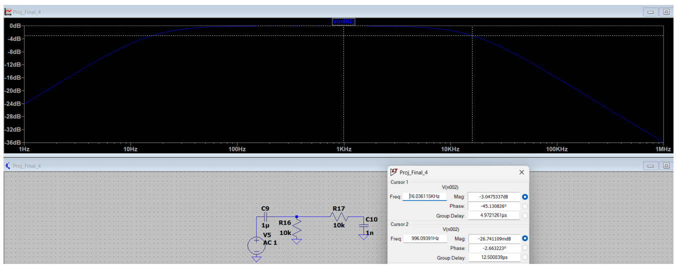

Fig. 26: Frequency response of Single Order LPF

V. Complete Circuit Prototype Design

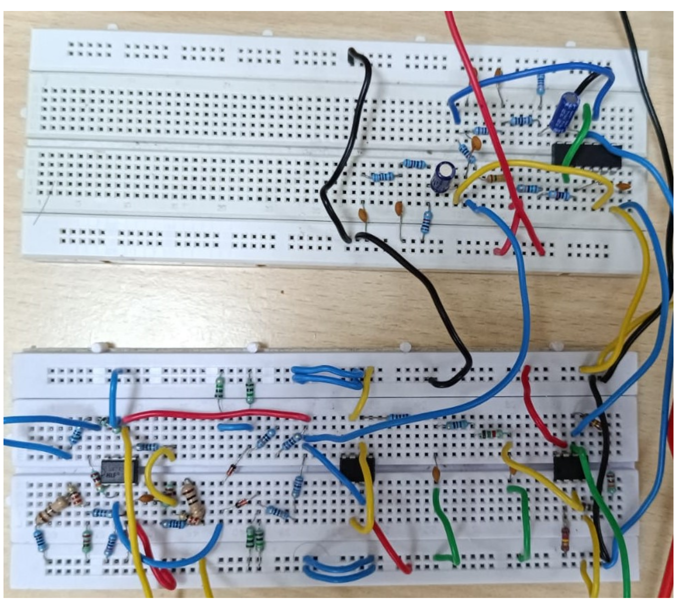

Fig. 29: Snap of the final Circuit

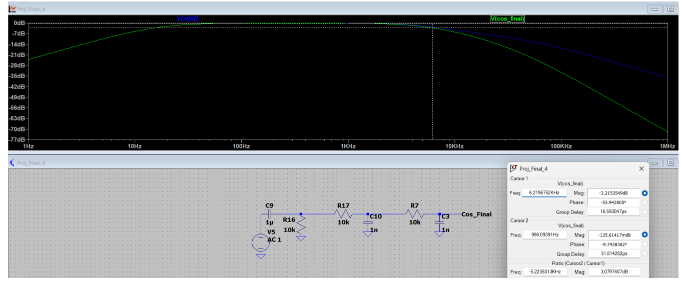

Fig. 27: Frequency response of Second Order LPF

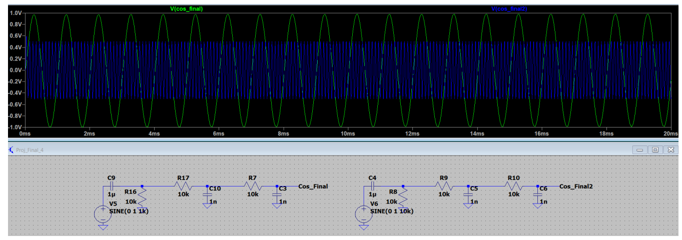

Fig. 28: Transient Response of 1kHz and 10kHz

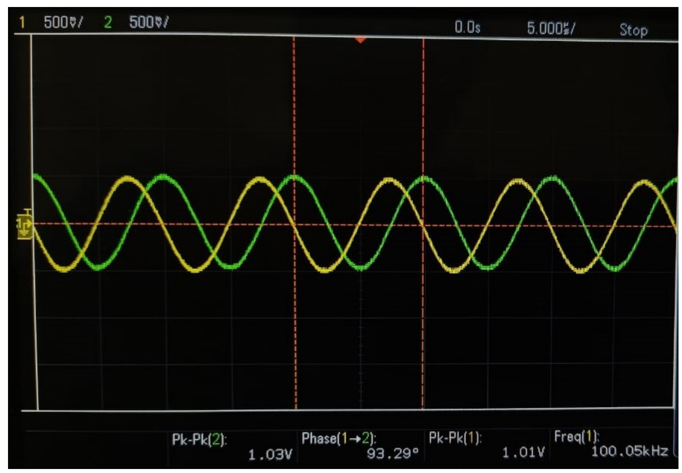

Fig. 30: Output of the Quadrature Oscillator

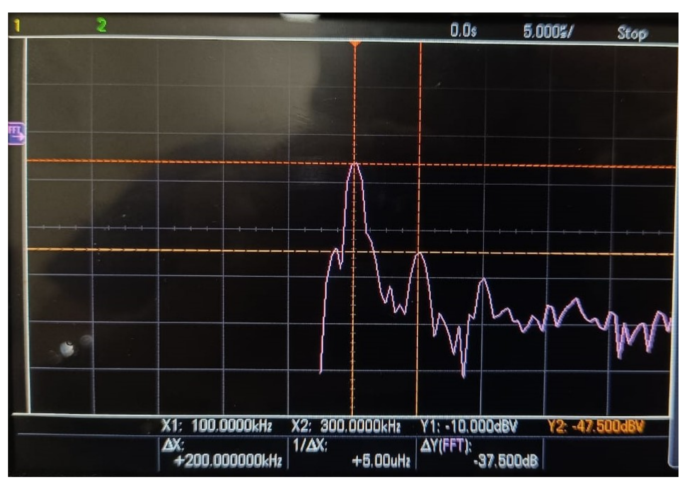

Fig. 31: FFT of Quadrature Oscillator Outputs

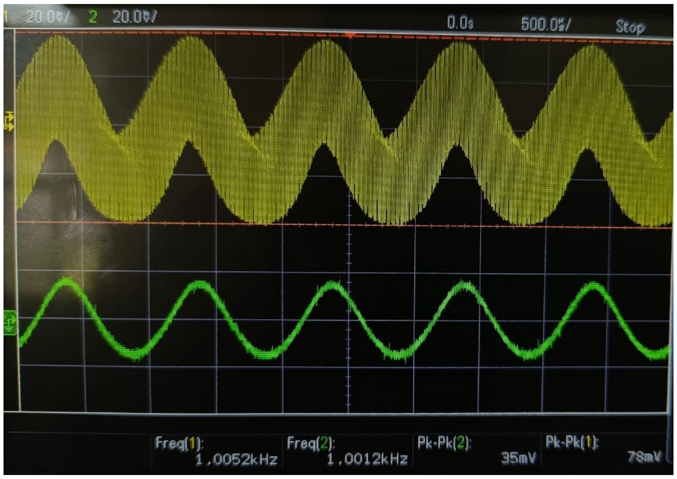

Fig. 32: Mixer Output of In-Phase signal with f_m = 99kHz

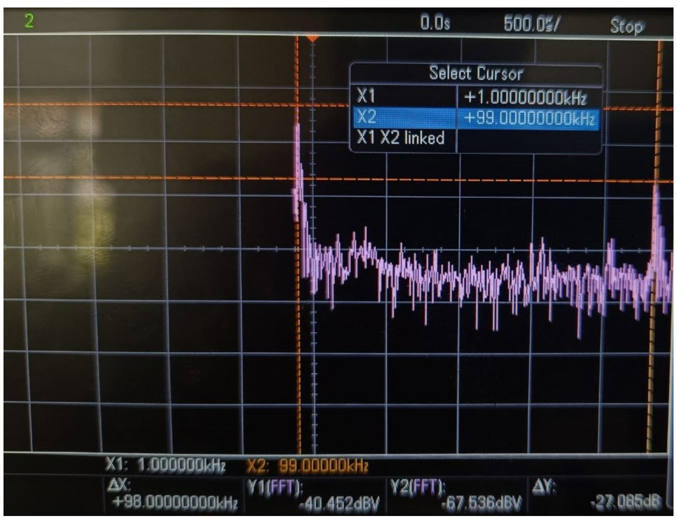

Fig. 33: FFT of Mixer Output of In-Phase with f_m = 99kHz

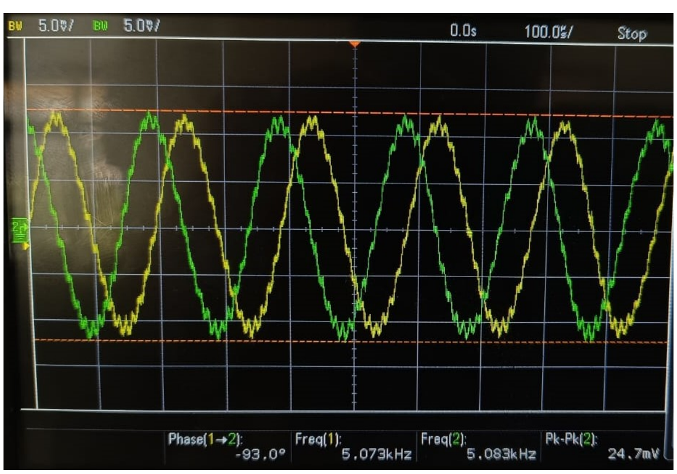

Fig. 34: Final Outputs of IQ signals, with f_m = 95kHz

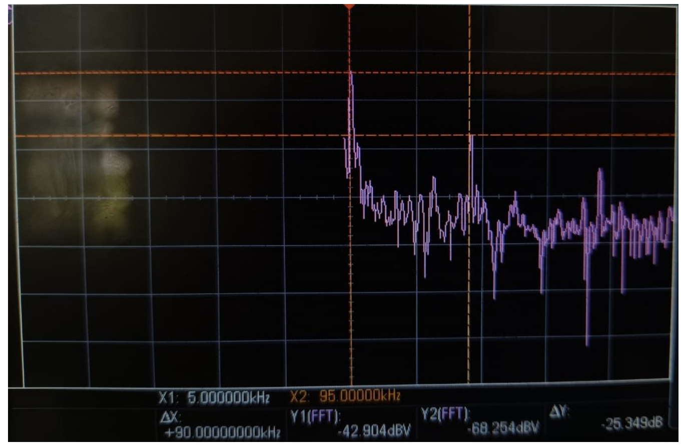

Fig. 35: FFT of the Final Output

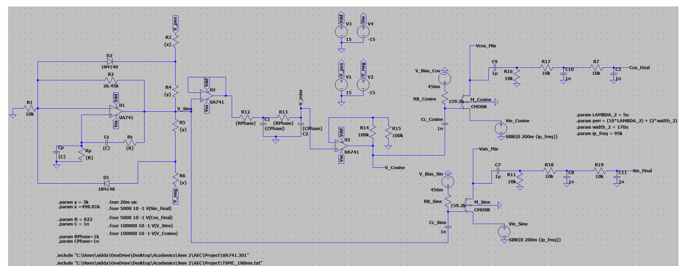
Fig. 36: Final Circuit Simulation

VI. Performance Summary

Table I captures all the parameters, results and circuit element values.

Further improvements include :

1) The oscillator can be designed for a lower supply voltage to reduce the power consumption. The current design uses a 15 V supply to allow for more headroom in the design. There is a definite scope for optimization in terms of power.

2) For a smoother output, a higher order low pass filter can be used. This will ensure a cleaner output by making the roll off steeper after the cutoff frequency.

3) The need for the high pass configuration after the mixer can be eliminated by accurately matching the bias voltage to the threshold voltage of the MOSFET. This can be achieved with high precision devices and accurate measurements

A few inevitable sources of error are :

1) Source variation in supplying a constant voltage of 15 V. When checked with a digital multimeter, the positive terminal and negative terminal yielded different output voltages.

TABLE I: Parameters for Design

Parameters	**Simulated**	**Measured**
Oscillator Frequency	100 kHz	100.05 kHz
Oscillator Amplitude (I-Phase)	1.004 V	1.03 V
Oscillator Amplitude (Q-Phase)	1 V	1.01 V
Input Frequency	95 kHz	95 kHz
IF	5 kHz	4.857 kHz
Supply	15 V	15 V
Supply	-15 V	-15 V
V_{BIAS}	456 mV	1 V
R_{BIAS}	159.2 kΩ	160 kΩ
C_C	1 nF	1 nF
R_1	10 kΩ	10 kΩ
R_2	26.45 kΩ	24.55 kΩ
R_p	822 Ω	1.0825 kΩ
R_s	822 Ω	1.0825 kΩ
C_s	1 nF	1 nF
C_p	1 nF	1 nF
R_3	498.81 kΩ	500 kΩ
R_4	3 kΩ	3.03 kΩ
R_5	3 kΩ	3.03 kΩ
R_6	498.81 kΩ	500 kΩ
R_{12}	1 kΩ	1 kΩ
R_{13}	1 kΩ	2.27 kΩ
C_1	1 nF	1 nF
C_2	1 nF	1 nF
R_{14}	100 kΩ	164 kΩ
R_{15}	100 kΩ	120 kΩ
C_9	1 μF	1 μF
C_{10}	1 nF	1 nF
C_3	1 nF	1 nF
R_{16}	10 kΩ	10 kΩ
R_{17}	10 kΩ	10 kΩ
R_7	10 kΩ	10 kΩ

2) Difference in resistance values is a limiting factor in tuning the circuit accurately. An error in large resistances would constrain the designer in tweaking the resistor values by small amounts.

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