Electronic Workshop - 2

Project - 2

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1 Introduction

Signal generators are a class of electronic devices that are considered as a vital part of test equipment setup for various applications ranging from consumer devices to aerospace and spacecraft programs. These systems are mainly used for testing, signal tracing, debugging, troubleshooting, etc. Signal generators generate different kinds of waveform in the form of an electrical signal based on the application, and are used as a stimulus for the item being tested.

We propose a novel signal generator with the following features :

1. Two Phase Synchronized channels
2. Sine, Square Triangle with variable Amplitude
3. Various Modulated Wave forms such as :
   (a) BFSK, QFSK, ... M - FSK (FSK - Frequency Shift Keying)
   (b) BPSK, QPSK, ... M - PSK (PSK - Phase Shift Keying)
   (c) Different PWM Signals (PWM - Pulse Width Modulation)
   (d) ASK (ASK - Amplitude Shift Keying)
   (e) Frequency Sweep
   (f) Conventional Amplitude modulation (Using a 4 Quadrant Multiplier)

Following is the complete circuit diagram. As seen in the figure, we are using two signal generators *AD9833*, *ESP-32* as the microcontroller, *74LS14N* Schmitt Trigger, *SN7486* XOR Gate, *TSH-82* High speed op-amps,*AD633JN* Analog Multiplier and *MC14051B* 8:1 Multiplexer. In addition, we also use *7805 and 7905* IC to convert the $\pm 8V$ to $\pm 5V$. The former is used to power the mixer and multiplexer whereas the latter is used to power the op-amps and other ICs.

The high speed op-amps TSH-82 provide a slew rate of $100\text{V}/\mu$ s, which is necessary for high frequency applications. The ESP-32 is connected to the laptop, where it is programmed by the user through the PC.

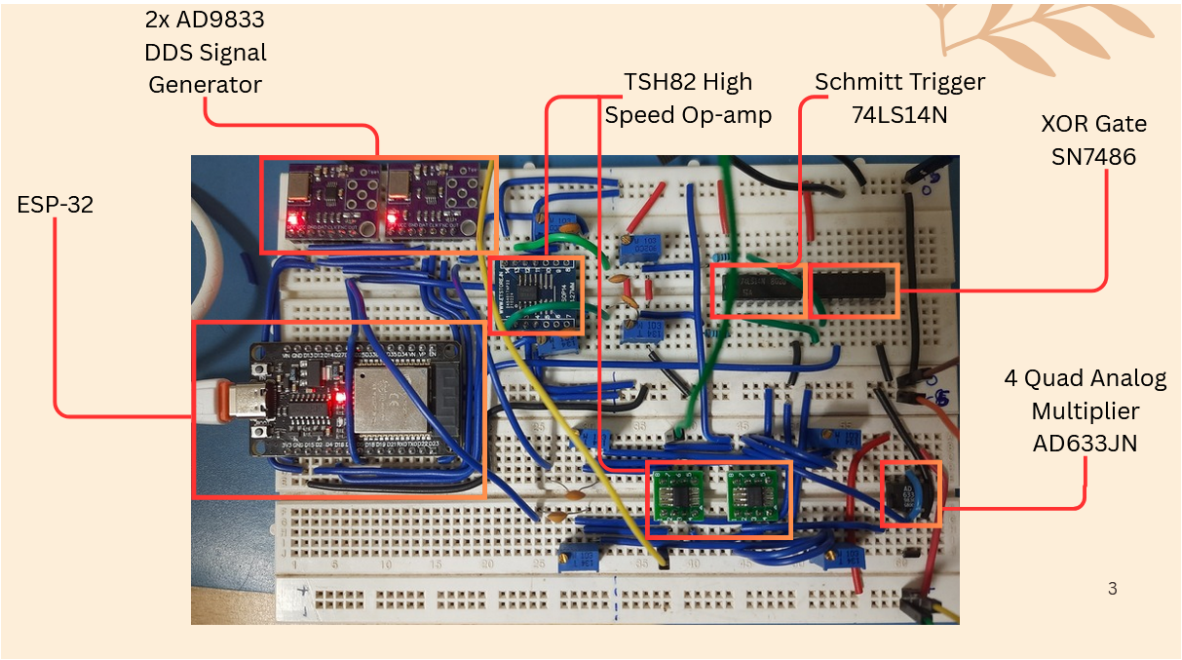


Figure 1: Complete Labelled Circuit

2 Basic Signal Generation

AD9833 is DDS based waveform generator IC which can generate Sine, Triangle and Square Wave at peak to peak voltage of about 0.6V, 0.6V, 5V respectively with a peak frequency of 12.5 MHz but the Quality and Amplitude of Signal deteriorate with increasing frequency. But the module generates acceptable waveforms until a maximum frequency of 3 MHz. It communicates over 3-wire serial interface SPI to set the Wave Type, Frequency, Modulating data and Phase which is provided by ESP-WROOM-32 MCU which acts as an interface between GUI (discussed in next section) and the signal generator. It is also responsible for establishing a feedback loop for phase synchronization. The internal circuitry of the AD9833 consists of the following main sections: a numerically controlled oscillator (NCO), frequency and phase modulators, SIN ROM, a DAC, and a regulator.
The NCO and modulators consist of two frequency select registers, a phase accumulator, two phase offset registers. The accumulator simply scales the range of phase numbers into a multibit digital word. The phase accumulator in the AD9833 is implemented with 28 bits. The input to the phase accumulator can be selected from either the FREQ0 register or the FREQ1 register and is controlled by the FSELECT bit. Modulation such as BFSK and BFPSK are performed by switching between the two registers. Following the NCO, a phase offset can be added to perform phase modulation using the 12-bit phase registers in a method similar to BFSK modulation. The AD9833 has two phase registers; their resolution is $2\pi/4096$ which is approximately 0.08794. The time taken to switch between registers using MCU is about 39 uS. This gives the maximum baud rate possible for Binary Modulations which are discussed further.

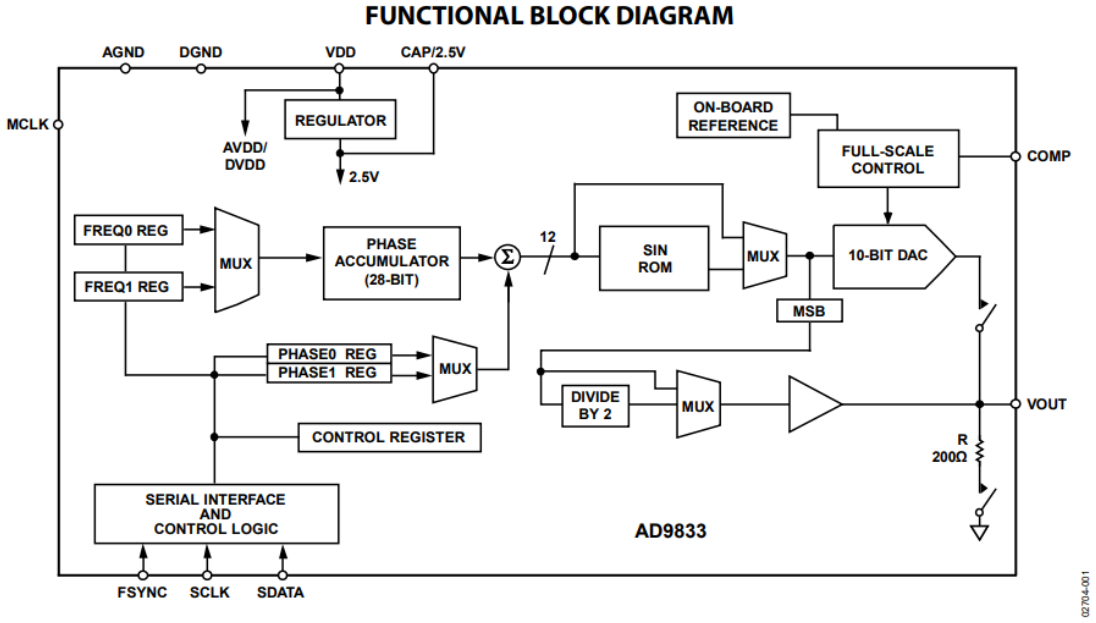


Figure 1.

Figure 2: AD9833 Block Diagram

The basic signals, viz Sinusoid, Triangle and Square are passed through a high bandwidth and high gain opamp where the amplitude can be varied upto 9.8V in real time via the trimpot's placed beside. But we limit our operation to **1 MHz** owing to the limitations of ICs such as Schmitt trigger and XOR gates used.

The following is the plot of Square and Triangle signals at 10kHz and 200kHz respectively. Here we skip the plot of Sinusoid, as this will be extensively used in the further sections. The amplitude of these signals are manually tunable by changing the resistor dividers implemented using the trimmer potentiometer's. The frequency however can simply be entered in the field of the GUI.

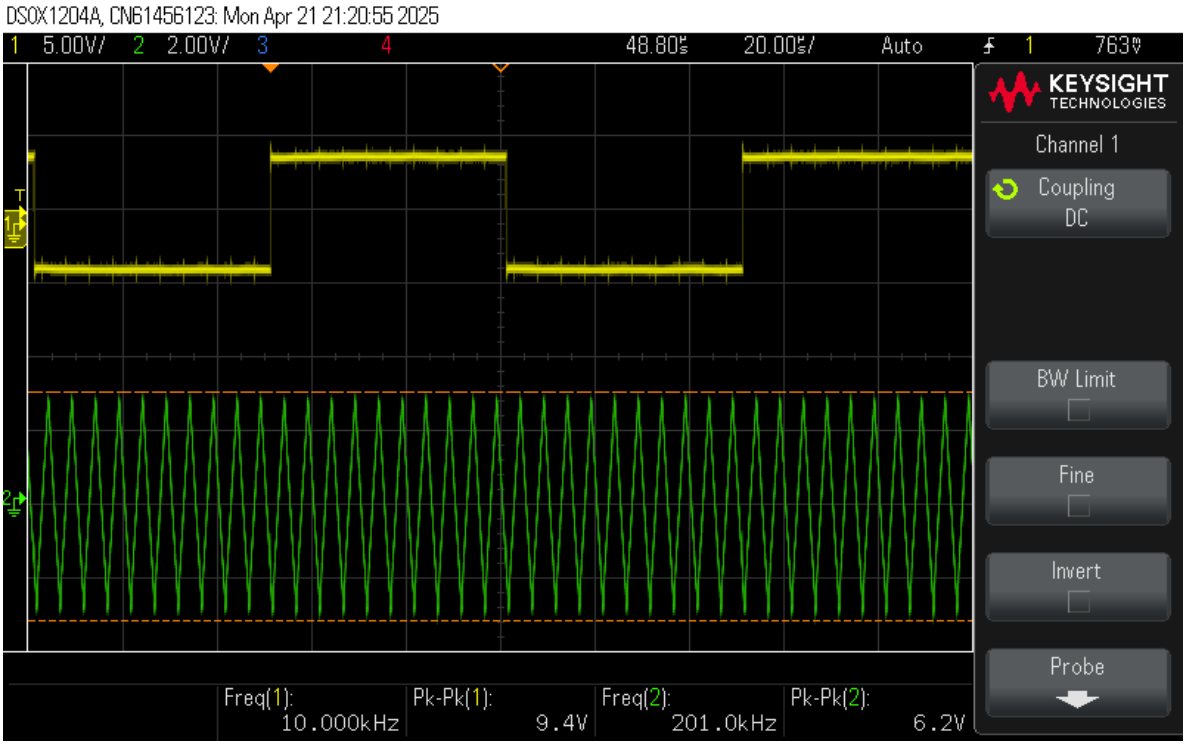


Figure 3: Square and Triangle Signals

3 Software Interface

To make the signal generation convenient, we implement a GUI (Graphical User Interface) using the *tkinter* python library. The inputs are registered by user on the computer and communicated to the ESP-32 via USB communication. The GUI features 3 tabs viz Channel-1, Channel-2 and Modulation. The first two are used to generate the basic signals of desired frequency and phase. The Modulation tab has a drop down menu where the user can select one among many digital modulation schemes and amplitude modulation. It also has fields for carrier frequency, M value, Delta(Hz or Degrees) required for FSK/PSK, Baud rate to specify rate of symbols and modulating data.

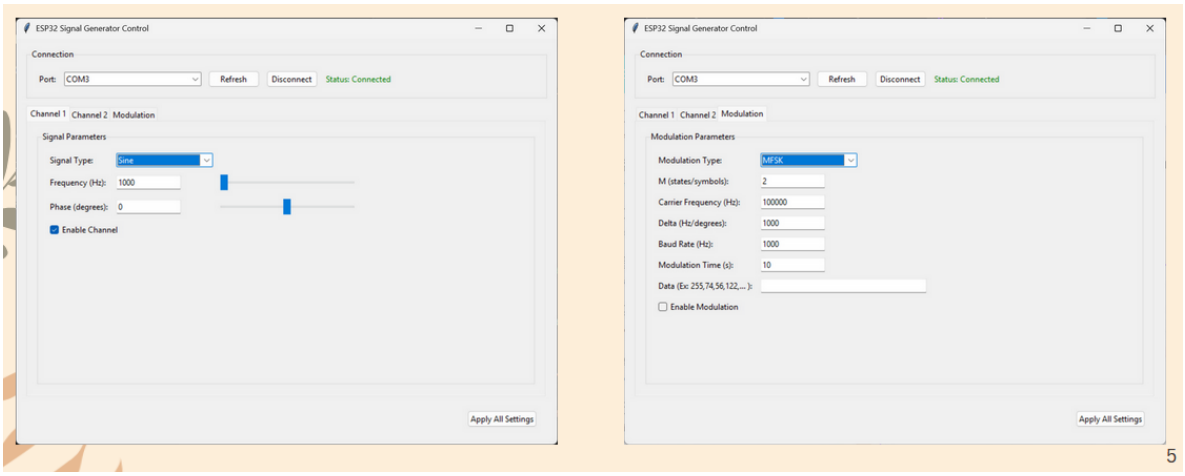


Figure 4: GUI for programming ESP-32

4 Phase Lock

We implement a phase detector circuit for locking the phase between the two channels to a desired value. For this first we pass the signal generated from the AD9833 to op-amp based amplifiers. This is necessary as the AD9833 generates only **300mV pk-pk** signals. Amplified signals are then passed to Schmitt Triger to convert them into square waves after removing DC component and offsetting them about the schmitt trigger's threshold. Then both square waves are passed through XOR gate. This generates a square wave output of twice the frequency. Consequently, the Duty cycle of the XOR output is proportional to the phase difference between the signals. A duty cycle of 100% corresponds to a phase difference of 180 whereas a duty cycle of 0% indicates that of 0 degrees.

$$Dutycycle = \frac{High\ Time}{Time\ period}$$

$$Phase\ difference = Dutycycle * 180.0$$

This XOR output is then passed on to the ESP-32 where the phase difference is calculated using measured dutycycle.

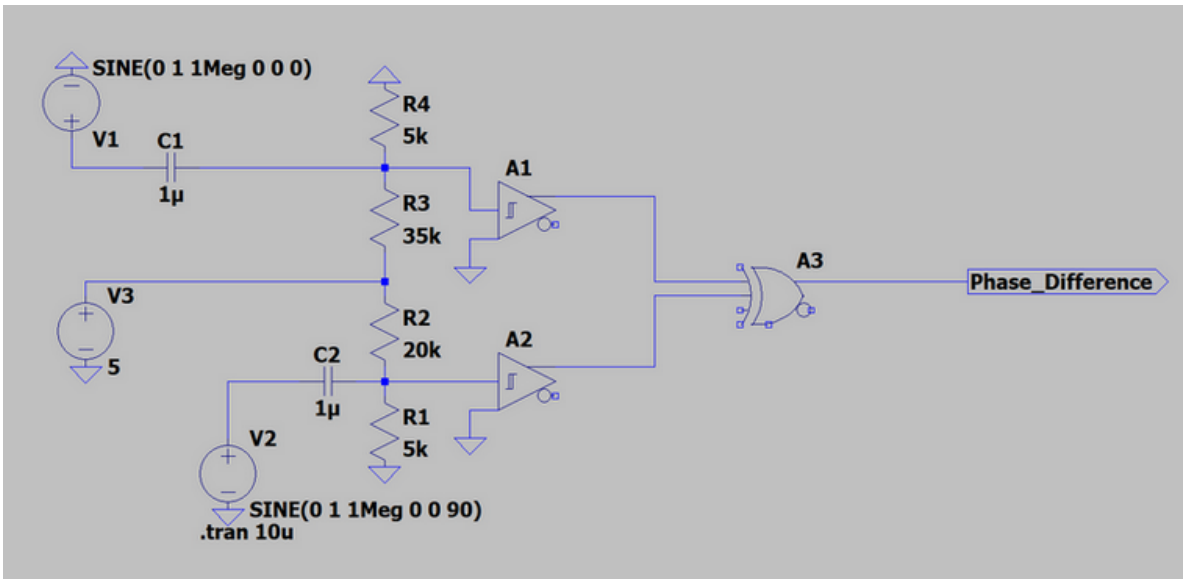


Figure 5: Circuit for Phase Comparator

The signals are delayed to obtain the desired phase difference. For this a **PD** (Proportional - Derivative) control system is used. The need to P-control is obvious so as to reduce the error (difference between measured and desired phase difference). The D-control is additionally employed to limit overshoot of the error and improves the stability of the feedback loop.
Assume the open-loop phase error (input) is of the form:

$$e(t) = \Delta\theta_1 + \Delta f \cdot t$$

This corresponds to a constant frequency offset Δf between both the signals. **PD Controller** The PD controller output is:

$$u(t) = K_p \cdot e(t) + K_d \cdot \dot{e}(t)$$

assuming that $\Delta f << $ carrier frequency

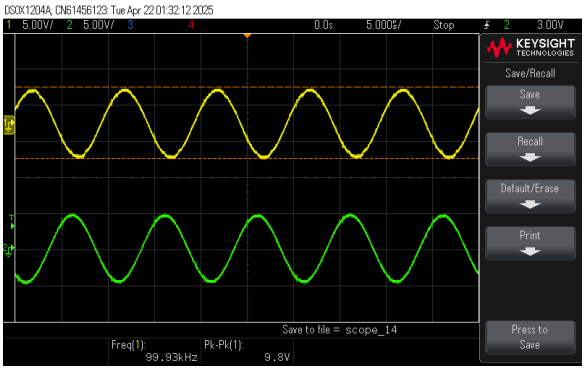
$$u(t) = K_p \cdot \Delta\theta_1 + K_d \cdot \Delta f$$

Steady-state phase error: Since u(t) is constant and independent of time, steady state error reduces to zero

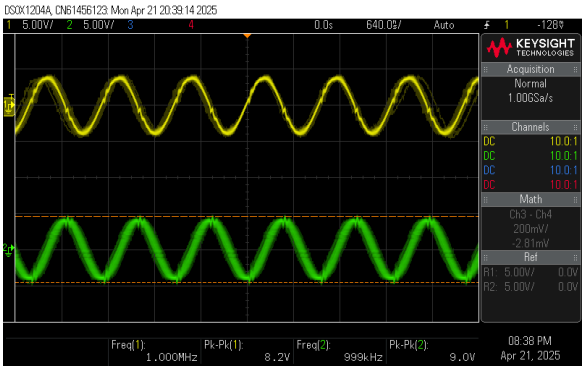
$$\lim_{t\to\infty} e(t) = 0$$

Conclusion A PD controller in a PLL ensures that, for a linearly increasing phase error (i.e., a constant frequency offset), the frequency error goes to zero. The phase of both the signals lock exactly to the specified phase frequency. But by physical observation, we noticed that the frequency error exists mainly in the crystals of both the signal generators. When these frequencies are scaled down, the Δf varies proportional to frequency. Since we set a constant derivative gain, this causes some amount of jitter and noise in the signal. Therefore, it may not be very useful to use derivative gain.

The following plots show the action of the Phase Lock. Without the feedback, one of the signal continuously appears to move w.r.t the other. This is because of the linear error is phase caused due to small innaccuracy in the frequencies of the signals. The first plot on the left locks 100KHz signals on to 180°, whereas the second plot on the right locks 1MHz signals on to 90°.



(a) 100kHz signals locked on to 180°



(b) 1MHz signals locked on to 90°

Figure 6: Phase Lock

5 Digital Modulation

Digital modulation is the process of encoding digital information onto an analog carrier signal by modifying its amplitude, frequency, or phase. It enables efficient and reliable data transmission over various communication channels, including wireless and wired systems. Common digital modulation schemes include FSK, PSK, ASK and PWM.

a) M-FSK (Frequency Shift Keying)

Frequency Shift Keying (FSK) is a digital modulation technique in which digital information is transmitted through discrete frequency changes of a carrier wave. In its simplest form, binary FSK (BFSK) uses two different frequencies to represent binary 0 and 1. More advanced forms like M-ary FSK use multiple frequencies to represent multiple bits per symbol. FSK offers better noise immunity than amplitude-based modulation schemes, making it suitable for use in wireless communication systems, modems, caller ID transmission, and radio frequency identification (RFID). Its simplicity and reliability make it ideal for low-complexity, low-power applications, especially in narrowband channels.

The following is the 8-FSK Plot. We use $f_c = 50$kHz, $\Delta f = 2.5kHz$ and a baud rate of 1kHz. We iterate through all possible input data viz. 0,1,...7. From the plot, we can clearly see the action of 8-FSK. First we see the base frequency 50kHz, and for every unit in time axis, the frequency increase by 2.5kHz, giving rise of higher frequency signals. In general any suitable carrier frequency and step frequency can be chosen to encode any input data.

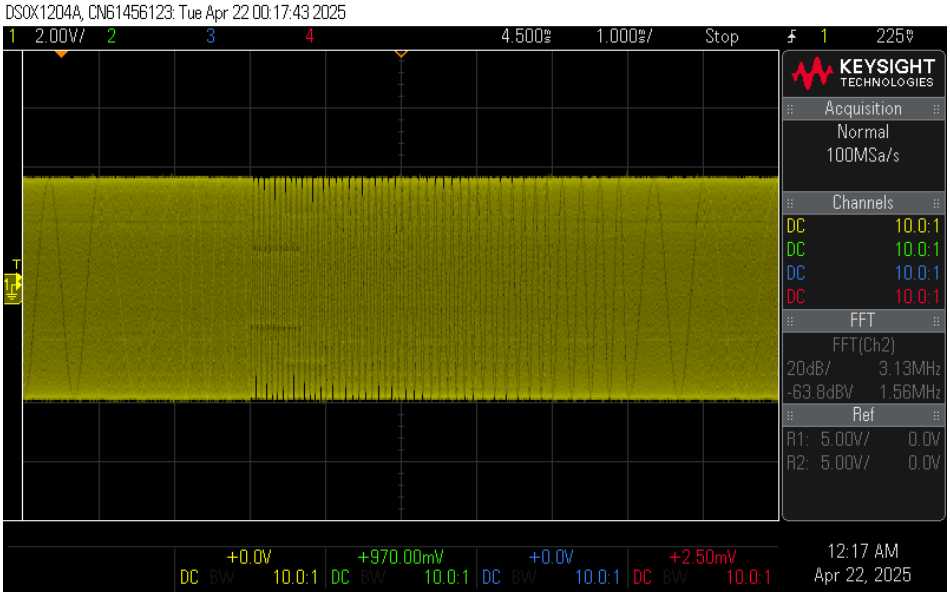
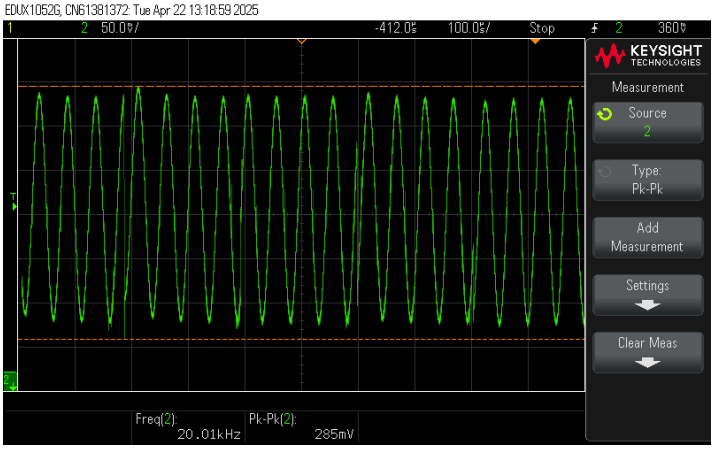


Figure 7: 8-FSK with $f_c = 50$kHz, $\Delta f = 2.5kHz$

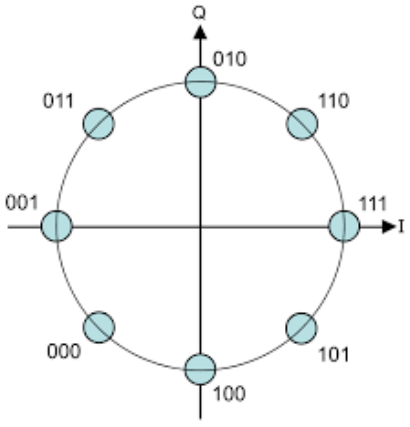
b) M-PSK (Phase Shift Keying)

Phase Shift Keying (PSK) is a digital modulation scheme that conveys data by altering the phase of a carrier signal. In its simplest form, Binary PSK (BPSK), the carrier phase is shifted between two values (usually 0° and 180°) to represent binary 0 and 1. More advanced variants like Quadrature PSK (QPSK) and M-ary PSK use four or more phase shifts to encode multiple bits per symbol, increasing data rates without increasing bandwidth. PSK is widely used in wireless communication systems, satellite links, and RFID due to its efficient bandwidth usage and robustness against noise in phase-coherent channels.

The following is the 8-PSK plot. We use $f_c = 20kHz$, $\Delta\phi = 45°$ and a baud rate of 5kHz. Similar to the previous case, we iterate through 0 to 7. With the time axis set at 200 μs, we can clearly see the change in phase after every unit in x-axis. The phase changes as per the constellation, which is **Gray Coded**. The Gray coded constellation diagram is also shown on the right.



(a) 8-PSK with $f_c = 20kHz$, $\Delta\phi = 45°$



(b) Constellation Diagram for 8-PSK

Figure 8: 8-FSK

c) ASK (Amplitude Shift Keying)

Amplitude Shift Keying (ASK) is a digital modulation technique where the amplitude of a carrier wave is varied to represent digital data. The simplest form, On-Off Keying (OOK), uses the presence of a carrier wave to represent binary 1 and its absence to represent binary 0. OOK is relied upon heavily in morse code transmissions. ASK is easy to implement and requires minimal bandwidth, but it is more susceptible to noise and signal degradation compared to phase or frequency-based modulation schemes. It is commonly used in optical communication systems, RFID, and remote control applications where simplicity and low power consumption are prioritized over robustness to interference.

The following is the plot for ASK where for a 1, we just send $cos(2\pi f_c t)$ and 0 otherwise. The following is plotted for a data sequence of 1,0,1,1,0,1,0. Corresponding to this the plot is obtained, where each time unit represents one symbol.

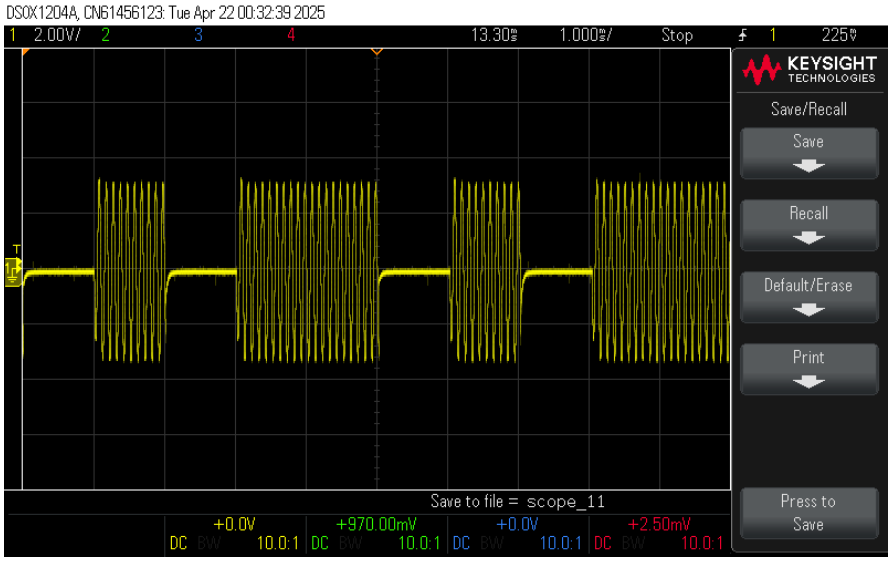
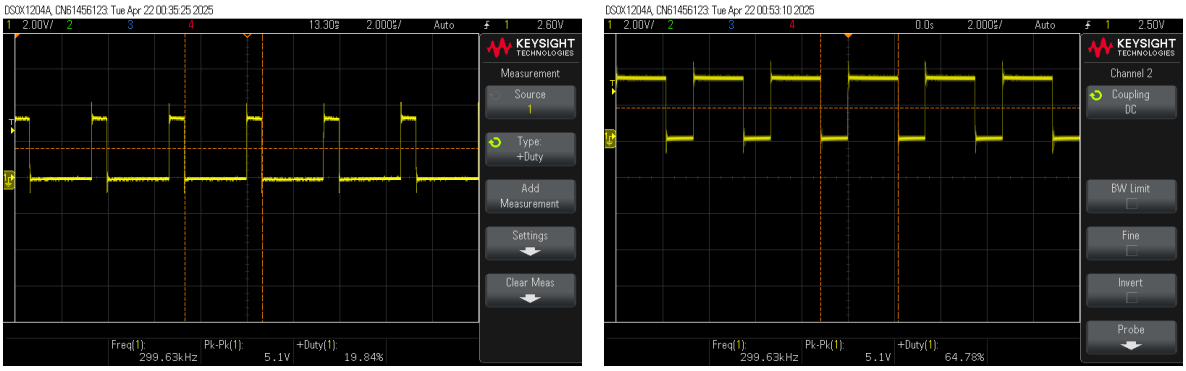


Figure 9: ASK with $f_c = 10kHz$

d) PWM (Pulse Width Modulation)

Pulse Width Modulation (PWM) is a modulation technique where the width (duration) of each pulse in a pulse train is varied in proportion to the amplitude of the modulating signal. In digital communication, PWM can represent data by encoding bits as pulses of varying widths within a fixed time period. Though not as bandwidth-efficient as other digital modulation schemes like PSK or FSK, PWM is simple to implement and offers good noise immunity. It is widely used in applications such as motor control, power regulation, audio signal generation, and LED dimming, where analog control is achieved using digital signals. The following are plots with Duty cycle of 20% and 65% respectively at a frequency of 300 KHz.



(a) Duty cycle = 65%

(b) Duty cycle = 20%

Figure 10: PWM with $f_c = 300kHz$

e) Frequency Sweep

Frequency Sweep, also known as Frequency Modulation or Chirp, involves varying the frequency of a carrier signal over time. In this modulation scheme, the frequency increases or decreases continuously within a specified range, often in a linear or exponential manner. The frequency sweep is used to encode information by mapping data to the rate or extent of frequency change. It is commonly used in radar systems, sonar, and communication systems like spread spectrum techniques, where the frequency variation provides advantages such as resistance to interference, improved signal detection, and better bandwidth utilization, especially in environments with high noise levels. It is highly useful in generating **Bode's Plot** over a wide range of frequency.

The following is the plot with base frequency of 25kHz, and then two increments of 25kHz giving us 50kHz and 75kHz. The increase in frequency can be clearly seen.

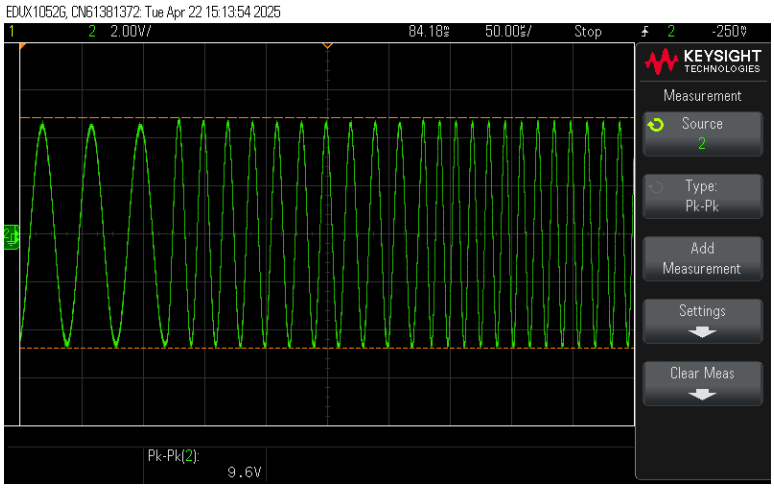


Figure 11: Frequency Sweep

6 AM (Amplitude Modulation)

Amplitude Modulation (conventional) is a modulation technique where the amplitude of a carrier signal is varied in proportion to the amplitude of the input (modulating) signal, while the frequency and phase remain constant. This modulation method is widely used in analog radio broadcasting, where the audio signal modulates the carrier wave to produce a signal that can be transmitted over long distances. AM is relatively simple to implement but is more susceptible to noise and interference, as these affect the amplitude of the signal. Despite this, AM remains popular in communication systems due to its ease of use and low complexity. In contrast to DSB-SC, in AM, we also add a carrier component, which makes the demodulation simpler at the cost of lower power efficiency.

Here we use *AD633JN* analog multiplier IC for performing AM as shown in the following circuit diagram. This IC is based on 4-Quadrant Multiplier where both the input signals can take both positive and negative values, providing good flexibility. The output is of course bipolar too.

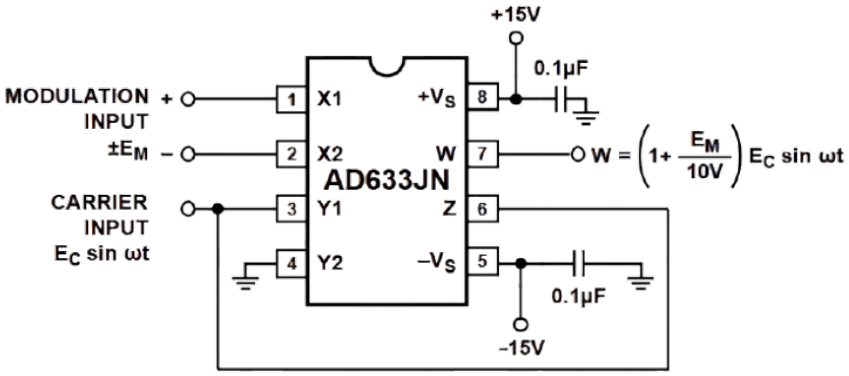


Figure 12: Circuit Diagram for Multiplier

We also provide the function of **variable modulation index**. This can simply done by changing the amplitude of either the message or carrier signal. This can be done by just changing the resistor divider ratio in the corresponding op-amp amplifiers. The following are the plots for AM

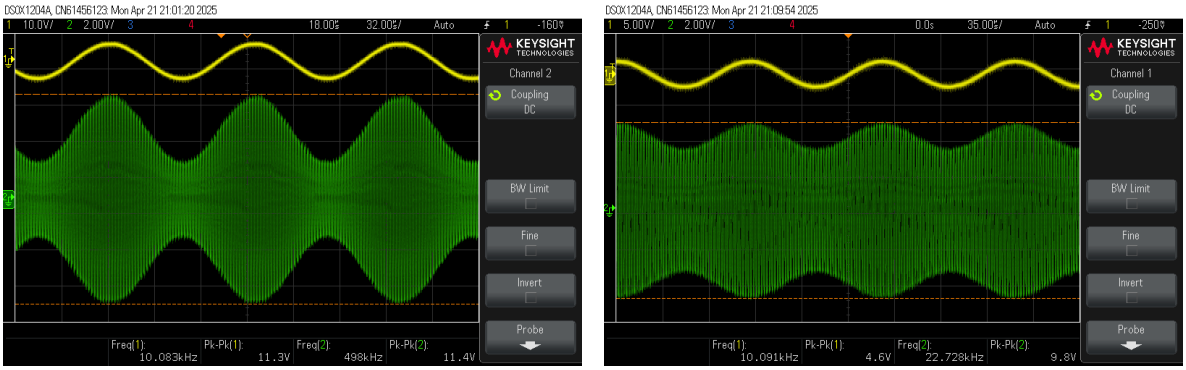


Figure 13: AM with $f_c = 500kHz$, $f_m = 10kHz$ with different modulation indices

The following is the FFT plot of the AM signal. We can clearly see the peaks at 490, 500 and 510 kHz. Also due to the inherent non-linearlity in the circuits, there exists multiple harmonics of the fundamental band of frequencies. To eliminate this, we additionally add a simple RC Low Pass Filter designed for a carrier of 500kHz. This attenuates tha harmonics further by more than **30dB** relative to the desired band.

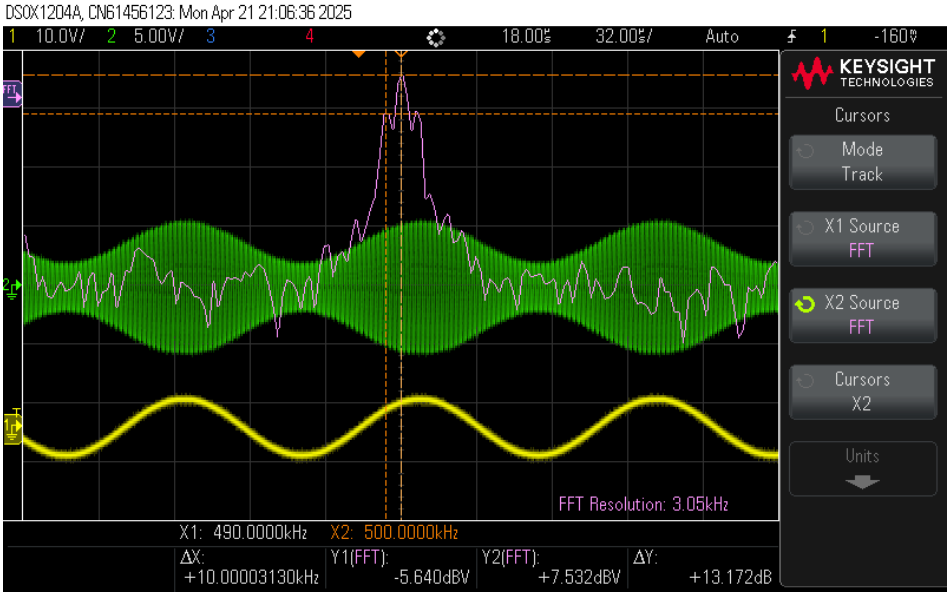


Figure 14: FFT Plot of the AM signal

Also, in the final stage, we also have a 3:1 Multiplexer to choose between three different signals. These are the Digital Modulation, PWM (coming from ESP-32) and the AM signal (from mixer). We assert the 2 bit select signals from the ESP-32 and feed them into the mux. This makes viewing the signals convenient.

7 Specifications Sheet

Following are the specifications achieved by prototype signal generator. We know that shifting between registers for binary modulations takes around 39μs and to change value of phase register directly for higher MPSK takes 40μs. Also to change the value of frequency register for higher MFSK takes around 114μs. These determine the minimum time period for symbol rate as this much time is required to change the generated symbol. This limits our maximum baud rate.

$$Baud\ Rate = \frac{Symbols}{Time\ (s)}$$

$$Data\ Rate = Max.\ Baud\ Rate\ *\ log_2 M\ (b/s)$$

The Max Freq is limited by the AD9833 IC.

Wave	Vpp	Max Freq	Min Freq	Max Baud (MB)	Speed
Sine	0.4-9.8	3MHz	2000Hz		
Square	0.4-9.8	3MHz	2000Hz		
Triangle	0.4-9.8	3MHz	2000Hz		
BFSK	0.4-9.8	3MHz	2000Hz	25000	25Kbps
BPSK	0.4-9.8	3MHz	2000Hz	25000	25Kbps
MFSK	0.4-9.8	3MHz	2000Hz	8000	MB*log2M Kbps
MPSK	0.4-9.8	3MHz	2000Hz	25000	MB*log2M Kbps
ASK	0.4-9.8	3MHz	2000Hz	25000	25Kbps
Sweep	0.4-9.8	3MHz	2000Hz		
PWM	0.4-9.8	5MHz	1Hz	200000	
AM	0.4-9.8	3MHz			

Figure 15: Modulator Specifications

The following are the specs for the PWM generated by the ESP-32, the duty step is better with lower frequency and higher timer resolution. The ESP has a reference crystal of 240 MHz which is pre-scaled to 80 MHz which is used as a reference to generate PWM signal. The higher the frequency, the lesser is the division ratio and therefore the counter generating PWM is not able to provide a high dutycycle resolution(as the amount of clock cycles to be counted reduce). Therefore we notice that with lower frequency we achieve a better dutycycle resolution.

RESOLUTION	MAX FREQ	MIN FREQ	DUTY STEP %
4 BIT	5 MHz	62	6.250
5 BIT	2.5 MHz	31	3.125
6 BIT	1.25 MHz	16	1.563
7 BIT	626 KHz	8	0.781
8 BIT	313 KHz	4	0.391
9 BIT	156 KHz	2	0.195
10 BIT	78 KHz	1	0.098
11 BIT	39 KHz	1	0.049
12 BIT	19 KHz	1	0.024
13 BIT	9.7 KHz	1	0.012
14 BIT	4.8 KHz	1	0.006
15 BIT	2.4 KHz	2	0.003
16 BIT	1.1 KHz	1	0.0015
17 BIT	611 Hz	1	0.00076
18 BIT	305 Hz	2	0.00038
19 BIT	152 Hz	1	0.00019
20 BIT	76 Hz	1	0.000095

Figure 16: PWM Specifications

8 Demo Video

Youtube video Link - Click here

9 Conclusion

We have designed and achieved a signal generator which supports a variety of features over a wide range of frequency, tunable signal amplitude and variable modulation parameters. We successfully demonstrated various modulations and signals which make this a feasible and worthy product at such a competitive low price. But there is future scope of improvement as mentioned below:-

- Adding offset functionality is future scope.
- Improved timing precision in modulated signals.
- Improve minimum frequency limitation.