॥ सा विद्या या विमुक्तये ॥

भारतीय प्रौद्योगिकी संस्थान धारवाड

Indian Institute of Technology Dharwad

Indian Institute of Technology, Dharwad
CS-311: Lab Report

Assignment-4: Pipelined processor with interlocks

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1 Introduction

In this assignment, we have simulated the 5-stage pipelined processor using Java. The pipelines now have interlocks and thus, each stage executed 1 instruction in 1 cycle. This is a major improvement since last assignment where there was no simultaneous execution of instructions.

2 Tabulation of Observations

Object File	No. of Instructions	No. of Cycles
evenorodd.asm	15	19
prime.asm	74	83
palindrome.asm	155	166
fibonacci.asm	144	164
descending.asm	824	916

3 Comments on Observations

In the previous assignment, a single-cycle processor was utilized, wherein each instruction technically consumed five times the time taken in the current assignment. However, the cycle count of programs dropped only around half when they are run on pipelined processor as compared to the non-pipelined processor.This can be attributed mainly due to the processor's handling of RAW (Read After Write) and control hazards, where bubbles are added that consume some amount of time in each cycle till the hazard exists. More the number of hazards faced, more is its deviation from ideal pipelined processor performance.

4 Scope for Further Improvement

The processor can be further enhanced by implementing forwarding techniques, which would lead to a reduction in the number of bubbles. This improvement would optimize the processor's performance by minimizing delays caused by data hazards, consequently enhancing overall efficiency.