Samarth Sharma

Major: Electrical Engineering
Minors: Industrial & Management Engineering, English Literature
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Samarth Sharma| samarthsb23

Academic Qualifications

Year	Degree/Certificate	Institute	CPI/%
2023-Present	Bachelors of Technology	Indian Institute of Technology Kanpur	**8.5**/10
2023	CBSE(XII)	Hope Hall Foundation School (HHFS), Delhi	**96.8**%
2021	CBSE(X)	Delhi Public School, Prayagraj	**97.4**%

Scholastic Achievements

- Incoming **Hardware/Silicon Engineering Intern** at **Google India** for **Summer 2026**.
- Secured an **All India Rank** of **1082** in the **Joint Entrance Examination (Advanced)**, 2023 among 200,000 candidates.
- Secured an **All India Rank** of **954** in the **Joint Entrance Examination (Main)**, 2023 among 1.2 million candidates.
- Awarded '**Outstanding Achievement in Academics**' for placing second overall in school in CBSE XII Boards. (2022-23)

Internship Experience

Radar Signal Processing on Zynq SoCs for Doppler Estimation | Prof. Sumit J. Darak | IIIT Delhi *(May'25-Present)*

Objective	• To accelerate and compare classical and **deep-learning-aided** doppler estimation algorithms to evaluate latency–resource trade-offs in real-time **radar systems** on **FPGAs** of **Zynq-SoCs** (**Pynq-Z2** and **ZCU111**).
Approach	• Developed custom **HLS IPs** and integrated **PYNQ** drivers via **Vivado** block design using **AXI4** interfaces. • Implemented **MUSIC** and **ESPRIT** as **Vitis HLS** IPs with resource optimizations like **word-length tuning**. • Benchmarked HLS design pragmas like **pipeline, unroll,** and **array partitioning** using **synthesis reports**. • Compared performance of single, double-precision float and fixed data types for **Doppler-separated targets**. • Integrated **deep neural networks** (DNNs) to boost accuracy under coherent sources and array miscalibration. • Used **Integrated Logic Analyzers** to debug AXI transactions and verify dataflow correctness on hardware.
Impact	• **Co-authoring two research manuscripts**, including one submitted to **IEEE RadarConf 2026**. • Achieved up to **4x acceleration** over NumPy in FPGA-accelerated matrix multiplication on ZCU111. • Created a **4-part YouTube tutorial series** on HLS-to-PYNQ design flow and benchmarking on **Vitis 2024.2**. • Attained a **30x acceleration** over NumPy for reliable Doppler estimation using MUSIC and ESPRIT. • Achieved **15x improvement** using MLP and CNN based architectures over classical Pytorch/NumPy ESPRIT.

Research Publications

- *Reconfigurable Low-Complexity Architecture for Doppler Velocity Estimation of Tightly-Spaced Mobile Users in ISAC* (Co-authors: A. Tewari, S. J. Darak, S. S. Ram), Submitted to **IEEE RadarConf 2026** (Under Review).

Research Projects

Transistor-Level Duty Cycle Correction Circuit on Cadence Virtuoso | Prof. Chithra | IIT Kanpur *(May'25-Jun'25)*

- Designed a **transistor-level** duty cycle correction circuit in **gpdk-180nm** CMOS technology on **Cadence Virtuoso**.
- Implemented a **bidirectional shift register (BSR)** and **XOR-delay-DFF** based feedback loop for adaptive convergence.
- Achieved a corrected duty cycle of **48–52%** for **0.5–1 GHz** inputs, starting from initial distortions ranging between **30–70%**.

Semiconductor Device Modeling using DEVSIM TCAD | Prof. Rituraj | IIT Kanpur (*Dec'24-Feb'25*)

- Explored **DEVSIM TCAD** framework, including device setup, **meshing**, and model definition using Python scripting.
- Simulated 1D **p-n junction diode** using **drift-diffusion** equations; analyzed **IV behavior** and **carrier** dynamics.
- Explored solver mechanics, **convergence** behavior via **Newton's method**, and visualized results using **Matplotlib**.

Technical Skills

Programming Languages: Verilog HDL, C, C++, Python, LaTeX; **Libraries:** NumPy, Pandas, Matplotlib, PyTorch, Scikit-learn; **Software:** Xilinx Vitis HLS, Vivado, Cadence Virtuoso, MATLAB, MicroCap, GNU Octave, Devsim TCAD

Relevant Courses

*: A (10/10) #: PG level elective *o*: Online Course

Electronics	Computer Science	Mathematics	Electrical and Physics
VLSI System Design#	Data Structures and Algorithms	Probability and Statistics	Communication Systems
Digital Electronics	Fundamentals of Computing	Complex Variables*	Signals, Systems and Networks
Microelectonics-I,II	Harvard's CS50x*o	Partial Differential Eqns	Quantum Physics
Chip-Based VLSI Design*o	Machine Learning*o	Differential Equations*	Classical Electrodynamics
Spin-Electronics Devices#*	Natural Language Processing*o	Linear Algebra	Control Systems

Positions of Responsibility (PoRs) and Volunteering

- **Academic Department Mentor, EE** - UG Academics Wing, Academics and Career Council, IITK (2025-26 tenure).
- **Academic Mentor**- Institute Counselling Service (ICS), IITK (2024-25 tenure): Mentored ∼**500** first-year students in **Quantum Physics** (PHY114) by conducting remedial sessions and providing personalized academic support and guidance.
- **Secretary**, Debating Society (DebSoc), IIT Kanpur (2024-25 tenure): Assisted in organizing flagship **national-level** debating tournaments like *IITK APD'24* (online) and *IITK BPD'25* (offline); **led marketing** efforts for *IITK APD'24*.
- **Volunteer**- National Service Scheme (NSS), IIT Kanpur (2023-24). Contributed in the field of **education** for socio-economically underprivileged youth by translating physics lectures into regional languages to increase accessibility.