Samarth Sharma Bhardwaj

Second Year Undergraduate (Sophomore)
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Research Statement

Sophomore at IIT Kanpur passionate about **Digital VLSI, FPGA Acceleration, and Embedded Systems**. Experienced in **Verilog-based digital design, RTL implementation, and high-level synthesis (HLS) for FPGA applications**. Currently working on **hardware acceleration of radar signal processing on Zynq SoC**, optimizing signal processing pipelines for real-time embedded systems. Eager to apply my skills in **circuit optimization, mixed-signal VLSI, and semiconductor design**.

Academic Qualifications

Year	Degree/Certificate	Institute	CPI/%
2023 - Present	B.Tech	Indian Institute of Technology, Kanpur	8.5/10.0
2023	CBSE(XII)	Hope Hall Foundation School (HHFS), Delhi	96.8%
2021	CBSE(X)	Delhi Public School, Prayagraj	97.6%

Scholastic Achievements

- Secured **All India Rank 1082** in **JEE Advanced 2023** among 200,000 shortlisted candidates.
- Secured **All India Rank 954** in **JEE Mains 2023** ($\sim$ 99.926 percentile) among 1.5 million registered candidates.
- Awarded Academic Excellence Award for exceptional academic performance in Class XII board exams and JEE, HHFS, Delhi
- Awarded Academic Excellence Award - Merit for exceptional academic performance in the session 2019-20, DPS, Udhampur
- **Positions of Responsibility** - i. Secretary, Quiz Club, IITK (2024-25) ii. Secretary, Debating Society IITK (2024-25)
- **Academic Mentor** of PHY114 (Quantum Physics) under the Institute Counseling Service. Mentored freshmen and taught remedial classes to guide them throughout their first year. (2024-25 Tenure)

Key Projects

- **FPGA-Based Radar Signal Processing on Zynq SoC** (*Mar'25- Present*)
  Research Intern, IIIT Delhi (Prof. Sumit J. Darak, Dept of ECE, IIITD)
  - Designed and implemented **high-performance FPGA architectures** for radar signal processing using **Xilinx Vivado HLS & Verilog RTL**.
  - Accelerated signal processing algorithms by translating C-based models into hardware-optimized Verilog using **HLS-based DSP pipelines**.
  - Integrated **HLS-generated modules with ARM-based embedded processing** on **Xilinx Zynq SoC**, leveraging **AXI interfaces** for efficient data transfer.
  - Optimized resource utilization, power consumption and latency for real-time radar applications.
  - Developed **Python-based driver software** to test and verify hardware performance.
- **Developing sensitive and efficient photodetectors at RT** (*Dec'24- Present*)
  Prof. Rituraj, Dept of EE, IIT Kanpur
  - Led the **simulation and analysis of device behavior** using **DEVSIM TCAD**, rigorously testing IV characteristics to identify optimal material configurations to help develop efficient **SPADs** with high EQE and low DCR at RT.
  - Identified a critical gap in DEVSIM's capabilities and initiated an effort to **develop and integrate avalanche functionality** into its open-source framework, significantly expanding its capabilities for advanced semiconductor research.
  - Spearheading the implementation of **impact ionization modeling** to improve accuracy in photodetector simulations, contributing directly to the open-source semiconductor community.
- **Audio Classification and Signal Processing using Deep Learning** (*Dec'24- Feb'25*)
  Electrical Engineers' Association, IIT Kanpur
  - Engineered a deep learning pipeline using CNNs and RNNs to classify and detect **deepfake audio**, achieving **>80% accuracy.**
  - Conducted in-depth feature extraction, leveraging **MFCCs** and **chroma features** to enhance model robustness against noise and variations in speech patterns.
  - Optimized hyperparameters and network architectures to improve classification performance, achieving a balance between precision and recall.

- **Fact Filter using NLP** (*May'24- Jul'24*)
  Public Policy and Opinion Cell, IIT Kanpur
  - Developed an advanced **NLP-based classification model** to reliably differentiate between authentic and fraudulent news articles, reducing misclassification rates.
  - Trained and fine-tuned models using **state-of-the-art NLP techniques**, extracting key linguistic and contextual features to enhance accuracy.
  - Applied machine learning on real-world datasets, iteratively refining the model to improve generalization across diverse news sources.
- **DIGIWARE- Digital Design using Verilog** (*Dec'23- Jan'24*)
  Electrical Engineers' Association, IIT Kanpur
  - Designed and implemented **multiple real-world digital systems** using **Verilog HDL**, including a smart car parking system, customized alarm clock, and traffic light controller.
  - Explored and optimized various Verilog modules for efficient **RTL design and digital logic synthesis**.
  - Built a foundational understanding of hardware description languages (HDLs) and their application in digital system design.

Technical Skills

- **Programming Languages:** C, C++, C#, Verilog HDL, Python, SQL, HTML/CSS, JavaScript, LaTeX, Django, Flask
- **Software and Libraries:** Git, Xilinx Vivado, Vitis, Vivado HLS, Arduino IDE, Unity, DEVSIM TCAD, MATLAB, SPICE, AutoCAD, Inventor, Fusion360

Relevant Courework

Analog Electronics and Control Systems	Spin Electronic Devices
Machine Learning Specialization (Stanford Online)	Chip Based VLSI Design Specialization
Data Structures and Algorithms, Fundamentals of Computing	Harvard's CS50x 2023
Probability & Statistics, Complex Variables and PDEs	Introduction to Electronics (Theory and Lab)

Extra-Curricular Activities and Recognitions

- **Volunteer in National Service Scheme, IITK**: Mentors- *Prof. Niraj M. Chawake, Prof. Manoj K. Harbola, IIT Kanpur.* Worked in the field of education of socio-economically underprivileged children and youth. Translated Prof. Harbola's PHY114 lectures into Hindi for wider accessibility in local schools and colleges.
- Represented IIT Kanpur in various debating tournaments including SBS'PD 2024 (Debating Society, IIT Kanpur)
- Represented Hall-12 in the Inter Hall Fresher's technical competition Takneek'23, IIT Kanpur in Game Development. *(Aug'23)*
- Won Best Delegate in e-MUN held at DPS, Prayagraj in 2020.
- Won Bilingual Turncoat held in DPS Udhampur's Unison consecutively in 2019 and 2020, delivered speeches in English & Sanskrit.