Samarth Sharma Bhardwaj

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Academic Qualifications

Year	Degree/Certificate	Institute	CPI/%
2023-Present	B.Tech-Electrical Engineering	Indian Institute of Technology Kanpur	**8.5**/10
2023	CBSE(XII)	Hope Hall Foundation School (HHFS), Delhi	**96.8**%
2021	CBSE(X)	Delhi Public School, Prayagraj	**96.5**%

Scholastic Achievements

- Secured an **All India Rank** of **1082** in the **Joint Entrance Examination (Advanced)**, 2023 among 200,000 candidates.
- Secured an **All India Rank** of **954** in the **Joint Entrance Examination (Main)**, 2023 among 1.2 million candidates.
- Awarded '**Outstanding Achievement in Academics**' for placing second overall in school in CBSE XII Boards. (2022-23)

Internship Experience

FPGA based Radar Signal Processing on a Zynq SoC | Prof. Sumit J. Darak | IIIT Delhi *(Apr'25 - Present)*

Objective	• To accelerate classical and **deep-learning-aided** direction-of-arrival (**DoA**) estimation algorithms to evaluate latency–resource trade-offs in real-time **radar systems** on **Zynq-SoCs** (**Pynq-Z2** and **ZCU111**).
Approach	• Developed custom **HLS IPs** and integrated **PYNQ** drivers via **Vivado** block design using **AXI4** interfaces. • Implemented **MUSIC** and **ESPRIT** as **Vitis HLS** IPs with optimizations like **word-length tuning**. • Benchmarked HLS design pragmas like **pipeline, unroll,** and **array partitioning** using **synthesis reports**. • Compared performance of single, double-precision float and fixed data types for **Doppler-separated targets**. • Integrated **deep neural networks** to boost DoA accuracy under coherent sources and array miscalibration. • Used **Integrated Logic Analyzers** (ILAs) to debug AXI transactions and verify correct dataflow on hardware.
Impact	• Achieved up to **4x acceleration** over NumPy in FPGA-accelerated matrix multiplication on ZCU111. • Created a **4-part YouTube tutorial series** on HLS-to-PYNQ design flow and benchmarking on **Vitis 2024.2**. • Attained a **30x acceleration** over NumPy for reliable DoA estimation using MUSIC and ESPRIT.

Key Projects

Transistor-Level Duty Cycle Correction Circuit on Cadence Virtuoso | Prof. Chithra | IIT Kanpur *(May'25-Jun'25)*

Objective	• To design a **transistor-level** all-digital duty cycle correction circuit in **gpdk-180nm CMOS** technology.
Approach	• Designed using **gpdk180**, with a XOR–delay–DFF loop and a bidirectional shift-register–based duty detector. • Built **transistor-level** schematic and testbench in **Virtuoso** to analyze delay loop under skewed inputs.
Impact	• Achieved **48–52%** corrected duty cycle for **0.5–1GHz** inputs with initial duty distortion between 30–70%.

Simulation of High-Efficiency Photodetectors in DEVSIM TCAD | Prof. Rituraj | IIT Kanpur (*Dec'24-Mar'25*)

Objective	• To simulate and analyze **single-photon avalanche diodes** (SPADs) targeting high EQE and low DCR at RT.
Approach	• Studied **quantum photonics** and **nanophotonics** literature to evaluate material/design strategies. • Simulated standard semiconductor devices (diodes, MOSFETs) in **DEVSIM TCAD** and evaluated IV behavior.
Impact	• Initiated integration of **avalanche modeling** into DEVSIM to support open source SPAD modeling.

Audio Classification and Signal Processing using Deep Learning | Electrical Engineers' Association *(Dec'24-Feb'25)*

- Built a **CNN**-based model for deepfake audio detection leveraging **MFCC** and **chroma features** for spectral analysis.
- Tuned architectures and hyperparameters for robust classification under noise and speech variation, achieving **85%** accuracy.

DIGIWARE- Digital Design using Verilog HDL | Electrical Engineers' Association *(Dec'23-Jan'24)*

- Modeled and verified **combinational** and **sequential** logic, like **FSMs** and **counters**, in **Verilog HDL** and **GTKWave**.
- Designed and simulated complex **digital systems** like a car parking system, alarm clock, and traffic controller in Verilog.

Technical Skills

Programming Languages: C, C++, Python, Verilog HDL, LaTeX; **Libraries:** NumPy, Pandas, Matplotlib, PyTorch, Scikit-learn; **Software:** Xilinx Vitis HLS, Vivado, Cadence Virtuoso, MATLAB, Devsim TCAD, LTspice

Relevant Courses

*: A (10/10) #: PG level elective *o*: Online course

Electronics	Computer Science	Mathematics	Others
Analog Electronics	Data Structures and Algorithms	Probability and Statistics	Control Systems
Chip-Based VLSI Design^{o}	Fundamentals of Computing	Complex Variables*	Signals, Systems and Networks
Spin-Electronics Devices$^{\#*}$	Harvard's CS50x^{o}	Partial Differential Eqns	Quantum Physics
Introduction to Electronics	Machine Learning^{o}	Ordinary Differential Eqns*	Classical Electrodynamics
		Linear Algebra	Introduction to Management*

Positions of Responsibility (PoRs) and Volunteering

- **Academic Mentor**- Institute Counselling Service (ICS), IITK (2024-25 tenure): Mentored **500+** first-year students in **Quantum Physics** (PHY114) by conducting remedial sessions and providing personalized academic support and guidance.
- **Secretary**, Debating Society (DebSoc), IIT Kanpur (2024-25 tenure): Assisted in organizing flagship national-level debating tournaments like *IITK APD'24* (online) and *IITK BPD'25* (offline); **led marketing** efforts for *IITK APD'24*.
- **Volunteer**- National Service Scheme (NSS), IIT Kanpur (2023-24). Contributed in the field of **education** for socio-economically underprivileged youth by translating physics lectures to regional languages to increase accessibility.