Samarth Sharma Bhardwaj

Third Year Undergraduate | samarthsb23@iitk.ac.in | +91-8791757203 | Samarth Sharma B. | samarthsb23

Academic Qualifications

Year	Degree/Certificate	Institute	CPI/%
2023-Present	B.Tech-Electrical Engineering	Indian Institute of Technology Kanpur	**8.5**/10
2023	CBSE(XII)	Hope Hall Foundation School (HHFS), Delhi	**96.8**%
2021	CBSE(X)	Delhi Public School, Prayagraj	**96.5**%

Scholastic Achievements

- Secured **All India Rank 1082** in **JEE Advanced 2023** among 200,000 shortlisted candidates.
- Secured **All India Rank 954** (top 0.074%) in **JEE Mains 2023** out of 1.2 Million candidates.
- Awarded '**Outstanding Achievement in Academics**' for placing second overall in school in CBSE XII Boards. (2022-23)

Internship Experience

FPGA based Radar Signal Processing on a Zynq SoC | Prof. Sumit J. Darak | IIIT Delhi *(Apr'25 - Present)*

Objective	• To accelerate classical and **deep-learning-aided** direction-of-arrival (**DoA**) estimation algorithms to evaluate performance–efficiency trade-offs in real-time **radar systems** on **Zynq-SoCs** (**Pynq-Z2** and **ZCU111**).
Approach	• Developed custom **HLS IPs** and integrated **PYNQ** drivers via **Vivado** block design using **AXI4** interfaces. • Implemented **MUSIC** and **ESPRIT** as **Vitis HLS** IPs with optimizations like **word-length tuning**. • Benchmarked HLS design pragmas (**pipeline, unroll, array partitioning**, etc.) using **synthesis reports**. • Evaluated the performance of single vs double-precision float for **Doppler-separated targets**. • Integrated **deep neural networks** to boost DoA accuracy under coherent sources and array miscalibration. • Used **Integrated Logic Analyzers** (ILAs) to debug AXI transactions and verify correct dataflow on hardware.
Impact	• Achieved up to **4x acceleration** over NumPy in FPGA-accelerated matrix multiplication. • Created a **4-part YouTube tutorial** on HLS-to-PYNQ design flow and benchmarking. • Attained a **30x acceleration** over NumPy for reliable DoA estimation using MUSIC and ESPRIT.

Key Projects

Transistor-Level Duty Cycle Correction Circuit on Cadence Virtuoso | Prof. Chithra | IIT Kanpur *(May'25 - Jun'25)*

Objective	• To design a **transistor-level CMOS** duty cycle correction circuit for **high-frequency** clock signals.
Approach	• Designed using **gpdk180**, with a XOR–delay–DFF loop and a bidirectional shift-register–based duty detector.
Impact	• Achieved **48–52%** corrected duty cycle for **0.5–1GHz** inputs with initial duty distortion between 30–70%.

Simulation of High-Efficiency Photodetectors in DEVSIM TCAD | Prof. Rituraj | IIT Kanpur (*Dec'24-Mar'25*)

Objective	• To simulate and analyze **single-photon avalanche diodes** (SPADs) targeting high EQE and low DCR at RT.
Approach	• Studied **quantum photonics** and **nanophotonics** literature to evaluate material/design strategies. • Implemented SPAD models in **DEVSIM TCAD** and analyzed IV behavior across configurations.
Impact	• Initiated integration of **avalanche modeling** into DEVSIM to support open source SPAD modeling.

Audio Classification and Signal Processing using Deep Learning | Electrical Engineers' Association *(Dec'24-Feb'25)*

- Built a **CNN** based model for deepfake audio detection using **MFCC** and **chroma features**, achieving **85%** accuracy.
- Tuned architectures and hyperparameters for robust classification under noise and speech variation.

DIGIWARE- Digital Design using Verilog HDL | Electrical Engineers' Association *(Dec'23-Jan'24)*

- Designed and simulated digital systems in **Verilog HDL**, including a car parking system, alarm clock, and traffic controller.
- Learned **digital design** fundamentals and Verilog syntax through structured assignments and practical projects.

Technical Skills

Programming Languages	Libraries	Software
C , C++ , Python, Verilog HDL, LaTeX	Numpy, Pandas, Matplotlib, PyTorch, Scikit Learn	Xilinx Vitis, Vivado, Cadence Virtuoso, MATLAB, Devsim TCAD

Relevant Courses

* -**A** (10/10) or equivalent #-**PG level elective**

Electronics & EE	Computer Science	Mathematics
Analog Electronics	Data Structures and Algorithms	Probability & Statistics
Chip-Based VLSI Design	Fundamentals of Computing	Complex Variables*
Spin-Electronic Devices#*	Harvard's CS50x	Partial Differential Eqns
Control Systems	Machine Learning*	Ordinary Differential Equations*
Introduction to Electronics		Linear Algebra

Positions of Responsibility (PoRs) & Volunteering

- **Academic Mentor** - Quantum Physics - Institute Counselling Service (ICS), IITK (2024-25 tenure).
- **Secretary**, Debating Society, IIT Kanpur (2024-25 tenure).
- **Volunteer**- National Service Scheme (NSS), IIT Kanpur - Vertical: Education (2023-24)