Lab 1

Zynq SOC
- PS → Processing system (ARM Cortex CPU)
- PL → Programmable logic (FPGA)

Accelerator :- Custom IP that offloads work from main CPU and does it repeatedly in a FPGA and gives it back to the CPU to save time (CPU can parallely do other computations)

Generate input data (random)

⇓

Send data to accelerator (PL)
using AXI DMA (MM2S)

⇓

Accelerator Processes data

⇓

Recive processed data (PL to PS)
using AXI DMA (S2MM)

⇓

Verify & Print

AXI stream → like a conveyer belt.

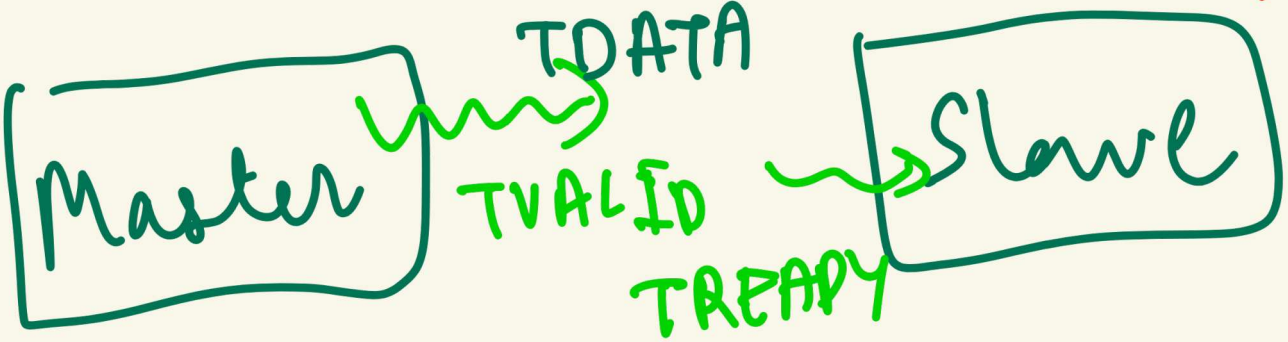
Continuous stream of data

MM2S : memory mapped to stream

(PS → AXI stream)

S2MM : stream to memory mapped

(AXI → back to DDR (PS))



TVALID → Master dictates

TREADY → Slave

Both need to be 1 for TDATA to flow.

(Handshaking)

TLAST → marks last data in a packet. (good for continuous data)

CPU → uses DDR (double data rate memory) [external RAM]