PROJECT REPORT ON

DESIGN OF TRANSMISSION GATE AND DYNAMIC SHIFT REGISTER USING CNT TECHNOLOGY

Submitted in partial fulfillment of the Requirement for the award of the degree of

BACHELOR OF TECHNOLOGY
IN
ELECTRONICS AND COMMUNICATION ENGINEERING

Submitted by

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CERTIFICATE

This is to certify that the dissertation entitled "DESIGN OF TRANSMISSION GATE AND DYNAMIC SHIFT REGISTER USING CNT TECHNOLOGY" is being submitted by Vadde Rishitha (20091A04E5), Saddala Anitharani (20091A0404), Neredujalla Aravind (20091A0407), Kaka Sai Prasad (20091A04F4) under the guidance of Smt. M. Maheswari, Assistant Professor for Project of the award of B.Tech Degree in Electronics and Communication Engineering, Rajeev Gandhi Memorial College of Engineering and Technology, Nandyal (Autonomous) (Affiliated to JNTUA Anantapuramu) is a record of bonafide work carried out by them under our guidance and supervision.

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CANDIDATES' DECLARATION

We hereby declare that the work done in this project titled **"DESIGN OF TRANSMISSION GATE AND DYNAMIC SHIFT REGISTER USING CNT TECHNOLOGY"** submitted for the completion of the main project in the IV Year II Semester of B. Tech (ECE) at **Rajeev Gandhi Memorial College of Engineering and Technology (Autonomous), Nandyal**, is an authentic record of our original work done under the guidance of **Smt.M.Maheswari, Assistant Professor**, Dept. of ECE, RGMCET, Nandyal. We have not submitted the material embodied in this main Project for the award of any other degree in any other institution.

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ABSTRACT

Carbon Nano Tube Field Effect Transistors (CNFETs) are having unique feature of alteration of threshold voltage by variations in CNT diameter to implement multi valued logic designs. Multi –valued logic design isa best alternative that offers a higher number of data/information which leads to energy efficiency, higher information density and reduced circuit in terms of interconnect complexity. In the project, transmission gates and dynamic shift registers were designed using Carbon Nano Tube (CNT) technology. Performance metrics such as delay, power consumption, and Power-Delay Product (PDP) were calculated utilizing CADENCE and other relevant tools. Additionally, the performance of these circuits was compared with that of CMOS circuits.

Keywords-CNTFET, Transmission gate, Dynamic shift register

CHAPTER-I

INTRODUCTION

1.1 Introduction

Very large scale integration is the processes of creating integrate circuits by combining thousands of transistor-based circuit's integrated circuits into a single chip. Very large scale integration began in the 1970's when complex semiconductor and communication technologies were being developed. The microprocessor is a Very large scale integration device. The term is no longer as common as it one's was, as chips have increased in complexity into the thousands of millions of transistors.

The first semiconductor chips held one transistor each. Subsequent advances added more and more transistors, and, as a consequence, more individual functions or systems were integrated over time. The first integrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device. Now known respectively as "Small Scale Integration" (SSI), improvements in technique led to devices with hundreds of thousand logic gates. Current technology as moved far past this mark and today's microprocessors have many millions of gates and hundreds of millions of individual transistors.

1.2 Very Large Scale Intergration

1.2.1 History of scale integration

VLSI stands for "Very Large Scale Integration". This is the field which involves packing more and more logic devices into smaller and smaller areas.

1. Simply, integrated circuit is many transistors on one chip.
2. Design/manufacturing of extremely small, complex circuitry using modified semiconductor material.
3. Integrated circuit (IC) may contain millions of transistor, each a few mm in size.
4. Applications wide ranging: most electronic logic devices.

5. Late 40s Transistor invented at Bell Labs. Late 50s First IC (JK-FF by Jack Kilbyat TI)
6. Early 60s Small Scale Integration (SSI), 10s of transistors on a chip.
7. Late 60s Medium Scale Integration (MSI), 100s of transistors on a chip.
8. Early 70s Large Scale Integration (LSI), 1000s of transistors on a chip
9. Early 80s VLSI 10,000s of transistors on a chip (later 100,000s and now 1,000,000s)

SSI- Small-Scale Integration (10-102)
MSI- Medium Scale Integration (102-103)
LSI- Large Scale Integration (103-105)
VLSI- Very Large Scale Integration (105-107)
ULSI- Ultra Large Scale Integration (>=107)

1.2.2 Advantages of ICs over discrete components

ICs have three key advantages over digital circuits built from discrete components:

i. *Size*:

Integrated circuits are much smaller-both transistors and wires are shrunk to micrometers sizes, compared to the millimeter or centimeter scales of discrete components. Small size leads to advantages in speed and power consumption, since smaller components have smaller parasitic resistances, capacitances, and inductances.

ii. *Speed*:

Signals can be switched between logic 0 and logic 1 much quicker within a chip than they can between chips. Communication within a chip can occur hundreds of times faster than communication between
chips on a printed circuit board. The high speed of circuits on-chips due to their small size-smaller components and wires have smaller parasitic capacitances to slow down the signal.

iii. *Power consumption*:

Logic operations within a chip also take much less power. Once again, lower power. Once again, lower power consumption is largely due to the small size

of circuits on the chip-smaller parasitic capacitances and resistances require less power to drive them.

1.2.3 Applications and advantages

Electronic systems now perform a wide variety of tasks in daily life. Electronic systems now perform a wide variety of tasks in daily life. Electronic systems in some cases have replaced mechanisms that operated mechanically, hydraulically, or by other means; electronics are usually smaller, more flexible, and easier to service. In other cases electronics systems have created totally new applications. Electronic systems perform a variety of tasks, some of them visible, some more hidden:

1. Personal entertainment systems such as portable MP3 players and DVD players perform sophisticated algorithms with remarkably little energy.
2. Electronic systems in cars operate stereo systems and displays; they also control fuel injection systems, adjust suspensions to varying terrain, and perform the control functions required for anti-lock braking (ABS) systems.
3. Digital electronics compress and decompress video, even at high-definition data rates, on-the-fly in consumer electronics.
4. Low-cost terminals for web browsing still require sophisticated electronics, despite their dedicated function.
5. Personal computers and workstations provide word- processing, financial analysis, and games. Computers
include both central processing units (CPUs) and special- purpose hardware for disk access, faster screen display, etc.
6. Medical electronic systems measure bodily functions and perform complex processing algorithms to warn about unusual conditions. The availability of these complexes, far from overwhelming consumers, only creates demand for even more complex systems.

The growth sophistication of applications continually pushes the design and manufacturing of integrated circuits and electronics systems to new levels of complexity. And perhaps the most amazing characteristic of this collection of systems is its variety-as systems become more complex, we build

not a few general-purpose computers but an everwider range of special-purpose systems. Our ability to do so is a testament to our growing mastery on both integrated circuit manufacturing and designs, but the increasing demands of customers continue to test the limits of design and manufacturing.

1.3 CNTFET

A Carbon Nanotube Field-Effect Transistor (CNTFET) is a type of field effect transistor that employs either a single carbon nanotube or an array of carbon nanotubes as the channel material, replacing the bulk silicon used in traditional MOSFET structures. First demonstrated in 1998, CNTFETs have undergone significant advancements since then.

Moore's Law dictates that the dimensions of individual devices within integrated circuits shrink by a factor of approximately two every two years. This downsizing trend has been a driving force behind technological progress since the late 20th century. However, as highlighted in the 2009 edition of the International Technology Roadmap for Semiconductors (ITRS), further scaling down faces substantial challenges related to fabrication technology and device performance when critical dimensions reach the sub22 nanometer range. These challenges include electron tunneling through short channels and thin insulator films, resulting leakage currents, passive power dissipation, short channel effects, and variations in device structure and doping. To address these limitations and enable further miniaturization of device dimensions, modifying the channel material in traditional bulk MOSFET structures with a single carbon nanotube or an array of carbon nanotubes offers a promising solution.

***Device Fabrication*:**

Below is an overview of the most common geometries of CNTFET devices, which encompass various types of configurations.

Back-Gated CNTFET's:

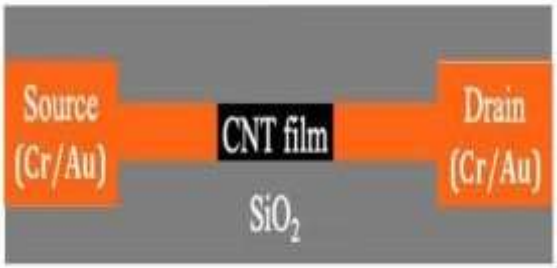


Fig 1.1: Top View

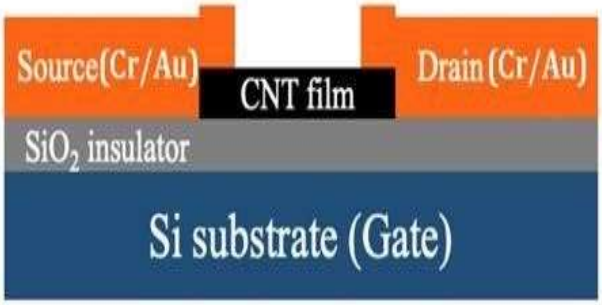


Fig 1.2: Side View

In the silicon back-gated CNTFET, both top and side views depict carbon nanotubes (CNTs) deposited on a silicon oxide substrate that has been pre-patterned with chromium/gold source and drain contacts.

The initial techniques for fabricating carbon nanotube (CNT) field effect transistors involved creating parallel strips of metal on a silicon dioxide substrate and subsequently depositing CNTs on top in a random configuration. Semiconducting CNTs that bridged two metal strips met the requirements for a basic field-effect transistor, with one metal strip serving as the "source" contact and the other as the "drain" contact. By applying a metal contact on the back, the semiconducting CNT could be gated using the silicon oxide substrate.

However, this approach had limitations. Firstly, the metal contact had minimal contact with the CNT, resulting in a small contact area and increased contact resistance due to the formation of a Schottky barrier at the metal-

semiconductor interface. Secondly, the back-gate device geometry's thickness made it challenging to effectively switch the devices on and off using low voltages, and the fabrication process often resulted in poor contact between the gate dielectric and the CNT.

Top-gated CNTFET's:

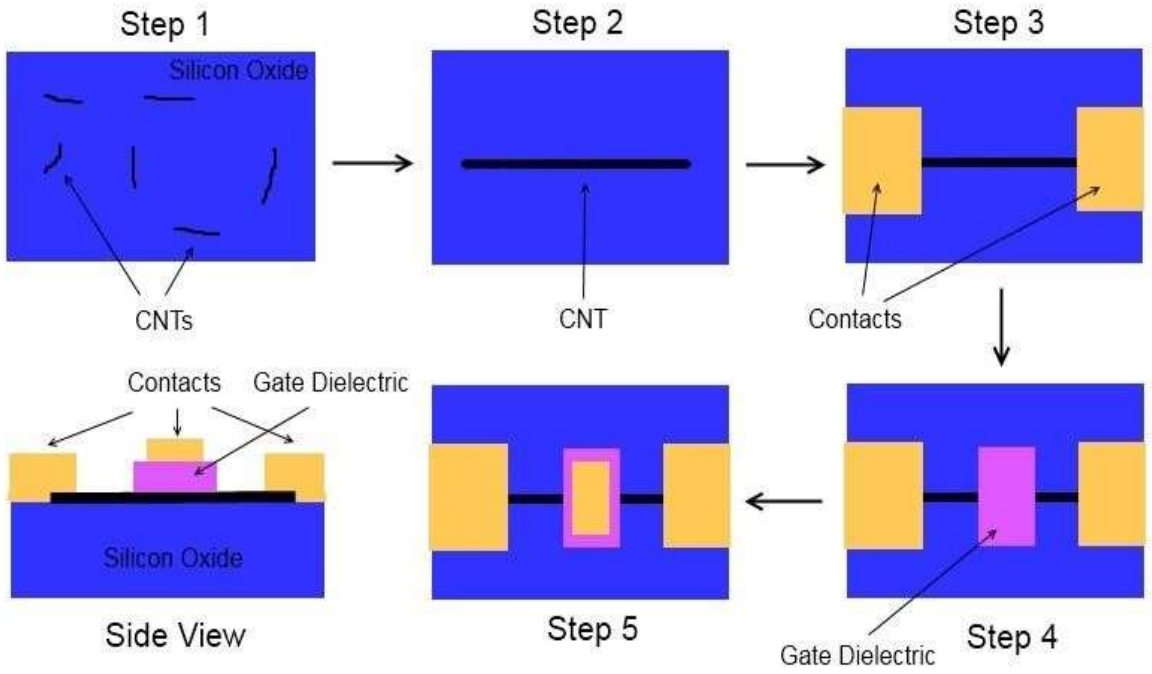


Fig 1.3: The Process for fabricating a top-gated CNTFET

Researchers have transitioned from the back-gate to a more sophisticated top gate fabrication method. Initially, single-walled carbon nanotubes are deposited onto a silicon oxide substrate using a solution. Subsequently, individual nanotubes are located via atomic force microscopy or scanning electron microscopy. Once isolated, source and drain contacts are defined and patterned using high-resolution electron beam lithography. A high-temperature annealing step is then employed to reduce contact resistance by enhancing adhesion between the contacts and CNT. Next, a thin top-gate dielectric is deposited atop the nanotube, either through evaporation or atomic layer deposition. Finally, the top gate contact is applied onto the gate dielectric, completing the process.

Arrays of top-gated CNTFETs can be produced on the same wafer since the gate contacts are electrically isolated from each other, unlike in the back-gated scenario. Furthermore, owing to the thinness of the gate dielectric, a larger electric field can be generated with respect to the nanotube using a lower gate voltage. These benefits render top-gated devices generally preferred over back-gated CNTFETs, notwithstanding their more intricate fabrication process.

Wrap-around gate CNTFET's:

Fig 1.4: Wrap around gate CNFET

Sheathead CNT:

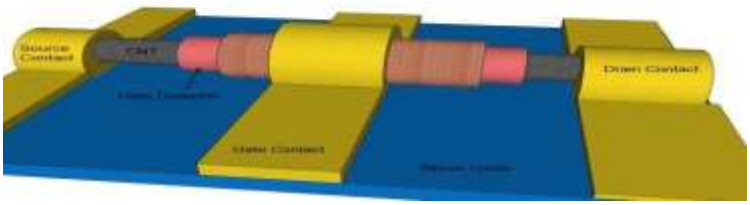


Fig 1.5: Gate all around CNT device

Wrap-around gate CNTFETs, also known as gate-all-around CNTFETs, were introduced in 2008 as an advancement over the top-gate device design. In this configuration, the entire circumference of the nanotube is gated instead of just a portion closer to the metal gate contact. This design enhancement aims to enhance the electrical performance of the CNTFET by reducing leakage current and improving the device on/off ratio.

The fabrication process begins by wrapping CNTs in a gate dielectric and gate contact through atomic layer deposition. These wrapped nanotubes are then deposited onto an insulating substrate via solution deposition, where the wrappings are partially etched off to expose the ends of the nanotube. Subsequently, the source, drain, and gate contacts are deposited onto the exposed ends of the CNT, as well as onto the metallic outer gate wrapping.

Suspended CNTFET's:

Another variation of CNTFET device geometry involves suspending the nanotube over a trench to minimize contact with the substrate and gate oxide, thereby reducing scattering at the CNT-substrate interface and enhancing device performance. Various methods are employed to fabricate suspended CNTFETs, including growing them over trenches using catalyst particles, transferring them onto a substrate followed by under-etching the dielectric beneath, and transfer-printing onto a trenched substrate.

However, suspended CNTFETs encounter significant challenges. They have limited material options for the gate dielectric, typically air or vacuum, and applying a gate bias pulls the nanotube closer to the gate, imposing an upper limit on the extent of gating. Moreover, this technique is only feasible for shorter nanotubes; longer ones may flex in the middle and sag towards the gate, potentially causing contact with the metal contact and device shorting. Generally, suspended CNTFETs are impractical for commercial applications but serve well for investigating the intrinsic properties of pristine nanotubes.

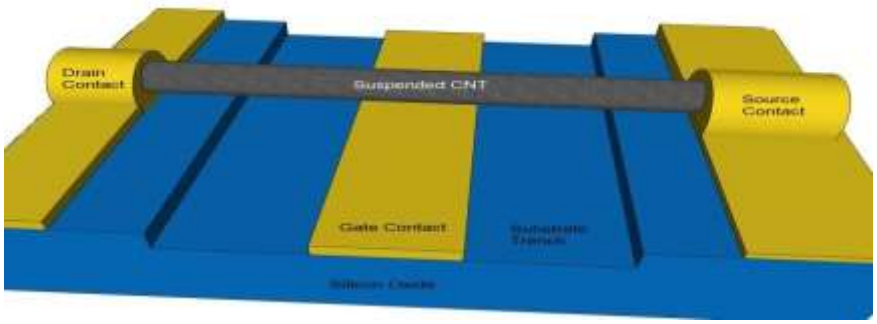


Fig 1.6: A suspended CNTFET device

CNTFET material considerations:

When selecting materials for fabricating a CNTFET, certain considerations come into play. Semiconducting single-walled carbon nanotubes are favored over metallic single-walled and metallic multi-walled tubes due to their ability to be completely switched off, particularly for low source/drain biases. Extensive research has focused on identifying an appropriate contact material for semiconducting CNTs, with Palladium emerging as the best option to date. This is because its work function closely aligns with that of nanotubes, and it exhibits strong adhesion to the CNTs.

A Carbon Nanotube Field-Effect Transistor (CNTFET) has three important parts: the source, drain, and gate. The source is like the entry point where electric charges start flowing into the transistor. The drain is where these charges exit after passing through the transistor. The gate is the control center—it decides how easily charges can move from the source to the drain. By adjusting the voltage on the gate, we can make the transistor allow a lot of charges to flow or stop them completely. This control makes CNTFETs very useful in electronics, especially for making things like faster and more efficient computers.

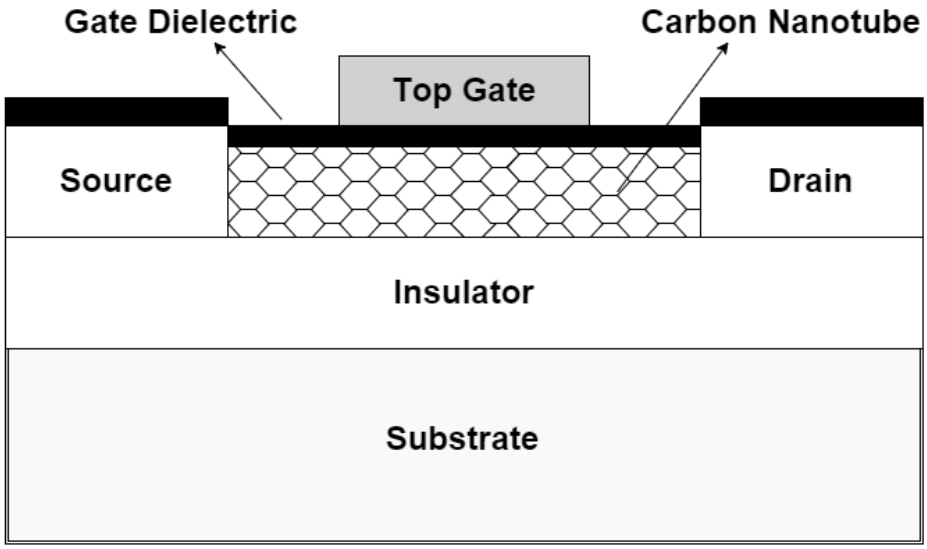
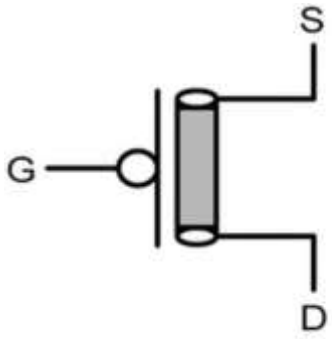


Fig 1.7: Structure of CNTFET

1.3.1 Types of CNTFET Transistor based on operation Modes

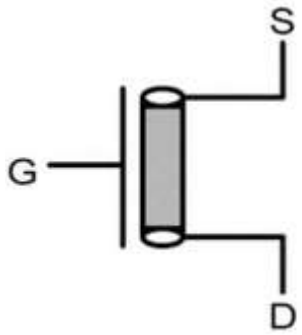
i. PCNFET:

The carbon nanotube channel predominantly conducts positive charge carriers known as holes, characteristic of p-type semiconductors. Under no gate voltage, the channel allows hole flow, creating a conductive path between the source and drain



Application of a positive voltage to the gate induces an electric field perpendicular to the channel, influencing hole concentration. By adjusting gate voltage, the number of holes in the channel is controlled, regulating current between source and drain.

ii. NCNFET:



In the NCNFET, the carbon nanotube channel predominantly conducts negative charge carriers, specifically electrons, which is characteristic of n-type semiconductors. When no gate voltage is applied, the channel remains non-conductive. However, upon applying a positive voltage to the gate terminal, an electric field perpendicular to the channel is induced, allowing the attraction of electrons to form a conductive path between the source and drain terminals. By modulating the gate voltage, the number of

electrons in the channel is controlled, thereby regulating current flow. This control mechanism enables the NCNFET to function as a highly efficient switch or amplifier in electronic circuits.

1.4 Transmission Gate

When the transmission gate is activated or turned ON, both the NCNFET and PCNFET transistors are conducting. the input signal is applied to the gates of both the NCNFET and PCNFET transistors. the NCNFET transistor acts as a low-side switch, connecting the input signal to the output node when it is turned ON.

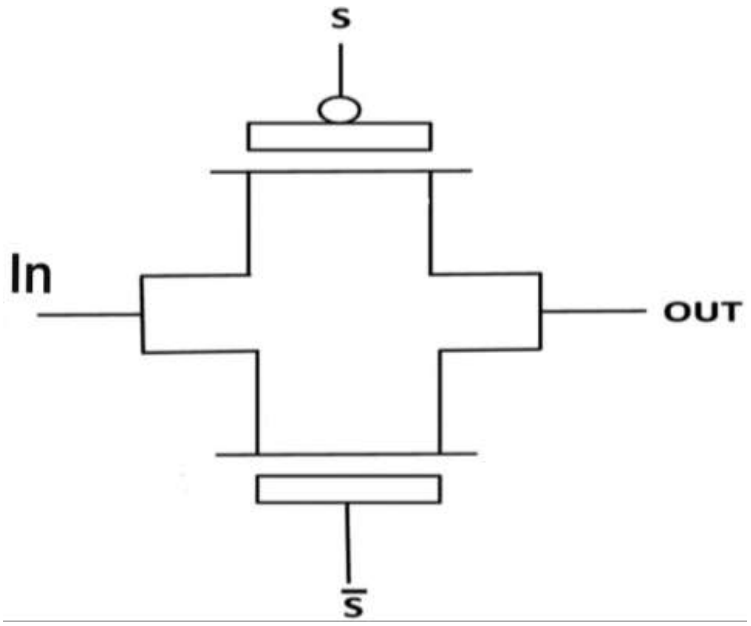


Fig 1.8: Circuit diagram of Transmission gate

Simultaneously, the PCNFET transistor acts as a high-side switch, connecting the complementary signal (inverted) to the output node when it is turned ON.

As a result, the input signal is transmitted directly to the output node without inversion, and its complementary signal is also transmitted with inversion.

A transmission gate is a fundamental electronic circuit used in digital and analog systems for various purposes such as signal routing, level shifting, isolation, and bidirectional data transfer.

CHAPTER-II

LITERATURE REVIEW

2.1 Low-Power and Area-Efficient Shift Register Using Pulsed Latches

This paper presents a novel approach to designing a low-power and area-efficient shift register using pulsed latches instead of traditional flip-flops. By replacing flip-flops with pulsed latches, significant reductions in both area and power consumption are achieved. The timing problem inherent in using pulsed latches is effectively addressed by employing multiple non-overlap delayed pulsed clock signals in the shift register design. This innovative solution allows for a smaller number of pulsed clock signals by grouping latches into sub shifter registers and utilizing additional temporary storage latches. The fabricated 256-bit shift register, implemented using a 0.18 μm CMOS process, demonstrates impressive performance, consuming only 1.2 mW at a clock frequency of 100 MHz. Compared to conventional shift registers with flip-flops, the proposed design saves 37% in area and 44% in power consumption, showcasing its efficiency and effectiveness in practical applications.

2.2 CNTFET design of a multiple-port ternary register file

This paper explores the implementation of ternary logic gates and CNTFET technology in the design of a multiple-port ternary register file. Ternary logic systems offer advantages over binary systems by reducing interconnection complexity, chip area, and energy consumption while enabling faster arithmetic operations. CNTFETs have emerged as a promising technology, overcoming CMOS challenges and providing better power and delay results. The study proposes various circuit realizations for ternary memory elements like ternary D-latch and ternary D-flip-flop, which are essential components in processor design. By comparing the performance aspects of using ternary register files, the research aims to pave the way for further advancements in full ternary computer architecture. The proposed

designs are evaluated in terms of power, area, and latency at different supply voltages and operating temperatures, highlighting the potential of ternary logic systems in enhancing digital integrated systems.

2.3 Design of energy-efficient and robust ternary logic and arithmetic circuits for nanotechnology

This Paper explores the development of energy-efficient and robust ternary logic and arithmetic circuits for nanotechnology utilizing carbon nanotube field-effect transistors (CNFETs). These circuits are designed to implement negative, positive, and standard ternary logics within a single structure, showcasing good driving capability and large noise margins. Leveraging the unique properties of CNFETs, such as the ability to set threshold voltages by adjusting nanotube diameters, the proposed designs aim to address challenges in traditional CMOS technology, including short-channel effects, gate control limitations, and high leakage power. By adopting a multi-Vt design methodology, the circuits demonstrate enhanced performance and resilience to process variations compared to existing CMOS and CNFET-based ternary circuits.

The study evaluates the delay, power consumption, and energy efficiency of CNFET-based ternary circuits in the presence of process variations, specifically deviations and mismatches in nanotube diameters and transistor channel lengths. Monte Carlo transient analysis with 30 iterations per simulation is conducted using the HSPICE simulator to assess the impact of these variations on circuit performance. The distribution of nanotube diameters and channel lengths is assumed to follow a Gaussian distribution, with the statistical significance of 30 iterations providing a high probability of proper circuit operation under varying component values. The results highlight the sensitivity of CNFET-based circuits to process variations and emphasize the importance of robust design strategies to mitigate performance degradation.

2.4 Design of CNTFET-Based Ternary ALU Using 2:1 Multiplexer Based Approach

This paper explores the implementation of ternary logic circuits using Carbon Nanotube Field Effect Transistors (CNTFETs) as an alternative to traditional silicon transistors. The proposed Ternary Arithmetic and Logic Unit (TALU) architecture consists of a function select block, a transmission gate block, and functional modules. This TALU design allows for four arithmetic operations (addition, subtraction, multiplication, and comparison) and five logic operations (Ex-OR, OR, AND, NOR, and NAND) on 2-trit inputs, providing a 2-trit output based on select lines S1S0. The paper introduces a new design optimized for performance, incorporating additional arithmetic operations like increment and decrement, along with a new encoder design for improved functionality. The architecture includes a function select block, transmission gate block, function processing modules, and an output multiplexer module to streamline operations and enhance overall efficiency. Simulation results showcase the effectiveness of the proposed design compared to existing TALU designs, highlighting its potential for reducing power consumption and enhancing computational capabilities in modern computing systems.

2.5 High-Density Memristor-CMOS Ternary Logic Family

This paper explores on the implementation of a complete memristor-CMOS ternary logic family, marking a significant advancement in hardware design. The research focuses on optimizing speed at the device level to outperform existing ternary logic simulations using memristors, while also highlighting challenges in power and speed compared to conventional CMOS. By fabricating threshold-switching metal-insulator-metal (MIM) structure memristor devices with fast switching speeds and integrating them into optimized ternary logic gates, the study achieves remarkable data density improvements. Ternary logic, computed at a higher radix than binary, offers enhanced data density, and the integration of memristors in the back end of the line enables substantially higher data density compared to traditional

CMOS logic. The research addresses issues such as slow switching

speeds and limited endurance in memristors, emphasizing the importance of achieving fast switching speeds without compromising endurance. By providing area, power, and speed metrics, the study sets a benchmark for future memristor-CMOS implementations and offers valuable insights for advancing multi-level applications like storage class memory and ternary content addressable memories. The availability of simulation data online ensures reproducibility and facilitates further research in this cutting-edge field.

2.6 High-Performance Ternary Adder Using CNTFET

This paper presents in advanced VLSI design by exploring the implementation of ternary logic circuits using Carbon Nanotube Field-Effect Transistors (CNTFETs). The paper highlights the potential advantages of ternary logic over traditional binary logic in terms of reduced interconnect complexity, lower power consumption, and enhanced computational speed. By leveraging the unique properties of CNTFETs, the authors propose innovative ternary half adder circuits that aim to optimize power efficiency and performance in data path circuits like adders.

The introduction section sets the stage by discussing the limitations of MOSFETs as semiconductor technology approaches nanoscale dimensions. It introduces CNTs as a promising alternative due to their exceptional physical properties and suitability for integration into electronic devices. The emergence of CNTFETs as a novel device structure is emphasized, with a focus on their potential to revolutionize post-silicon electronics.

The paper emphasizes the ongoing research in fabricating and purifying CNTs to enhance their orientation and performance in electronic applications. It references previous works that have explored CNTFET fabrication methods and the manipulation of CNT properties for specific applications. The growing interest in CNTFETs for logic gates, memory cells, and multiple-valued logics is highlighted, showcasing the diverse range of potential applications for these advanced devices.

A detailed analysis of ternary logic circuits is presented, focusing on the design and implementation of ternary half adder circuits using CNTFET technology. The paper discusses the advantages of ternary logic in reducing interconnection complexity, improving computational speed, and enhancing overall system efficiency. The proposed ternary half adder circuits demonstrate superior performance metrics such as power consumption, delay, and power delay product compared to existing binary and ternary designs, showcasing the potential for high-performance arithmetic circuits.

The experimental results and performance comparisons provided in the paper validate the effectiveness of the proposed ternary adder circuits in achieving significant improvements in power efficiency and computational speed. The detailed circuit implementations, transistor configurations, and performance metrics offer valuable insights into the feasibility and advantages of utilizing CNTFET technology in ternary logic applications.

CHAPTER-III

CNTFET CIRCUITS

3.1 CNTFET Inverter

A carbon nanotube field-effect transistor (CNTFET) inverter operates based on the principles of field-effect transistor technology but utilizes carbon nanotubes as the semiconductor material. In this device, the input signal controls the flow of current between the source and drain terminals by modulating the electric field within the carbon nanotube channel. The inverter configuration consists of one PCNFET and one NCNFET connected in series: one acting as a pull-up transistor and the other as a pull-down transistor. When the input signal is low, the pull-up transistor conducts, creating a path for current from the power supply to the output. Conversely, when the input signal is high, the pull-down transistor conducts, providing a path for current to flow from the output to ground. This inversion of the input signal is crucial for digital logic operations. The use of carbon nanotubes offers advantages such as high carrier mobility, which enhances the device's speed and efficiency. Below figure 3.1 shows the schematic diagram of CNTFET inverter

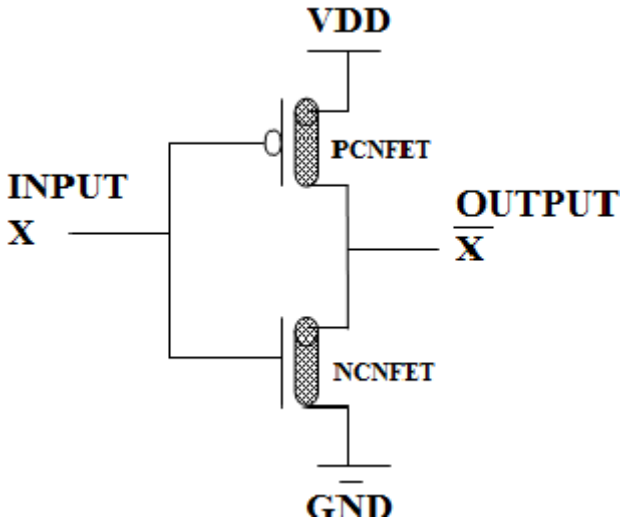


Fig 3.1: Schematic diagram of CNTFET Inverter

3.2 Standard Ternary Inverter:

CNTFETs are well-suited for implementing ternary logic, which operates with three logic levels:

- **-1 (Logic Low)**
- **0 (Logic Zero)**
- **+1 (Logic High)**

The STI inverter transistor implementation which is deployed is shown in Fig. 3.2

They consist of six CNTFETs: two pull-up transistors that turn on at -1 input, two pull-down transistors that turn on at +1 input, and two level shifters to maintain proper voltage levels. The operation depends on the threshold voltages of the transistors. When the input is -1, the level shifters activate pull-up transistors, driving the output to +1. Conversely, a +1 input turns off the level shifters and activates pull-down transistors, leading to a -1 output. For a 0 input, the level shifters enter a high-impedance state, isolating the input and preserving the previous output state (+1 or -1), achieving the latching behavior.

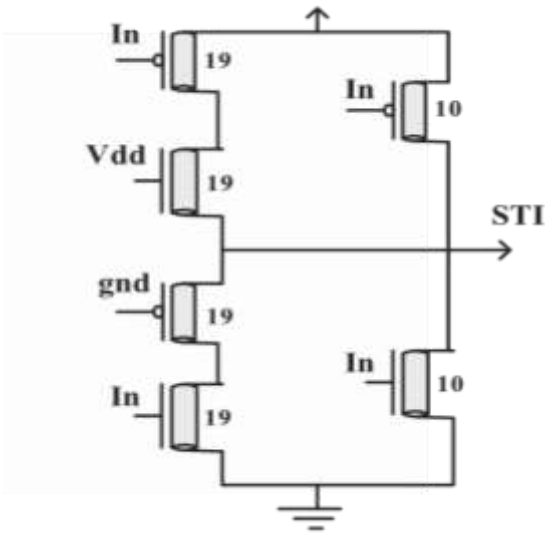


Fig 3.2 : Standard Ternary Inverter

Compared to traditional transistors, CNTFETs offer advantages like faster switching, sharper transitions, and potentially lower power consumption in specific scenarios.

3.3 Transmission Gate using Ternary Logic:

A transmission gate acts like a switch controlled by a signal. It allows a signal to pass through when the control signal is on and blocks it when the control signal is off. the Transmission gate using CNTFET designed with both PCNFET and NCNFET are connected as parallel. They works like when the input signal is 0(low) PCNFET turns ON and NCNFET turns OFF. when the input signal is 1(high) NCNFET turns ON and PCNFET turns OFF. A specific type of input signal, a piecewise linear pulse, can be used with the gate. This pulse consists of straightline segments with different slopes. How the circuit behaves depends on the control signal and the pulse itself.

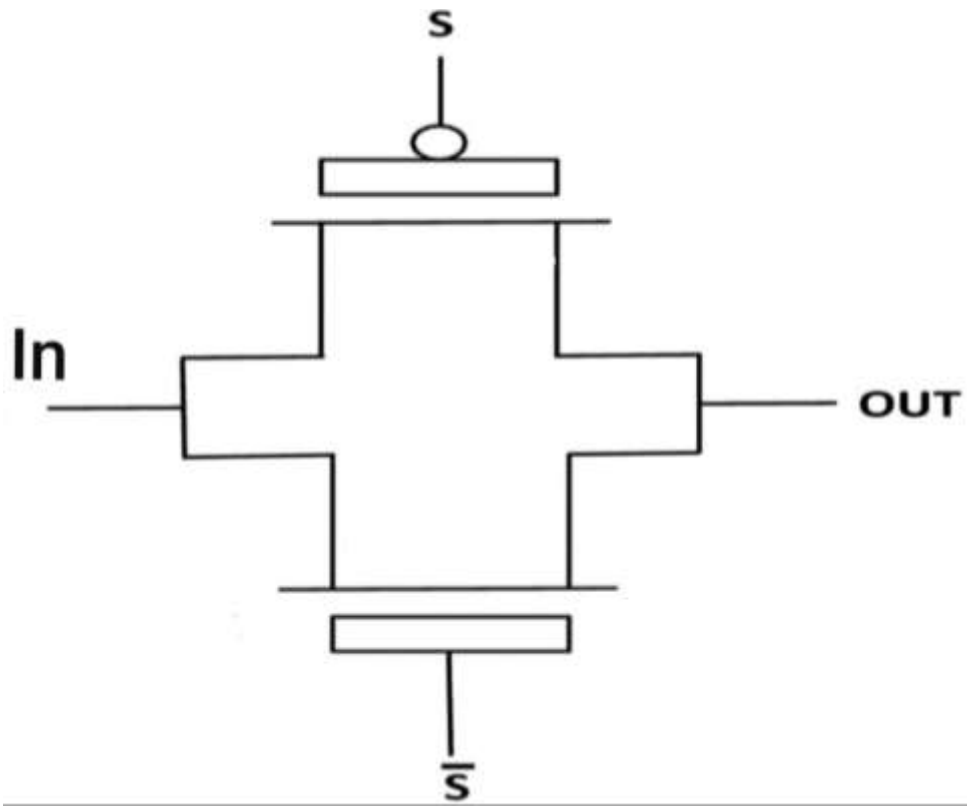


Fig 3.3: Transmission Gate

When the control signal is on and the pulse voltage is within the operating range of the transistors, the pulse passes through with minimal distortion. If the control signal is off, the output is isolated from the input regardless of the pulse voltage. Understanding how these transistors behave electrically and how the timing of the control signal works is important for

designing these circuits effectively. While CNTFET-based transmission gates have advantages, challenges like fabrication and variability in the transistors themselves need to be addressed before they are widely used.

CHAPTER-IV

Multiplexer Based Ternary Latches

Latches are level sensitive devices that allow passage of applied input to the output side whenever a high clock signal is fed across it. There are two types of latches viz. positive latch and negative latch based on the sampling of data. For positive latch, the input D is selected when the clock is at a high logic level and the output will be held if the clock is at a low logic level. Similarly, the negative latch gives applied D input if the clock is at low logic while it will be in hold state for high logic clock transition

4.1 Positive Latch

Positive latches are fundamental building blocks in digital circuits used to store data. They can be designed using CNTFETs (carbon nanotube field-effect transistors) to potentially offer advantages over traditional silicon-based designs. If a latch with two input signals, data (D) and a clock (CLK). The data we want to store is into the D input. The CLK acts like a switch that controls when the data is captured and held. Fig 4.1 shows the Block diagram of Positive latch

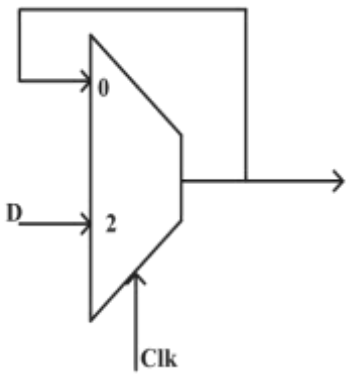


Fig 4.1: Block diagram of Positive latch

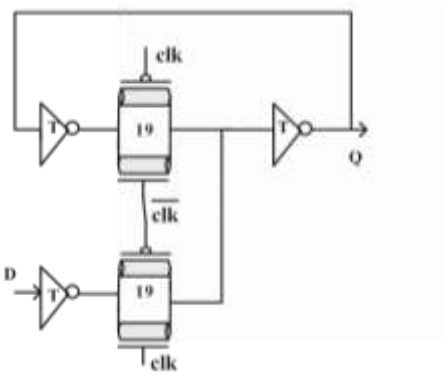


Fig 4.2: CNTFET implementation of Positive latch

Inside the latch, a feedback loop is created using CNTFETs. This loop amplifies any existing voltage difference between two internal nodes. When CLK is low, the loop is inactive. If D is high, one node in the loop will be charged to a higher voltage. When CLK transitions high, the loop becomes active and strengthen the potential difference. This high voltage at one node keeps the other node low, effectively storing the value of D. As long as CLK remains high, the data is held regardless of any changes on the D input. However, when CLK goes low again, the feedback loop deactivates. Any new data presented at D can now influence the internal nodes, potentially changing the stored value upon the next rising level of CLK. This creates a latching window controlled by the CLK signal. Fig. 4.2 shows the multiplexer based implementation of the positive latch.

4.2 Negative Latch:

Negative latches capture data on the **falling level** of the clock (CLK) signal.

The inputs as data (D) and clock (CLK). The data to be stored goes to the D input, while CLK acts like switch. Within the latch, CNTFETs are arranged to form a transparent latch during a specific period. When CLK is high, the CNTFETs act like open switches, creating a direct path for the D signal to reach an internal storage node.

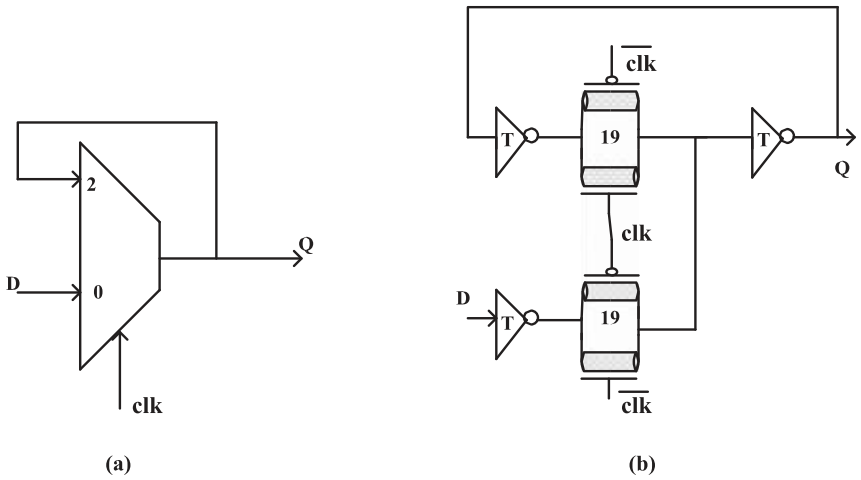


Fig 4.3: (a) Block diagram of Negative latch (b) CNTFET implementation of Negative latch.

Any changes in D are directly reflected at the storage node. However, this data isn't held yet. when CLK transitions from high to low (falling level). The CNTFETs abruptly switch, becoming closed switches. This isolates the storage node from the D input, effectively capturing the data value present at D just before the falling level. As long as CLK is low, the data is latched, unaffected by further changes on the D input. Fig 4.3 shows the Block diagram of Positive latch and CNTFET implementation of Negative latch

A rising level of CLK resets the latching condition. The CNTFETs become open switches again, allowing the D input to influence the storage node if needed. This creates a capture window solely defined by the falling level of CLK. CNTFET-based negative latch utilizes a clock edge-triggered switch formed by CNTFETs. Data is captured on the falling level of CLK and held as long as CLK remains low.

4.3 Multiplexer based Ternary D-flip-flop:

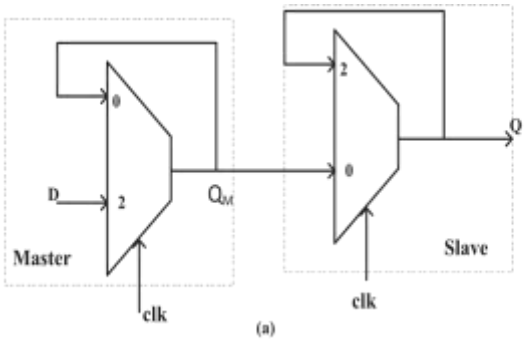


Fig 4. 4: Block diagram representation of D-flip-flop

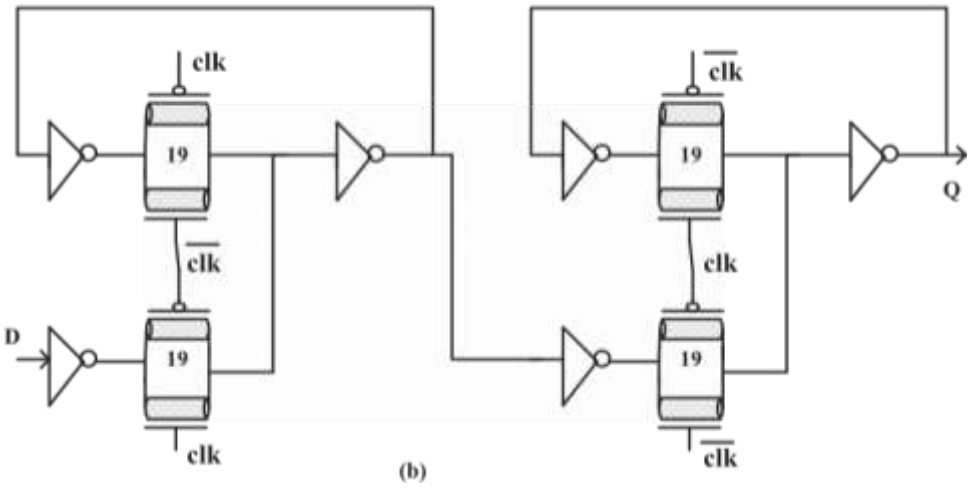


Fig 4. 5: CNTFET implementation of proposed D-flip-flop using ternary latches.

whenever clock input is at one logic, the master stage is in on state so whatever input D is applied that is latched at the output of positive latch and Negative latch is in off state. If clock transitions occur to another logic, then the Negative latch enters into active state and whatever output of the positive latch is latched to the output of the slave stage.

The proposed multiplexer-based ternary D-flip-flops using CNTFETs present a novel approach distinct from existing designs. Unlike conventional methods, these D-flip-flop designs leverage cascading successor and predecessor unary operators, exploiting rotational symmetry. This unique

strategy enhances the realization of ternary counters, particularly with the Q(+1) input, which serves as a more suitable feedback input for advancing the sequence. Instead of employing traditional inverters, the design utilizes shifting unary operators, resulting in more efficient hardware utilization. This departure from conventional methods prevents the complexity that arises from using inverters.

D-flip-flop realization using positive and negative multiplexer based latches is shown in Fig 4.5

With the usage of tenary logic three voltage levels representing "0," "1," and a middle value. Each latch captures data based on the clock signal: Positive latch on the rising level and Negative latch on the falling level. Standard ternary inverters complement these captured values. Meanwhile, CNTFET transmission gates act as controlled switches, allowing manipulation of the ternary data based on additional control signals.

The complexity lies in ensuring proper functionality with a three-level input pulse. Precise timing and configuration are crucial for all elements to capture, manipulate, and output the desired ternary data. Depending on the specific arrangement, this circuit could potentially perform tasks like data selection, comparison, or even basic ternary arithmetic.

4.4 Shift Registers:

Ternary Serial Input Serial Output Register:

A serial-in-serial-out (SISO) shift register is a type of shift register where data is entered serially, one bit at a time, and shifted out serially, one bit at a time. It's a sequential digital circuit that can store and move data

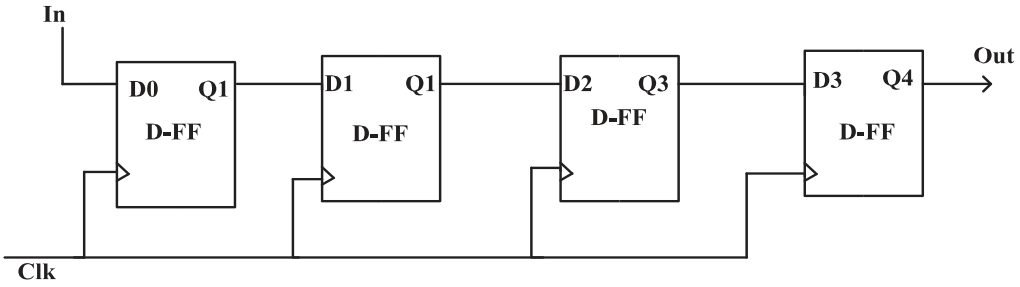


Fig 4.6: Ternary serial input serial output register implementation using proposed multiplexer based D-flip-flops

The operation of a SISO shift register involves four main steps: initialization, serial input, shift operation, and serial output. Firstly, during initialization, all flip-flops in the shift register are set to a known state, often all zeros. This ensures that the register starts with a clean slate before data is inputted. Next, data is serially inputted into the shift register. This input process typically starts with the least significant bit (LSB) and proceeds to the most significant bit (MSB). The input data is usually synchronized with a clock signal, where each clock pulse corresponds to one bit of data being inputted. After the data is inputted, the shift operation begins. With each clock pulse, the data in the shift register shifts by one bit position. The direction of shifting (left or right) depends on the design of the shift register. In a SISO shift register, the shifting is usually towards the right, meaning data moves from the LSB towards the MSB.

Finally, the serial output is obtained from the last flip-flop in the shift register, which holds the most recently shifted-in bit of data. This serial output represents the data that has been shifted through the register. The serial output can be used as input for another SISO shift register or for further processing in a digital system.

Overall, a SISO shift register provides a way to sequentially process and manipulate data in a serial fashion, making it suitable for applications such as serial communication protocols, data storage, and signal processing.

Shift registers are an essential storage element in VLSI circuits and are employed in various electronic applications such as filters, communication receivers and image processing ICs. For instance, digital image processing applications demand high quality images, therefore the input size of the image also get increases as a higher number of pixels inclusion should be done. In that case size of the shifter also need to be increased in order to process large-sized image files. As shifter input size is increased leads to an increment in area as well as power consumption also. Hence the introduction of ternary logic can address this increment in shifter word length and helps in optimizing design parameters for a digital circuit. The construction of the SISO register is done by a series connection of D-flip-flop cells. As each D-flip-flop can store one bit at a time so a register formed by connecting N-stage flip-flops constitutes N-bit register storage capacity. The SISO register accepts input data in serial form Fig. 4.6 Ternary serial input serial output register implementation using proposed multiplexer based D-flip-flops. and based on every input clock edge the input data is shifted serially and passed to the output(Q). The 4-stage serial input serial output register implementation using proposed multiplexer based D-flip-flop cells is as indicated in Fig. 4.6. All the flip-flops are driven by the clock signal and the output of one flip-flop is fed as input to the next flip-flop. In the SISO register area and power consumption are primary design parameters and delay does not matter a lot. This is because in the shift register there is no circuitry between the flip-flops and all are driven by a same clock signal.

CHAPTER – V

HARDWARE DESCRIPTION

Cadence Tool

Cadence EDA

The accompanying Cadence CAD tool will be utilized as a part of this instructional exercise Virtuoso Schematic for schematic catch Spectral for simulation. We will work on utilizing

CADENCE with a CMOS Inverter: making (1) Schematic (2) Simulation

Computer Account Setup

If it's not too much trouble see the Unix/Linux command before doing this new Instructional exercise.

You must include your atmosphere position up for CADENCE and extra TOOLS

Running the Cadence tools

Sign in to your UNIX/LINUX account.

Open the terminal window.

Presently you ought to have the capacity to run the Cadence tool. Never run Cadence from your root directory, it makes numerous additional records that will mess your root. Rather please make a directory (e.g. cadence).

>>mkdir cadence

>>cd cadence Now start Cadence by typing

>>csh

>> source cshrc

>>cd cadence_ms_labs_613

>>virtuoso

Please see the Fig.5.1 for above command

Fig 5.1: Terminal Window

The command will set up Cadence and later than a while you must get a window with the

"Virtuoso@ 6.1.5", also called Command Interpreter Window (CIW) as below: Fig 5.2

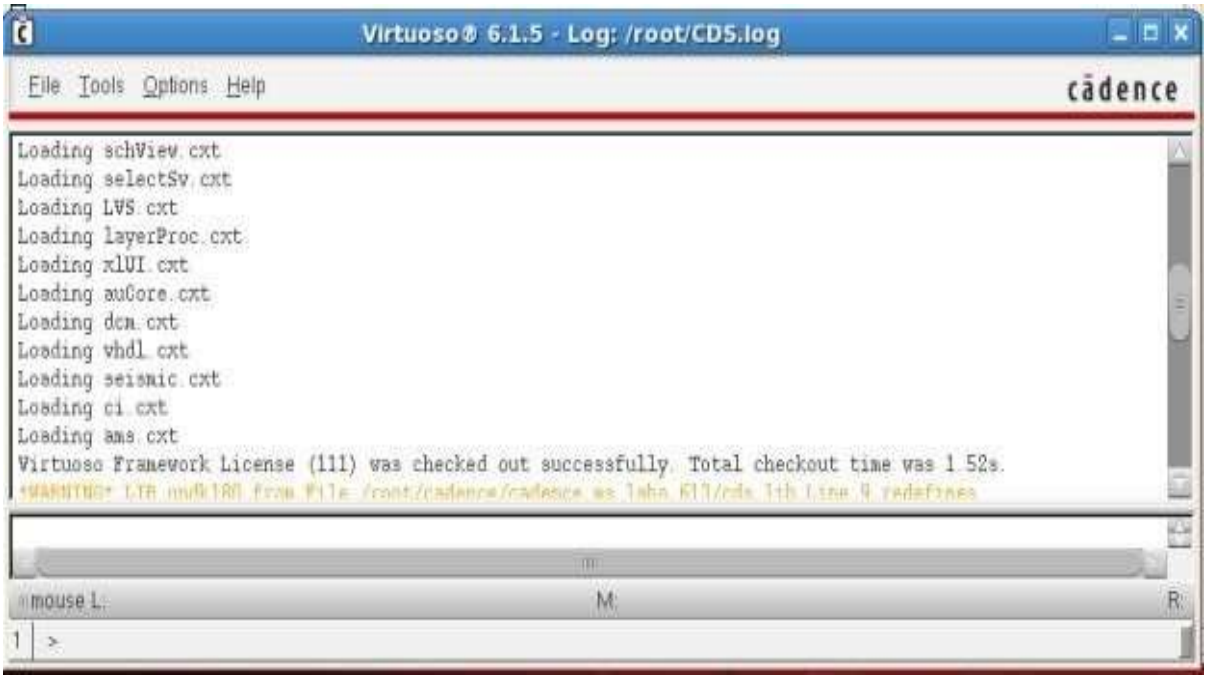


Fig 5.2: Cadence virtuoso (CIW) window

For more data on the different Cadence tool I encourage you to read the corresponding user manuals. You can get to the manuals by pressing Help - > Virtuoso Documentation on any Cadence window (e.g. CIW) Now we have to make another library (to contain your circuits) so from the Virtuoso (Fig 2) Command Interpreter Window (CIW).
go to File - > New - > Library from the File menu. You will see "Another Library" window

3). Fill for the sake of the new library (e.g. CMOS Inverter) in the exchange window (this will make the library in the directory where you began "Virtuoso", you could likewise set a way in the event that you needed another directory). Tap on "Attach to existing tech library" and snap OK.

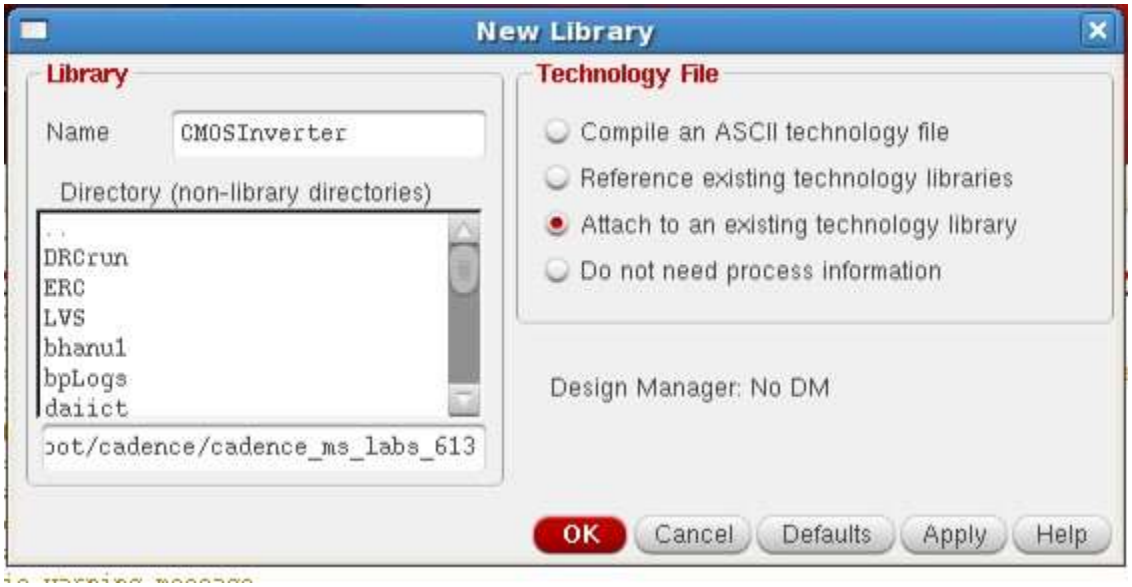


Fig 5.3: New Library Window

The above advances can be equally performed utilizing the Library Manager. After you begin Cadence and get the "Virtuoso CIW" window, go to Tools->Library Manager or press F6 on console. It will open the Library manager window (Fig 4) as established as follows. You can make the new library (CMOS Inverter) from the Library Manager following an impossible to differentiate strides from clarify previously. Presently the "CMOS Inverter" library ought to show up in the Library Manager

window. It is less severe to work with Library Manager. In any case, for this report we will work through Virtuoso-CIW window. Let's start our first schematic now!

How about we begin our first schematic at this point!

Schematic Capture

In the Virtuoso CIW window go to File - > New - > Cell View. You will get a "Make new record" window (Fig 4). Fill in the data in the discourse window as underneath and after that press OK.

Library Name: CMOS Inverter

Cell Name: my inverter (you can choose other name if you want)

View Name: Schematic

Tool: Composer-schematic

Fig 5.4: Create New File window

Sit tight for some time. "The schematic window will show up. You ought to get the "Virtuoso Schematic Editing" window as demonstrated as follows (Fig 5). Invest some energy dissecting the window. On the left side you have different easy routes to regular utilized summons, for example, putting segment occurrences (resembles an IC), drawing wires, setting ports, extending, replicating, zooming in and out, sparing, and so forth. On the off chance that you pass the mouse pointer over

the catches you get short fly up help messages. You likewise approach these orders (and others) from the menu. It isn't conceivable here to portray all the usefulness of Virtuoso Schematic so you are emphatically urged to peruse the on-line client manuals. you should see that the best bar of the window will demonstrate the name of the library (CMOSInverter), cellview (myinverter) and toward end.

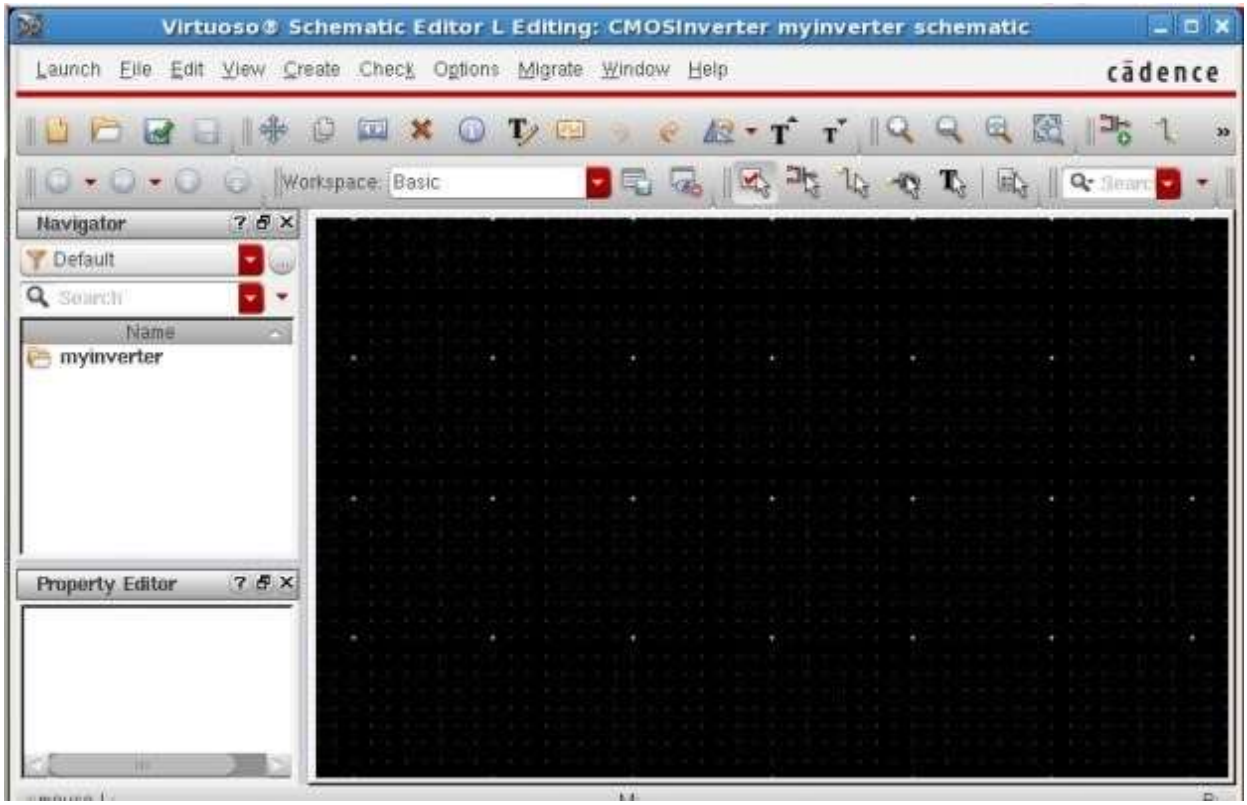


Fig 5.5: Virtuoso Schematic Editing window (Composer)

How about we start our primary diagram to make the CMOS Inverter. Build up the Virtuoso Schematic upgrading window if original. We will have the capacity to % the NMOS and PMOS transistors on the schematic.

Placing instance.

Click on the “Instance” switch (icon) on the left side (which looks somewhat like an IC, or go to Add -> Instance), this will pop-up an “Add Instance” window (Fig 5.6).

Fig 5.6: Add Instance Window

Presently tap on the Browse. Another window called "Library Browser

– Add Instance" (Fig 5.6) will fly up. We will choose PMOS transistor and will put it on the Virtuoso Schematic window. Take after the means now. Select as follows in the Library Browser window (Fig

5.7).

Library =>gpdk180

Cell =>pmos

View =>symbol

Fig 5.7: Library Browser window

Change following properties of pmos in “Add instance” as given here.

Names => M1

Width =>800 nm

Length => 180 nm

Essentially, now we will put the NMOS transistor. Backpedal to the "Library Browser-Add Instance" by left tapping on this window. Select as takes after:
Library =>gpdk180

Cell => nmos

View => symbol

Notice deliberately. You have to choose "nmos" under the cell for NMOS. Presently tap on the "Include Instance" window. Change following properties of the nmos in the "Include example" window.
Names => M2, Width => 360 nm, Length => 180 nm.

Ok, you have NMOS and PMOS on your schematic. So far so good!!!!

To change the parameters of the case, select the occasion (by tapping on it with the mouse) and afterward utilize "properties" symbol or press "q".Presently we likewise need to include wires, I/O sticks and power supply. To begin with we should include wires (limit) to interface

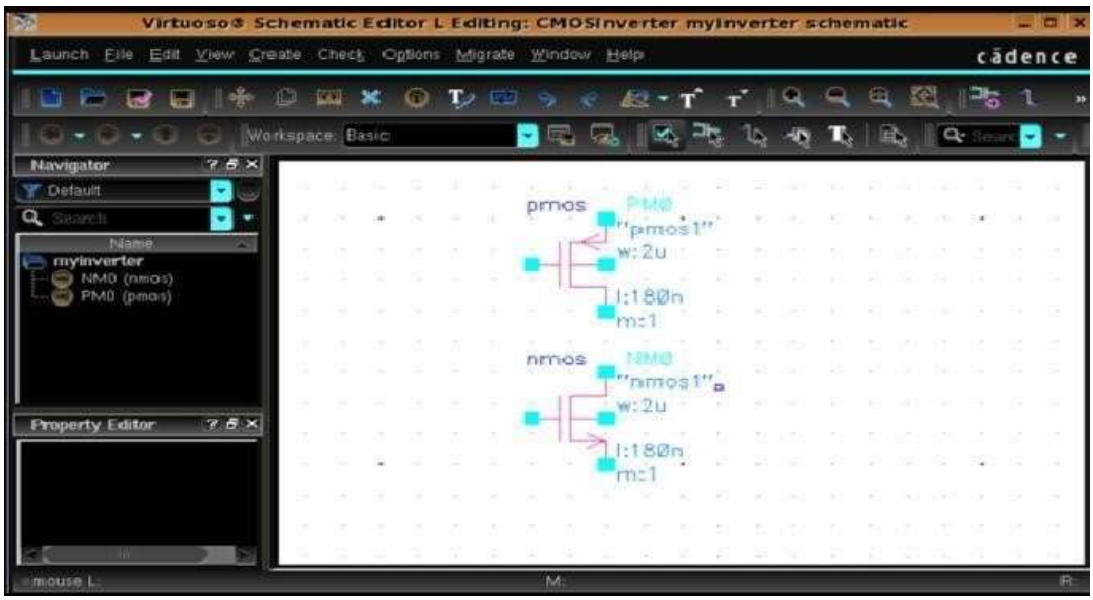


Fig 5.8 NMOS and PMOS on schematic

transistor's terminals and frame a schematic of the CMOS Inverter.

Connecting Wires To associate the wires, tap on the symbol "Wire (limit)" on the left side. You will see an "include Wire" window. You can pick the shading whatever you need to. Presently enact the Virtuoso Schematic Editing window by tapping on its title bar. Move the mouse over or tap on the s key on your console. This snaps the wires to interface between the little precious stone shapes showing by the hubs. You can tap on the hub (diamond shape) with left mouse catch, move the mouse over (you will see wire joined) and after that double tap at opposite end to interface wire between those focuses. Interface every one of the wires like manner. When you are done hit "Esc" on the console. You can erase undesirable wires if associated incidentally. To erase the wire, select that wire by left mouse snap and afterward hit Delete on the console.

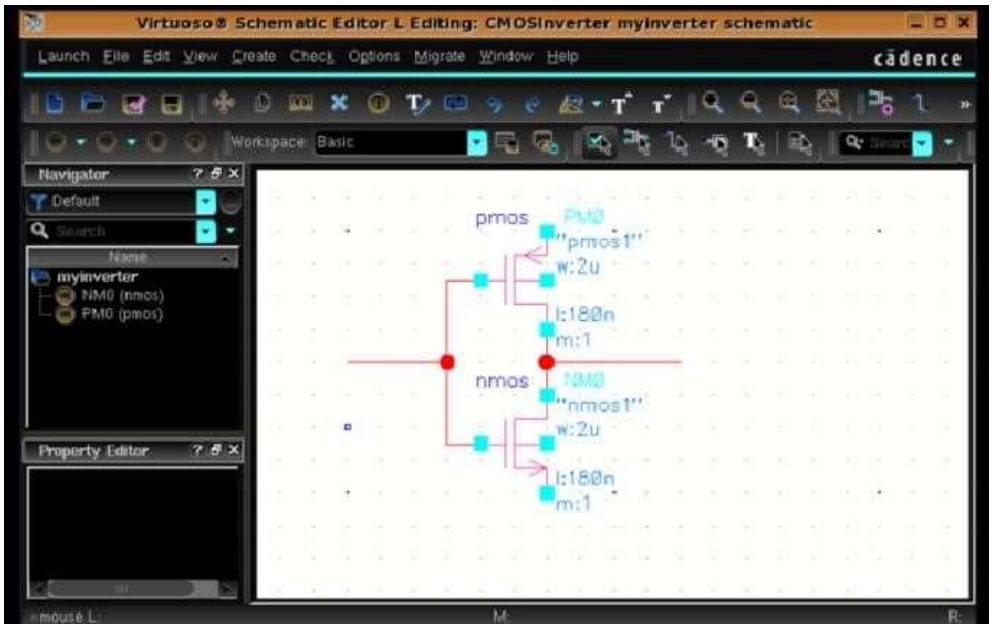


Fig 5. 9: CMOS with no pins

Let's connect the I/O pins now.

Adding Pins

To include the center and yield pins, tap on the "Stick" symbol at the scale down left corner. The "Include Pin" shape shows up. below the Pin

title shape Vin. Note that course in the sort peruses giving, as established underneath (Fig 5.10).

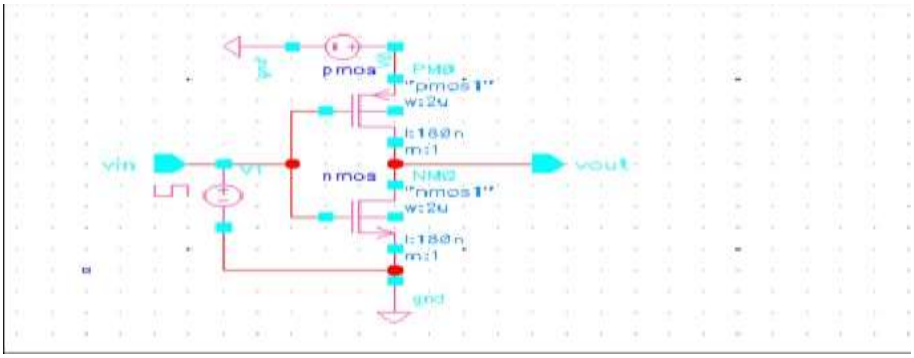


Fig 5.10 CMOS with pin, gnd and supply (Vdd)

The last diagram should look to some degree like this (Fig 17).

Victory? It's a smart thought to spare your plan now and again on the off chance that the framework crashes.
The lot worked fine so far!!!! Praise!!!

Check and Save

Currently you need to check and shop your plan (both tap the upper left catch and go to Design - > confirm and shop). Make sure you appear at the "Virtuoso" CIW window and there aren't any bungles or notice, if there are any you must backpedal and fix them! The Virtuoso window will give the message as established below. "Schematic" decides finished without a mistake. "CMOS Inverter my inverter schematic" spared.
We should now take an notice in the renewal on the inverter circuit to peer the ultimate result!!!

Inside the Virtuoso diagram window go to Launch ADE L Then you will get the play window or ADE fly up window
If you don't mind see Fig. 5.11

Devices - > Analog Environment. You will get "Virtuoso Analog Design Environment (1)" window (Fig 12).
In the Virtuoso Analog Design Environment, go to "Setup - > Model Libraries… … ".

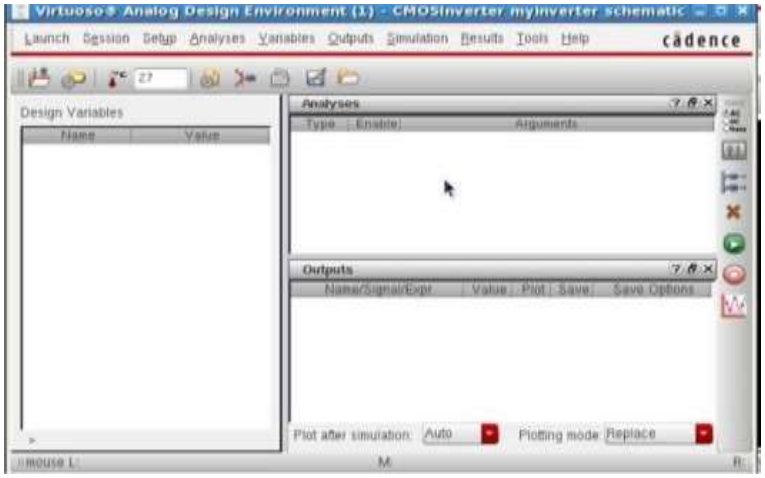


Fig 5.11 ADE Window

currently you should prefer the type of duplicate. From "Virtouso Analog Artist"(Fig thirteen) go to Analyses - > settle on... (Fig thirteen). On this case we will pick a transient assessment. Enter the stop time for transient test. How about we sort 200p for cease time. Tap on adequate.

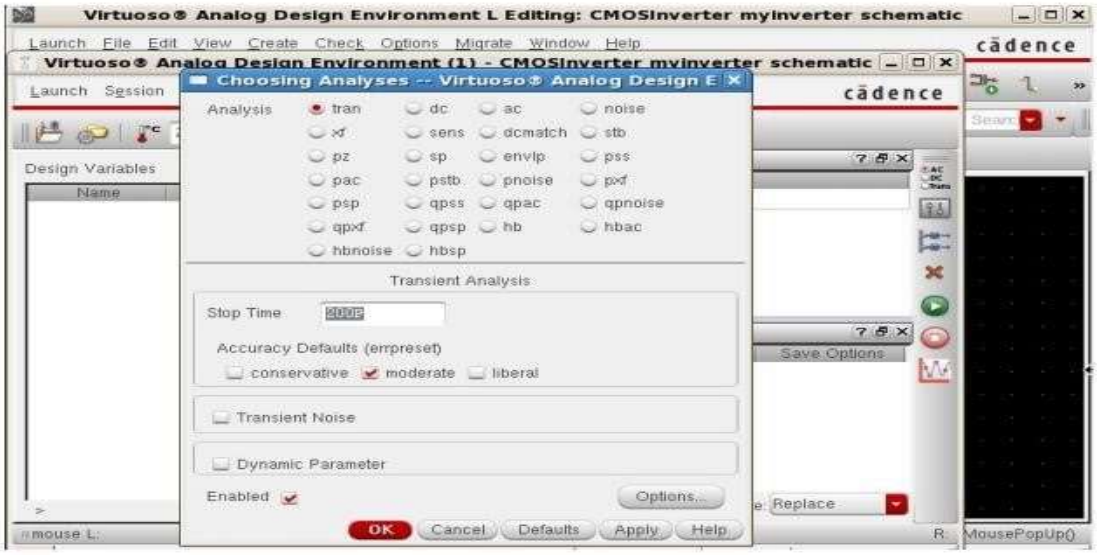


Fig 5.12 Choosing Analysis (Transient Analysis)

For DC analysis, please see the Fig. 14.

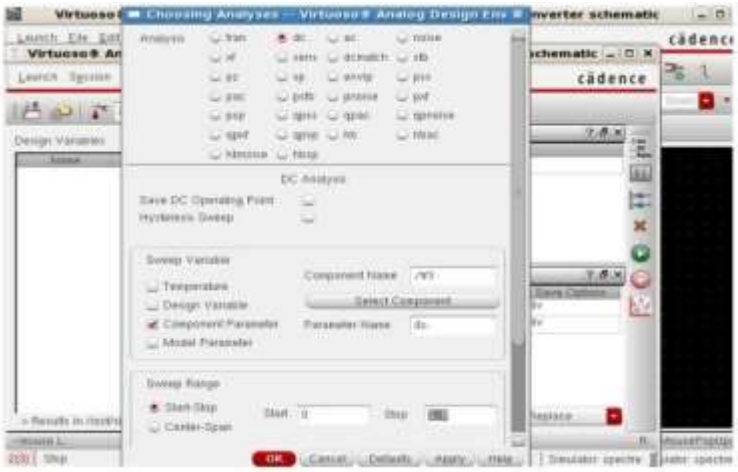


Fig 5.13 Choosing Analysis (ac or dc analysis)

Presently in the "Virtuoso Analog Artist" (Fig 15) go to "Yields - > to be plotted - > pick on diagram". With a reason to express your inverter phone see window in entrance. Favor hub voltages by method for patter on the web. We can tap on in order and yield nets (wires) to choose enter and surrender voltages. The streams may equally be chosen by means of tapping on the terminal (red squares).

CHAPTER – VI

SIMULATION AND RESULTS

6.1 Simulations:

The circuits mentioned above are constructed using Cadance Virtuoso tools.

6.1.1 Simple Inverter using CNTFET:

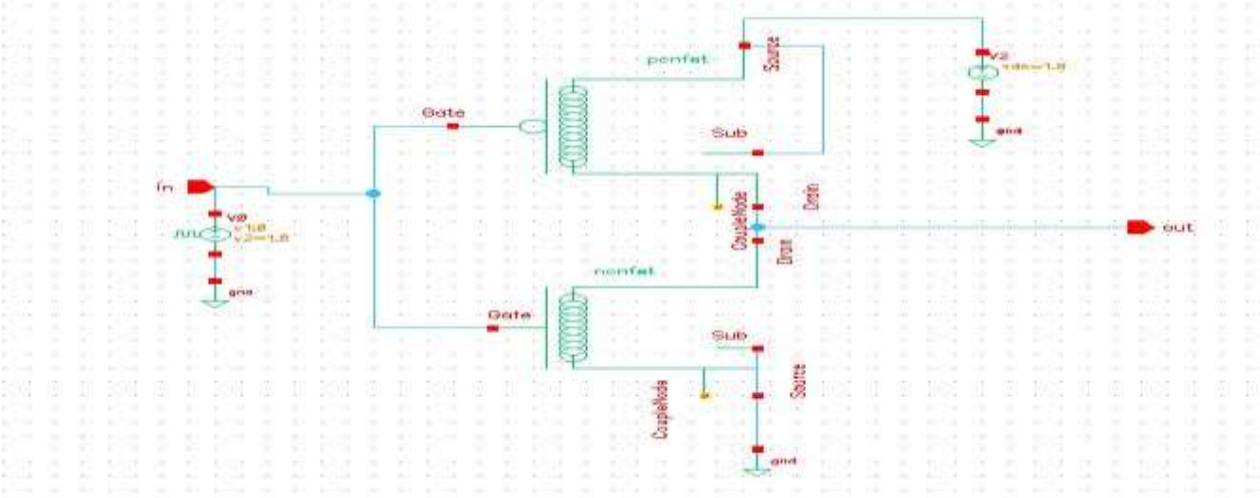


Fig 6.1: CNTFET Inverter in Cadence Tools

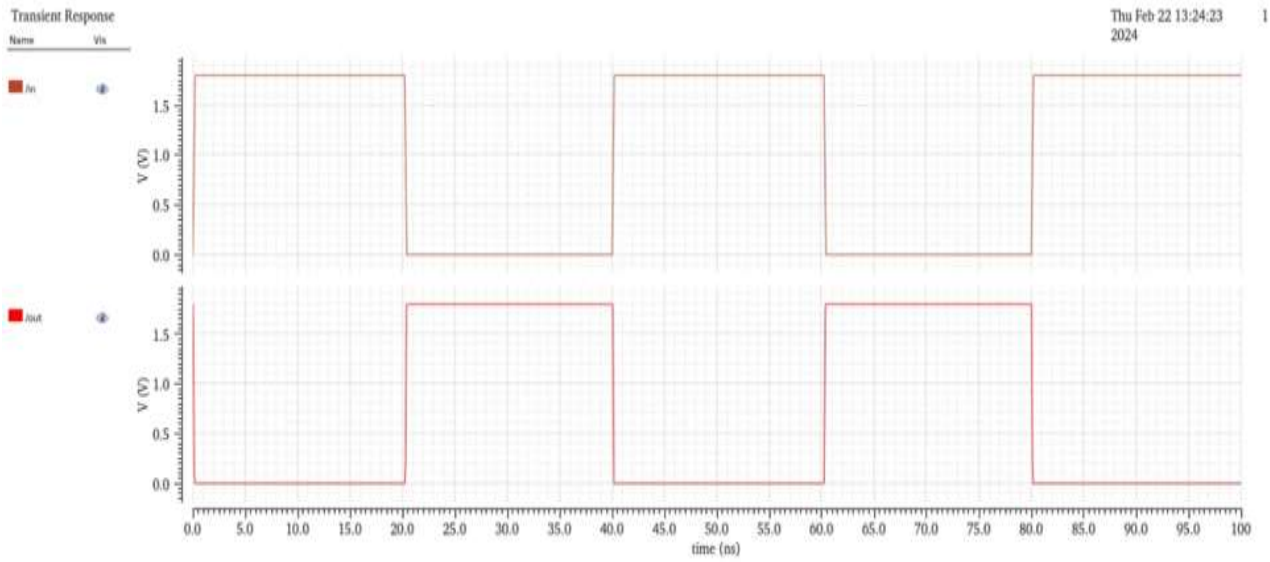


Fig 6.2: CNTFET inverter Waveforms

6.1.2 Simple Inverter using MOSFET:

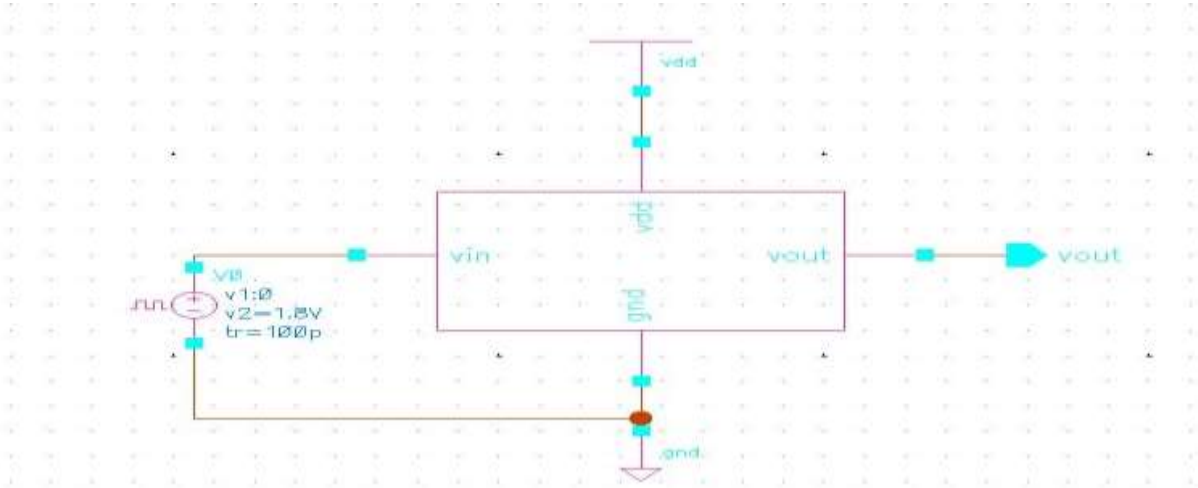


Fig 6.3: CMOS Inverter in Cadence

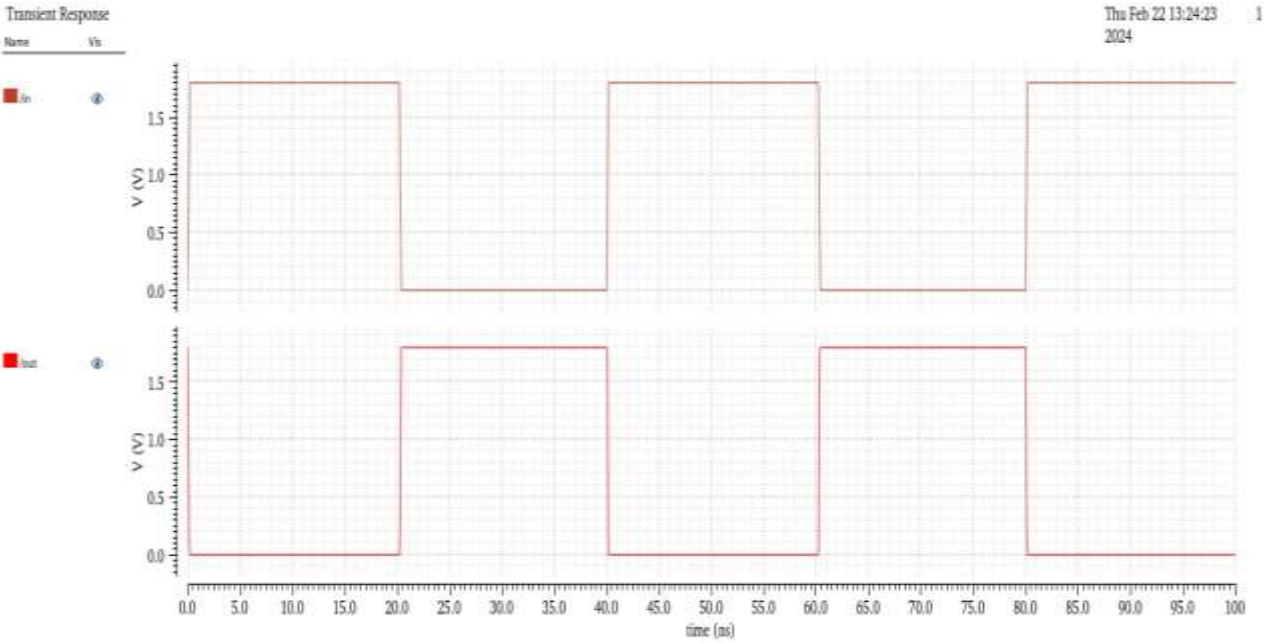


Fig 6.4: CMOS INVERTER waveforms

6.1.3 Transmission Gate using CNTFET:

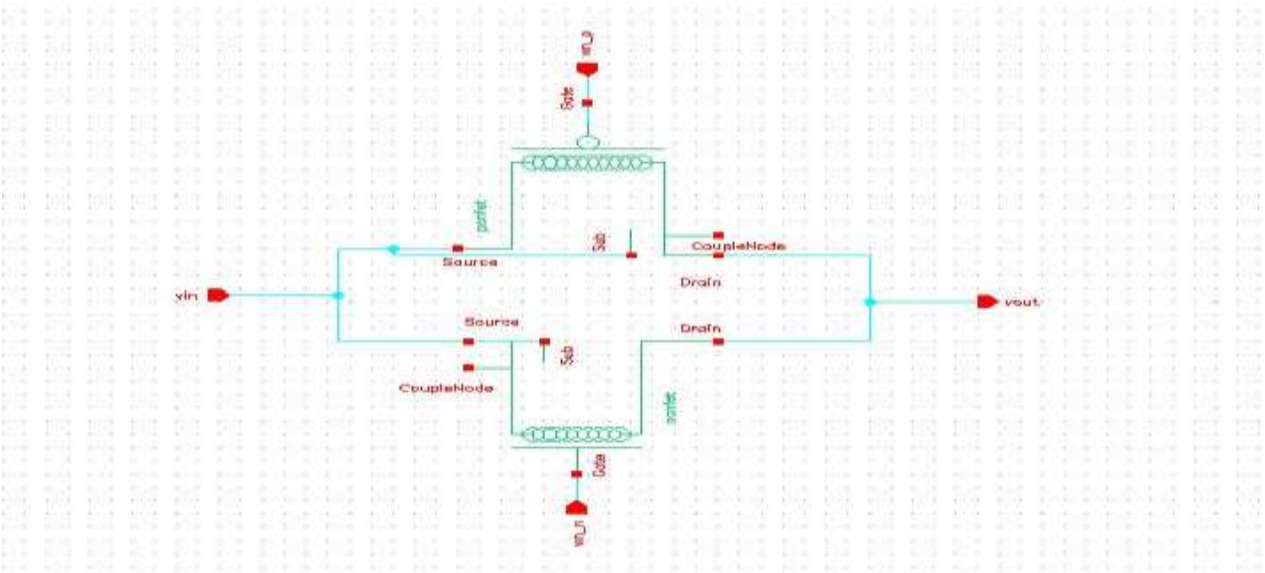


Fig 6.5: Transmission gate in Cadance tool

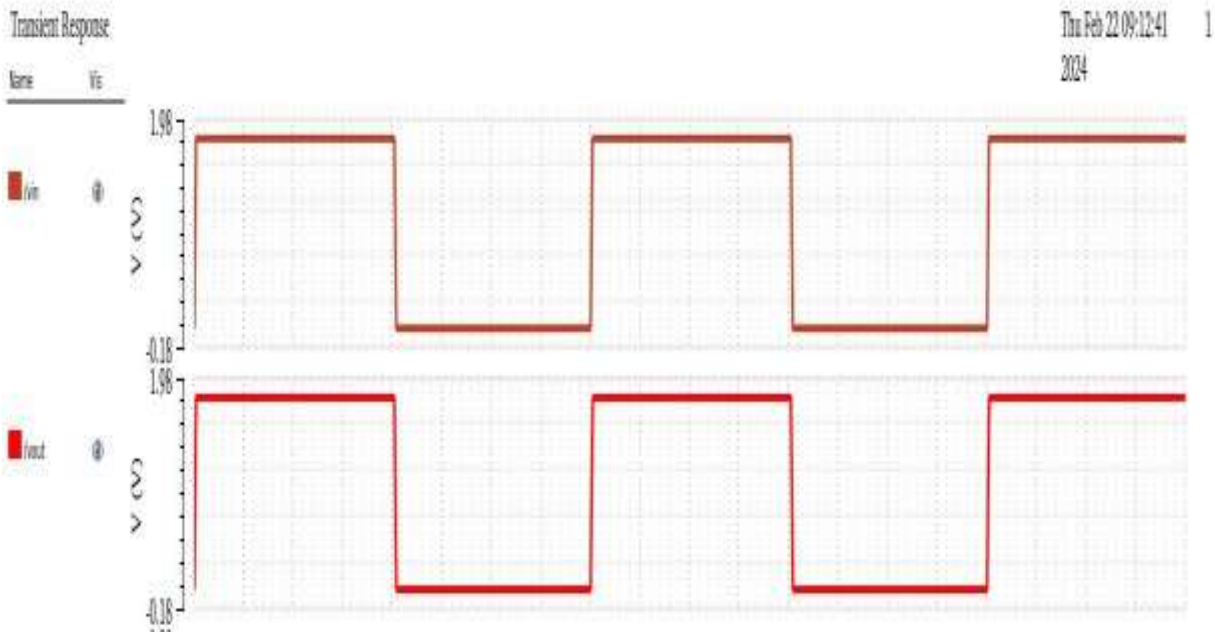


Fig 6.6: Transmission gate Waveforms

6.1.4 Transmission Gate Using MOSFET:

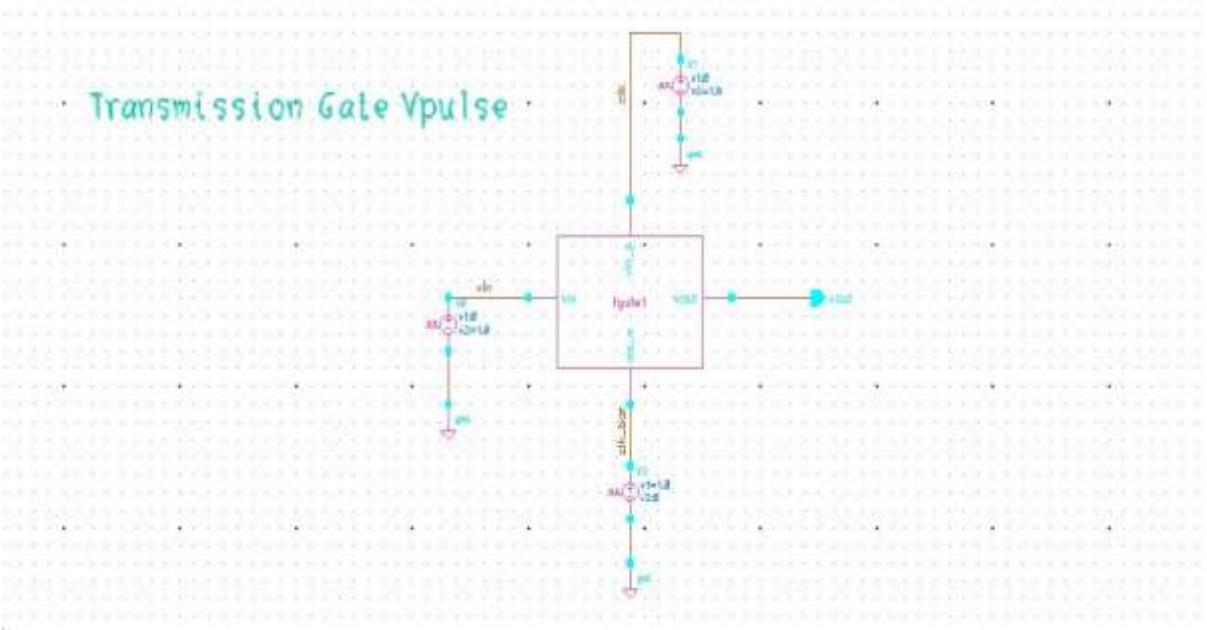


Fig 6.7: Transmission gate using MOSFET in Cadence

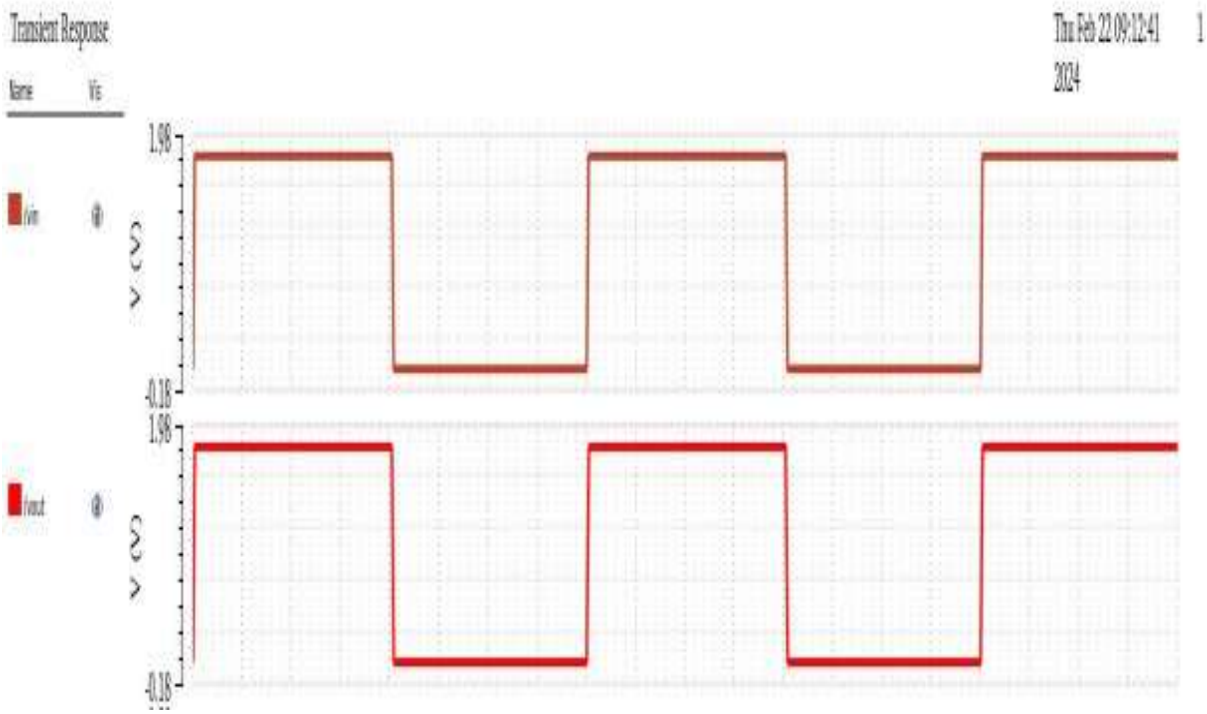


Fig 6.8: Waveforms of Transmission Gate

6.1.5 Standard Ternary Inverter using CNTFET:

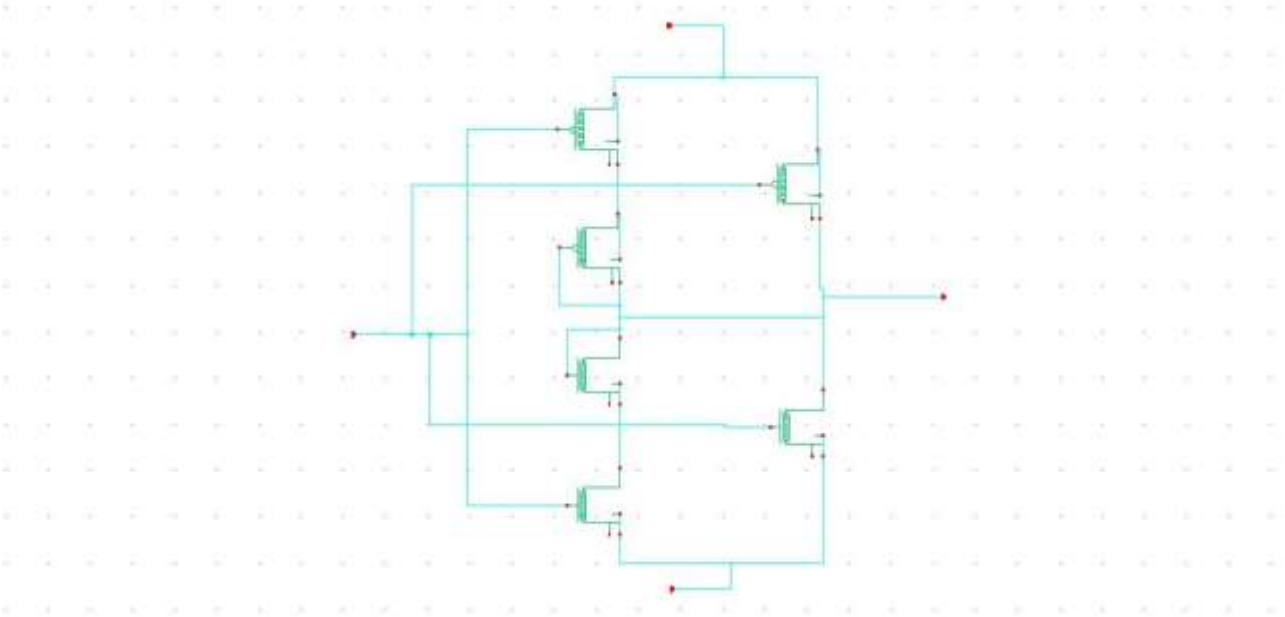


Fig 6.9: Standard ternary inverter in cadence tool

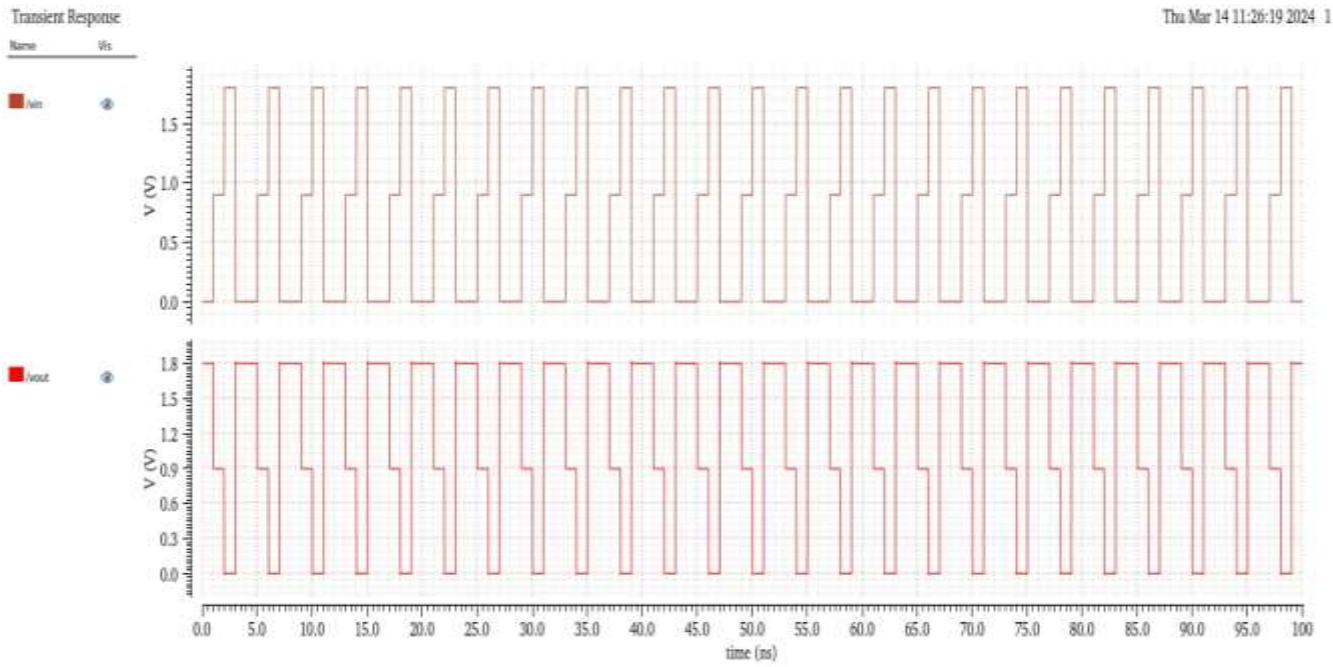


Fig 6.10: Standard ternary inverter waveforms

6.1.6 Standard Ternary Inverter using MOSFET:

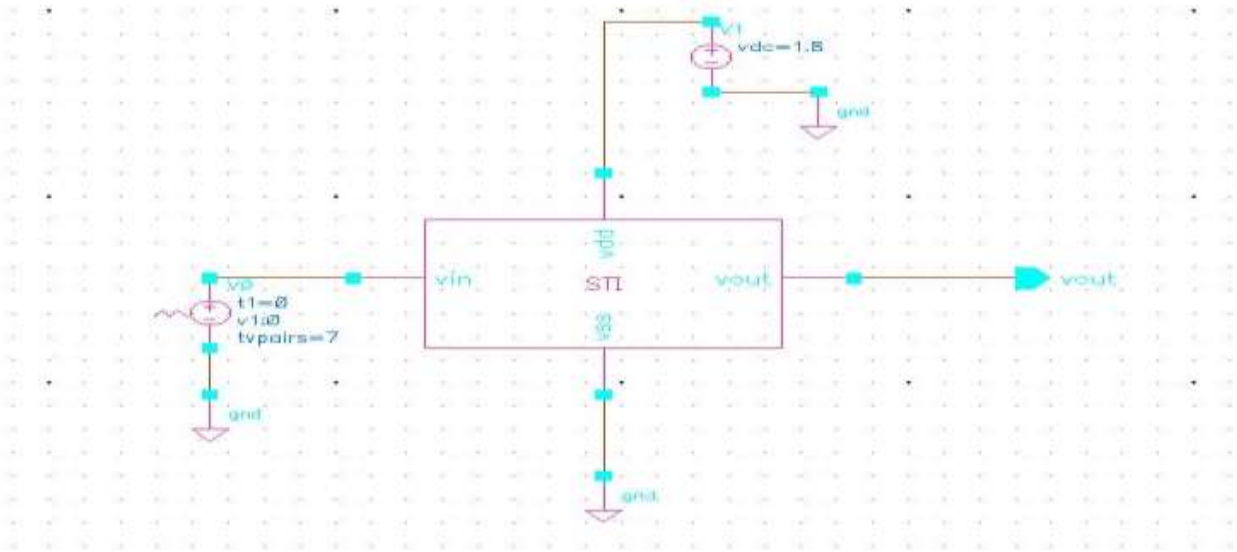


FIG 6.11: Standard ternary inverter in cadence tool

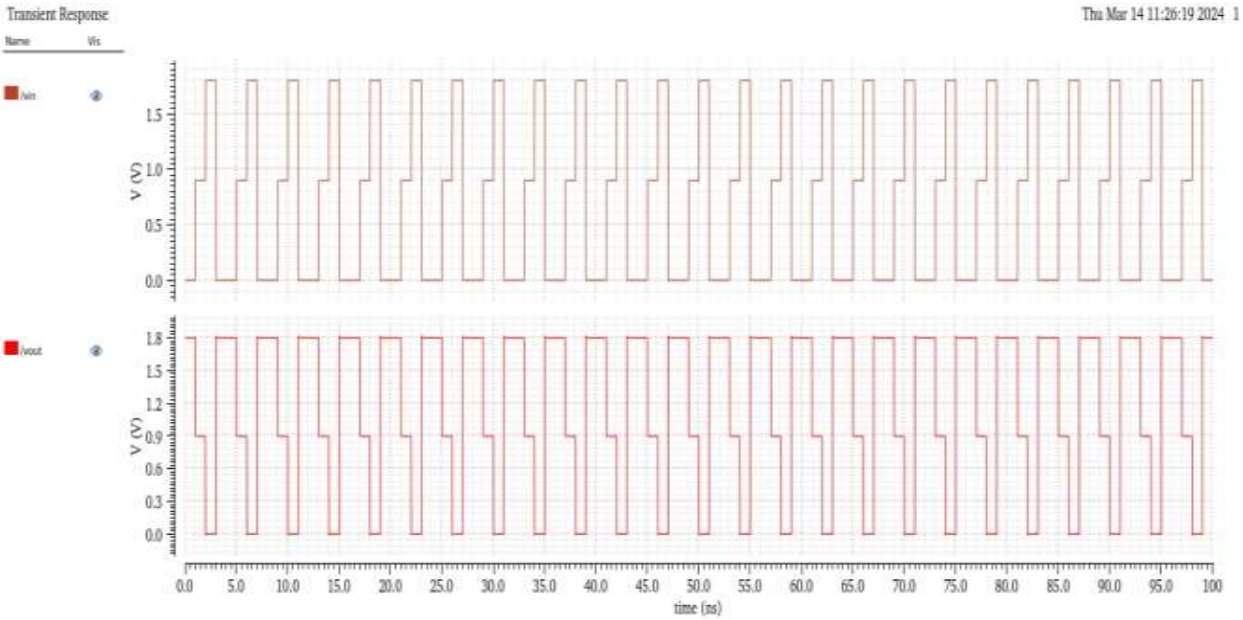


Fig 6.12: Standard ternary inverter waveforms

6.1.7 Ternary Transmission Gate using CNTFET:

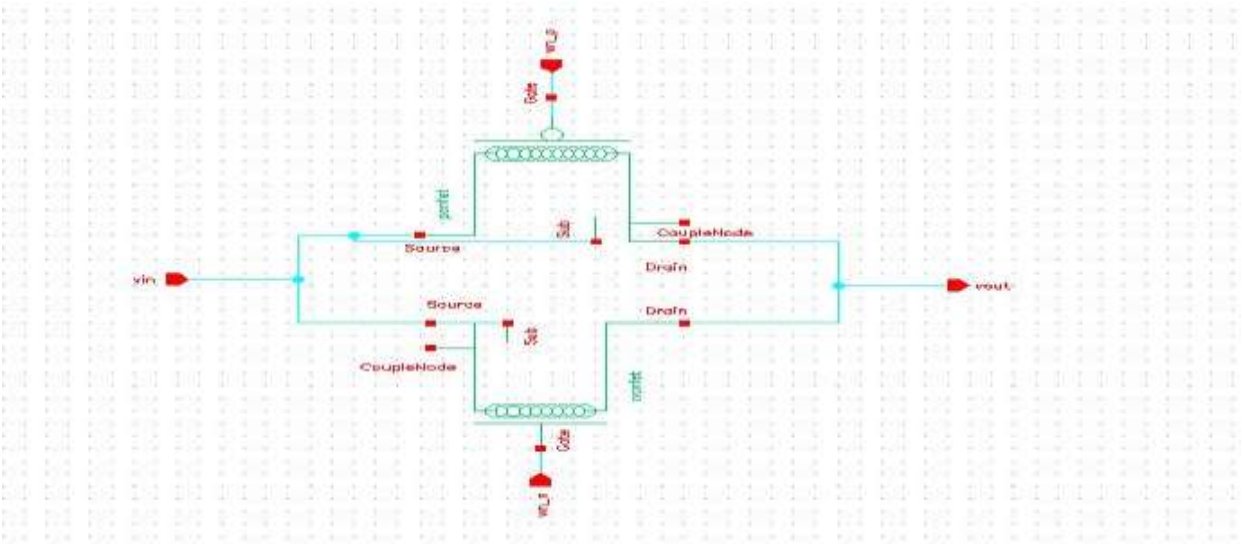


Fig 6.13: Transmission gate using ternary logic in cadence tool

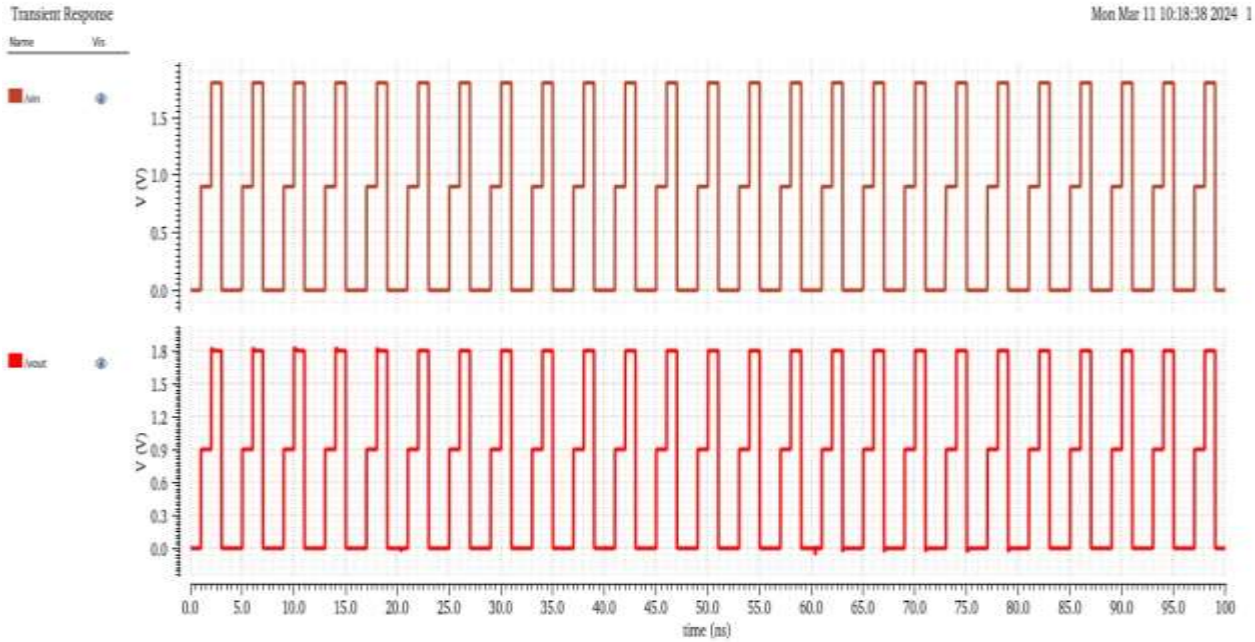


Fig 6.14: Transmission gate using ternary logic waveforms

6.1.8 Ternary Transmission Gate using MOSFET:

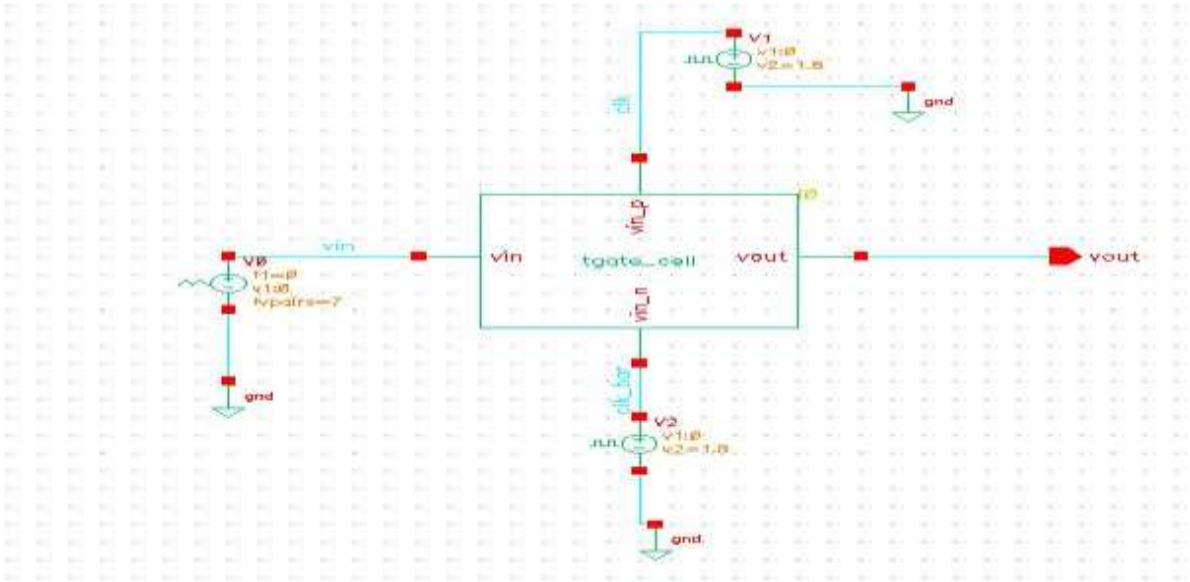


Fig 6.15: Transmission gate using ternary logic in cadence tool

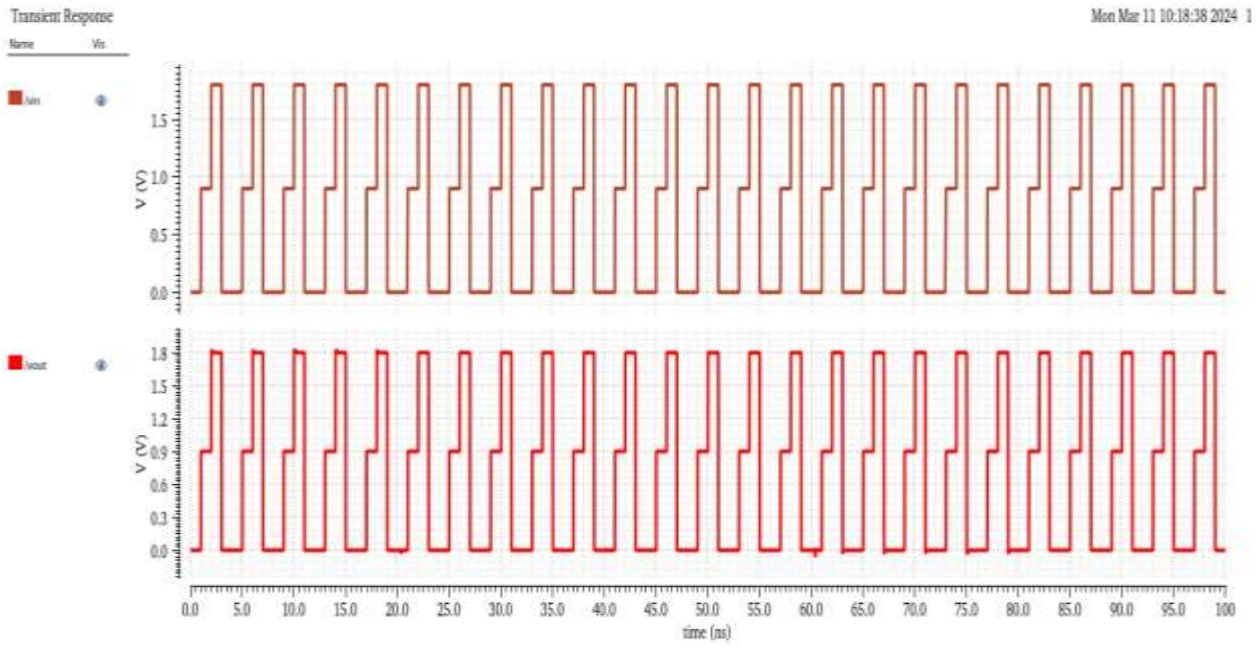


Fig 6.16: Transmission gate using ternary logic waveforms

6.1.9 Positive Latch using CNTFET:

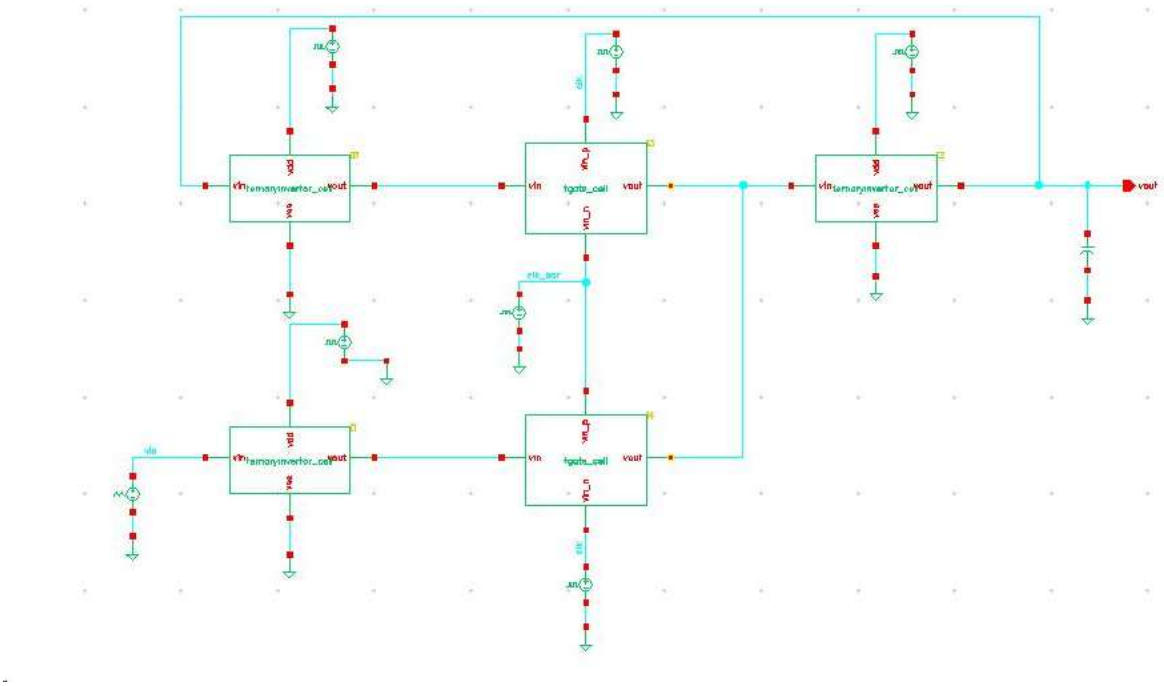


Fig 6.17: Positive latch using CNTFET in Cadence tool

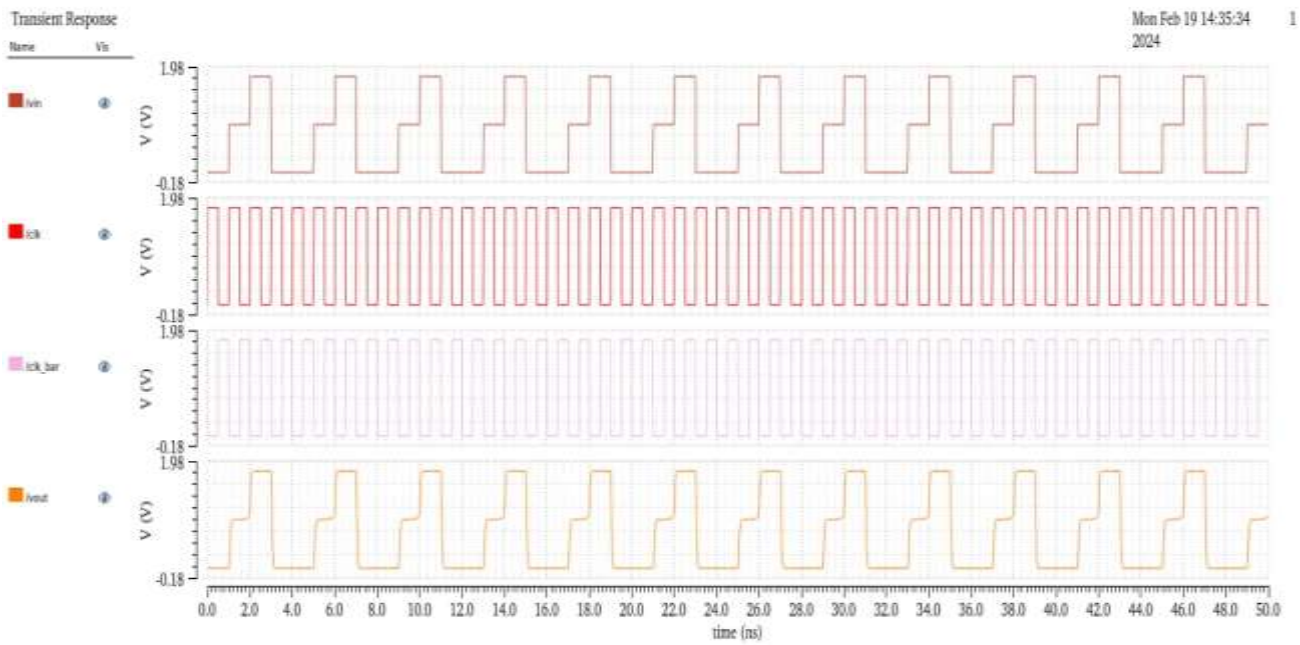


Fig 6.18: Waveforms of Positive latch using CNTFET

6.1.10 Positive latch using MOSFET:

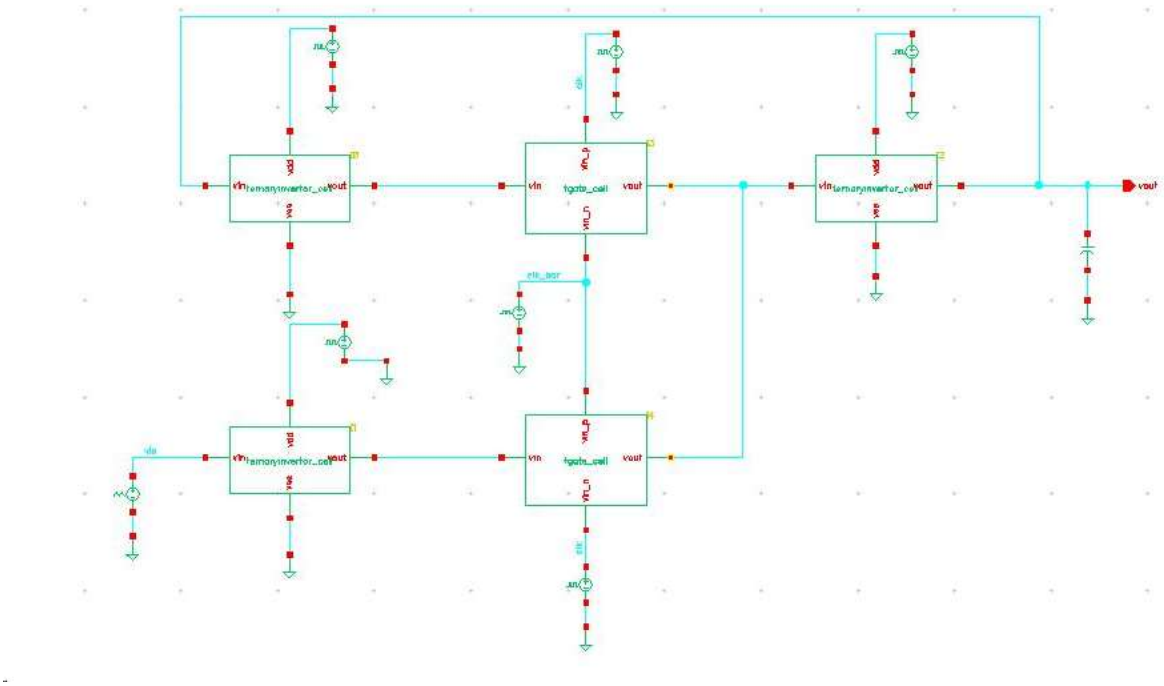


Fig 6.19: Positive latch using MOSFET in Cadence tool

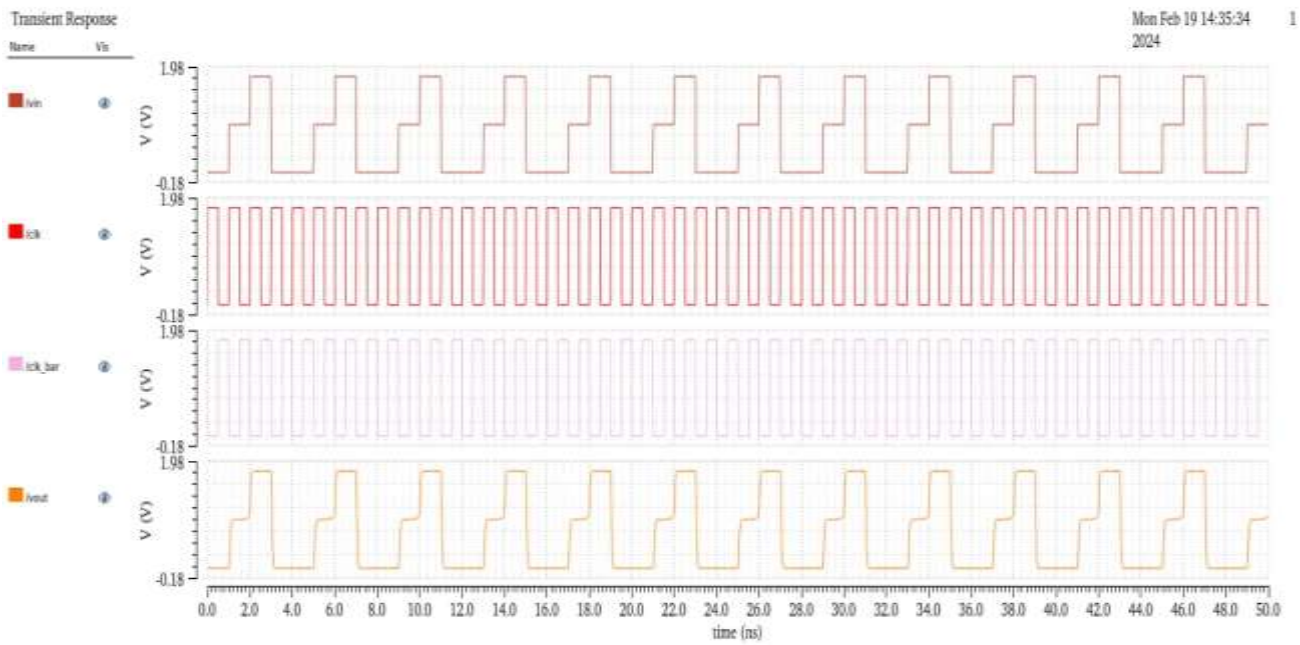


Fig 6.20: Waveforms of Positive latch using MOSFET

6.1.11 Negative Latch using CNTFET:

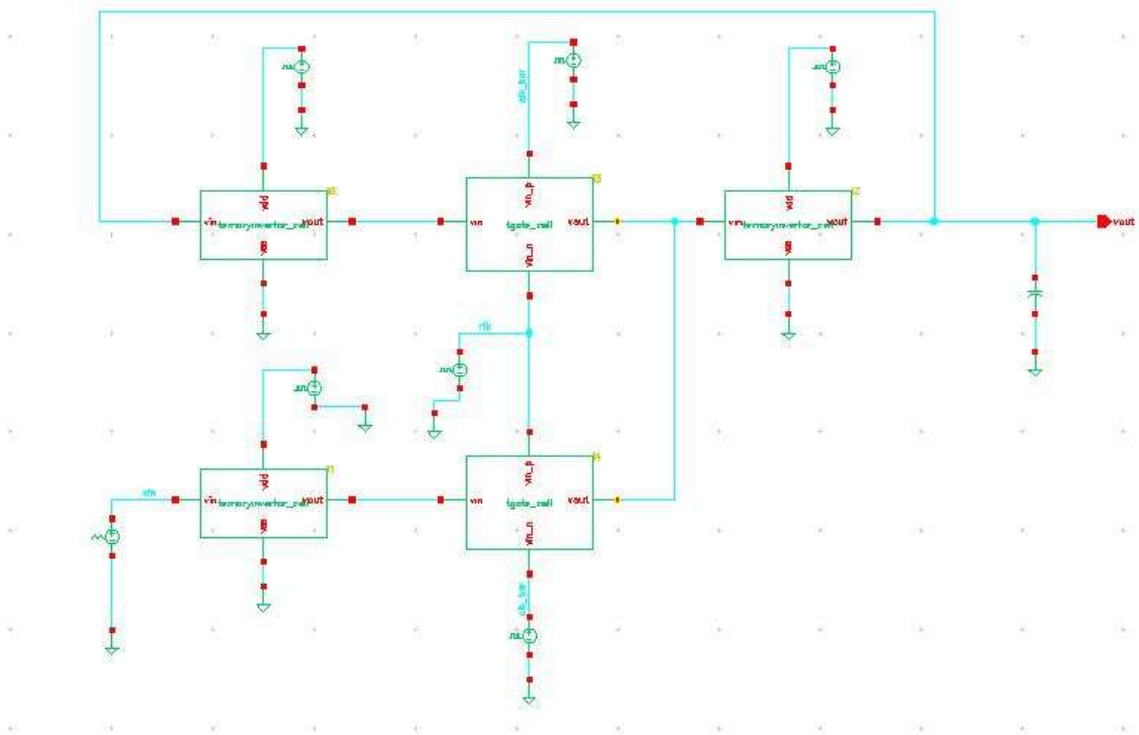


Fig 6.21: Negative latch using CNTFET in Cadence tool

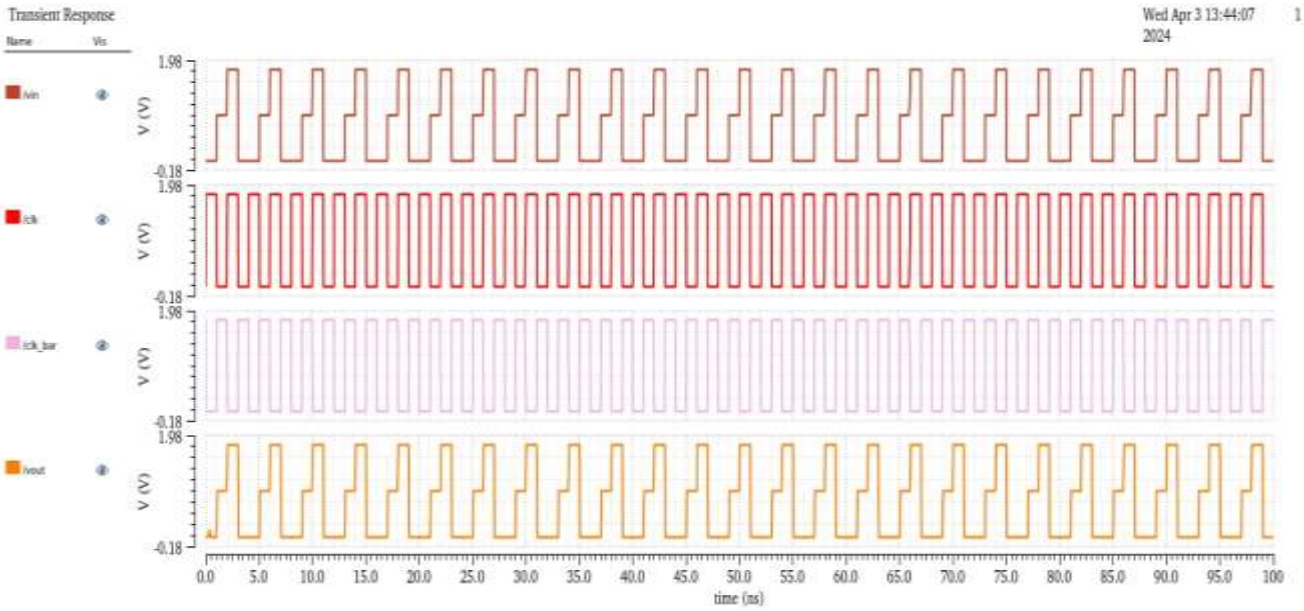


Fig 6.22: Waveforms of Negative latch using CNTFET

6.1.12 Negative Latch using MOSFET:

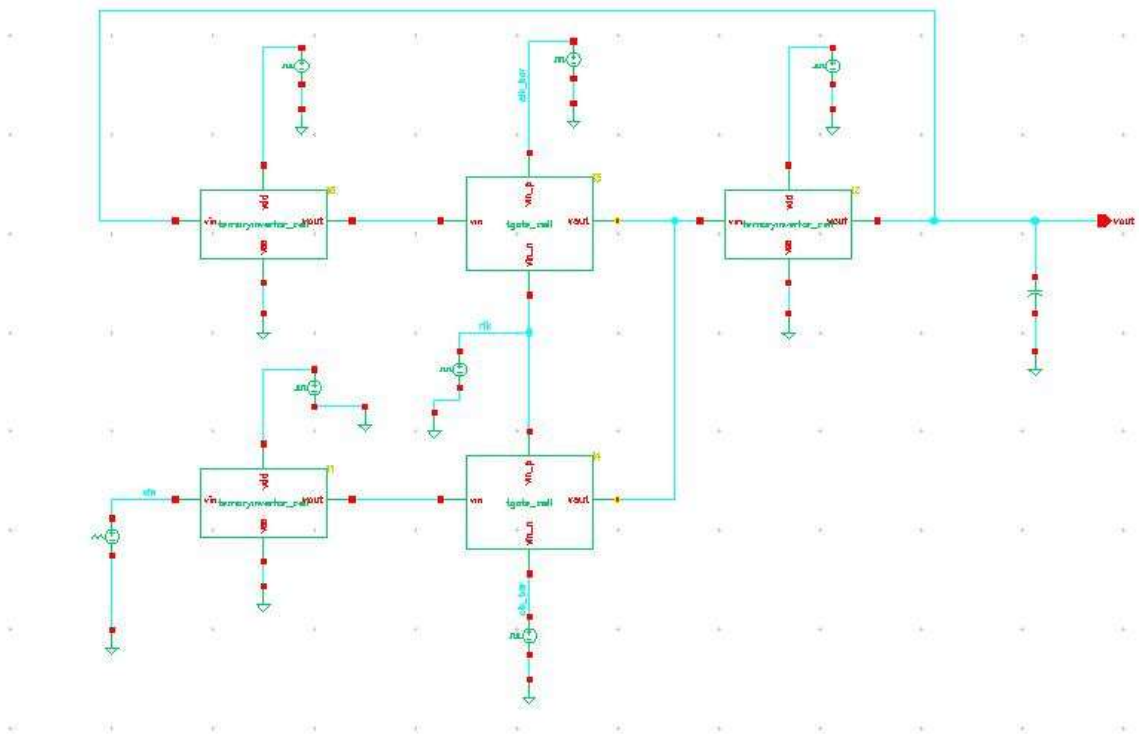


Fig 6.23: Negative latch using MOSFET in Cadence tool

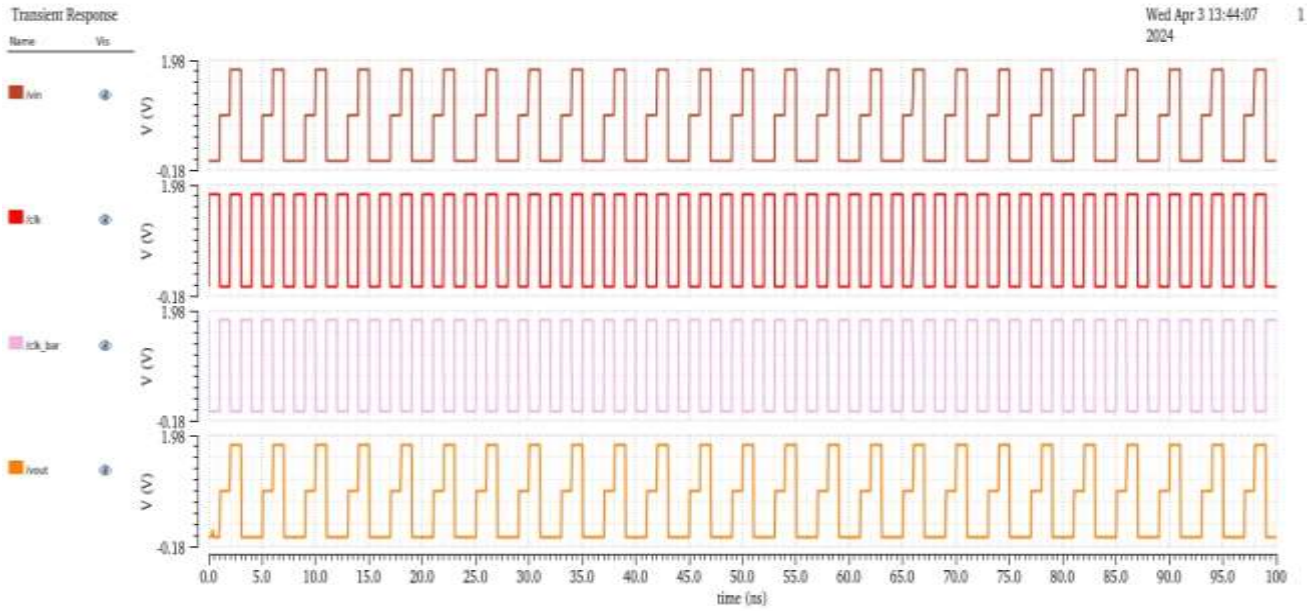


Fig 6.24: Waveforms of Negative latch using MOSFET

6.1.13 Multiplexer based Ternary D-flip-flop using CNTFET:

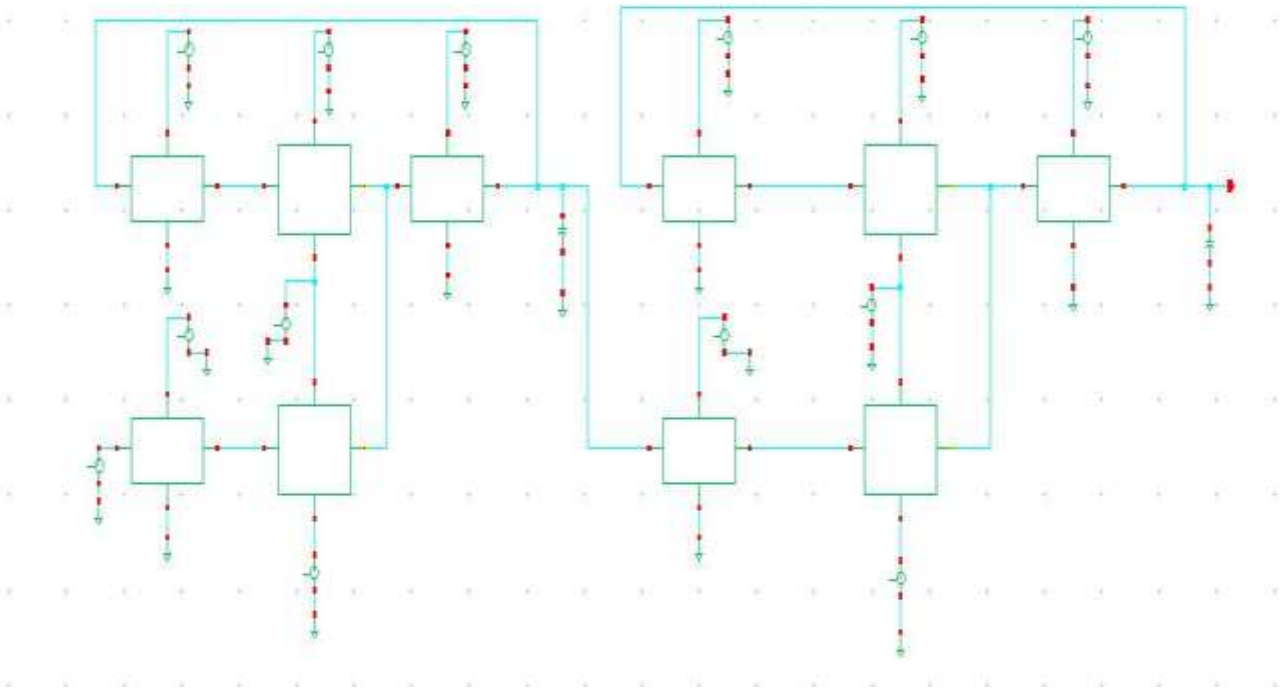


Fig 6.25: multiplexer based ternary D-flip flop in cadence

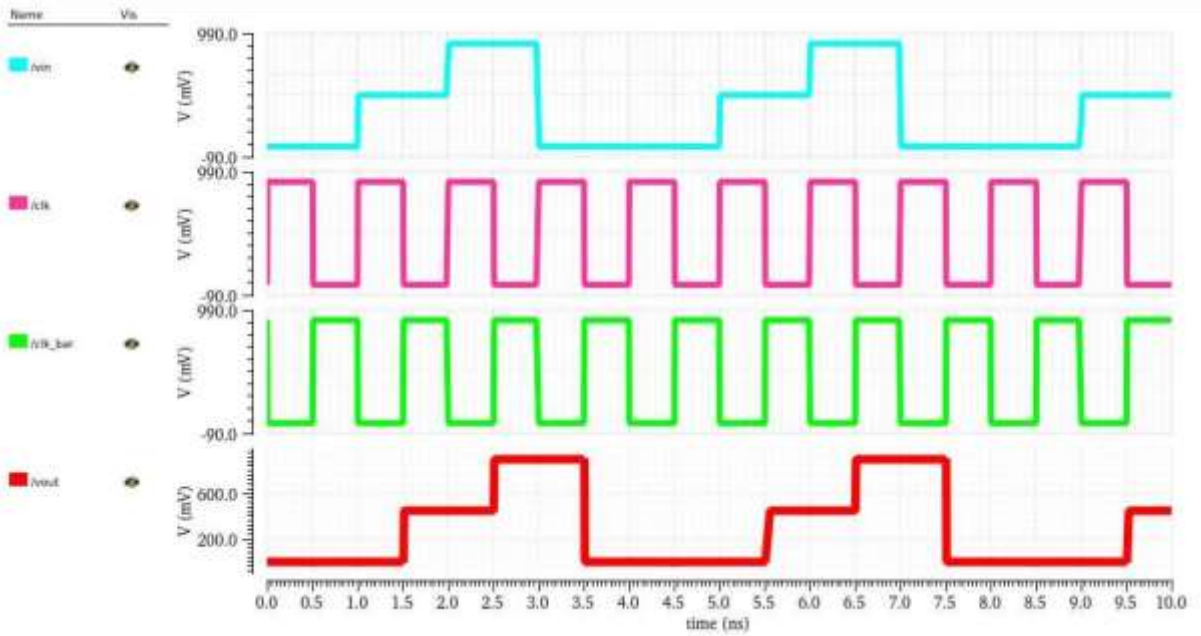


Fig 6.26: Transient response of multiplexer based ternary D-flip flop

6.1.14 Multiplexer based Ternary D-flip-flop using MOSFET:

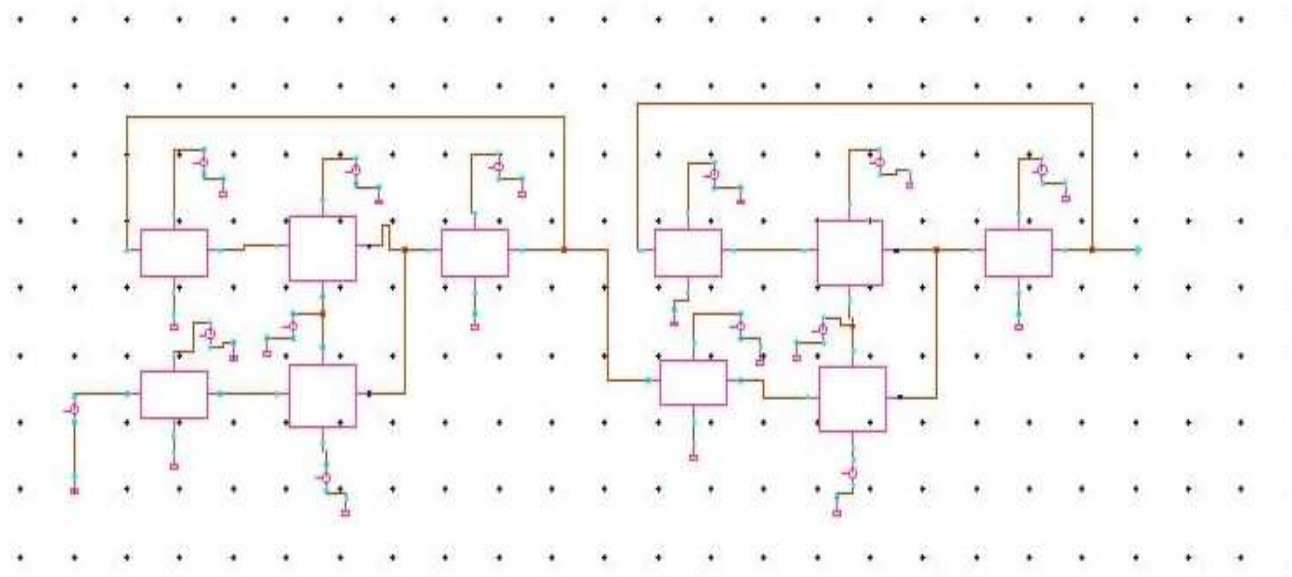


FIG 6.27: multiplexer based ternary D-flip flop in cadence

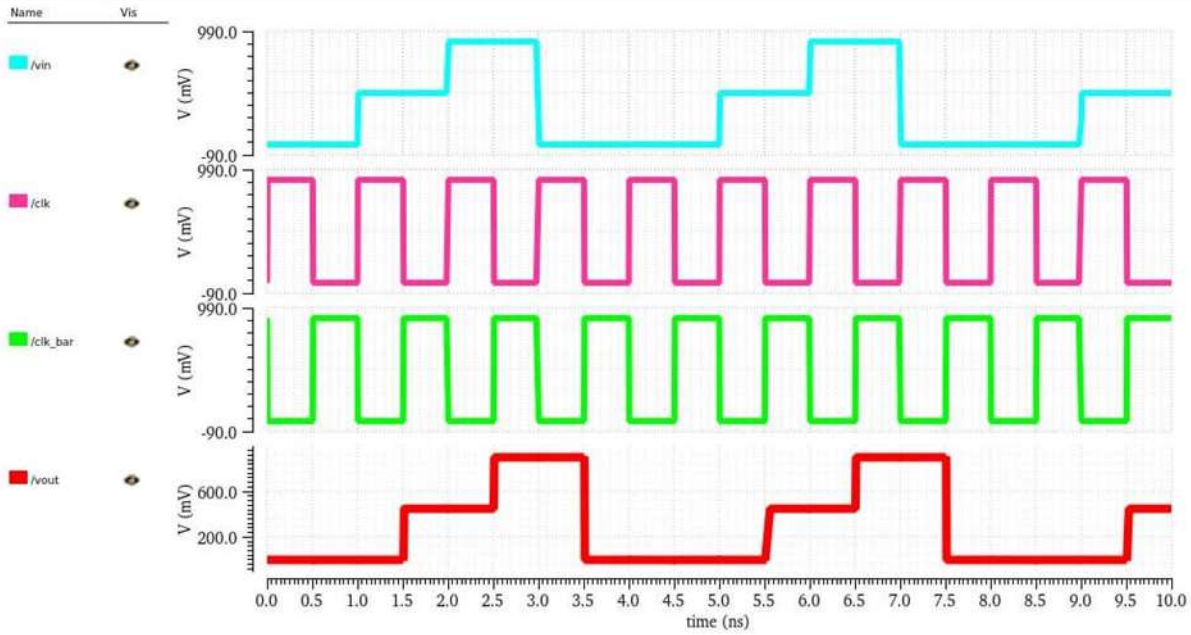


Fig 6.28: Transient response of multiplexer based ternary D-flip flop

6.1.15 SISO using CNTFET:

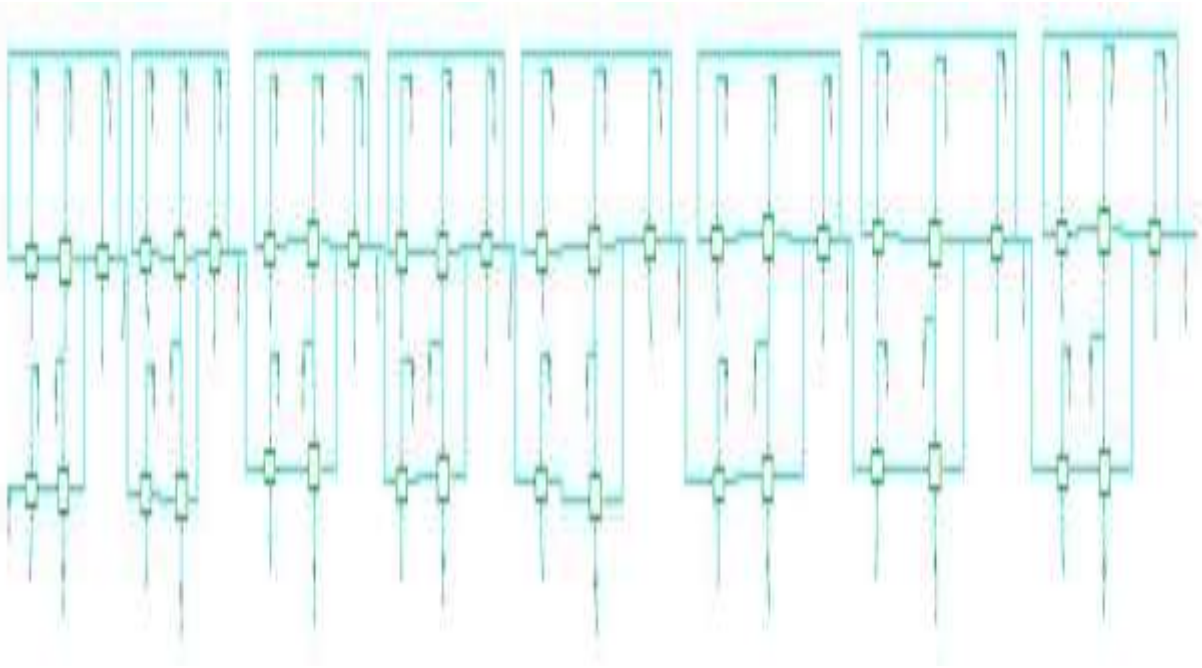


Fig 6.29: SISO in cadence tool using CNTFET

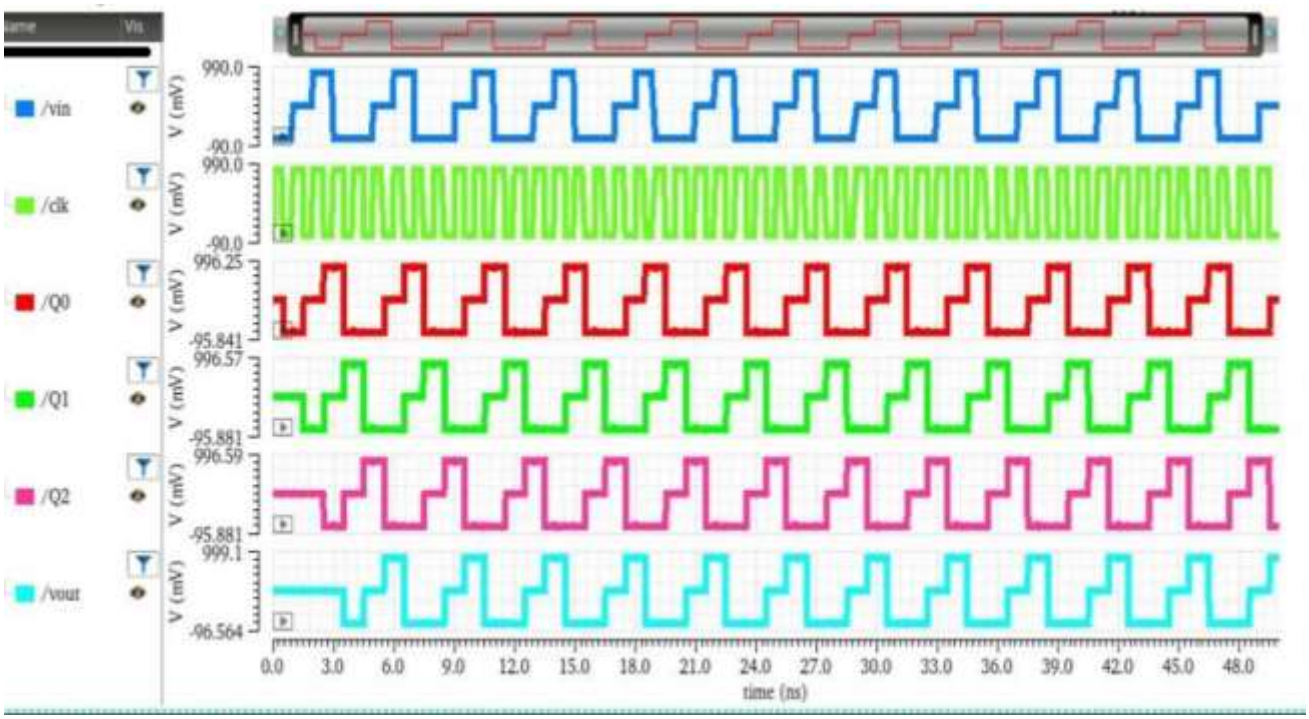


Fig 6.30: Waveforms of SISO in Cadence tool

6.1.15 SISO using MOSFET:

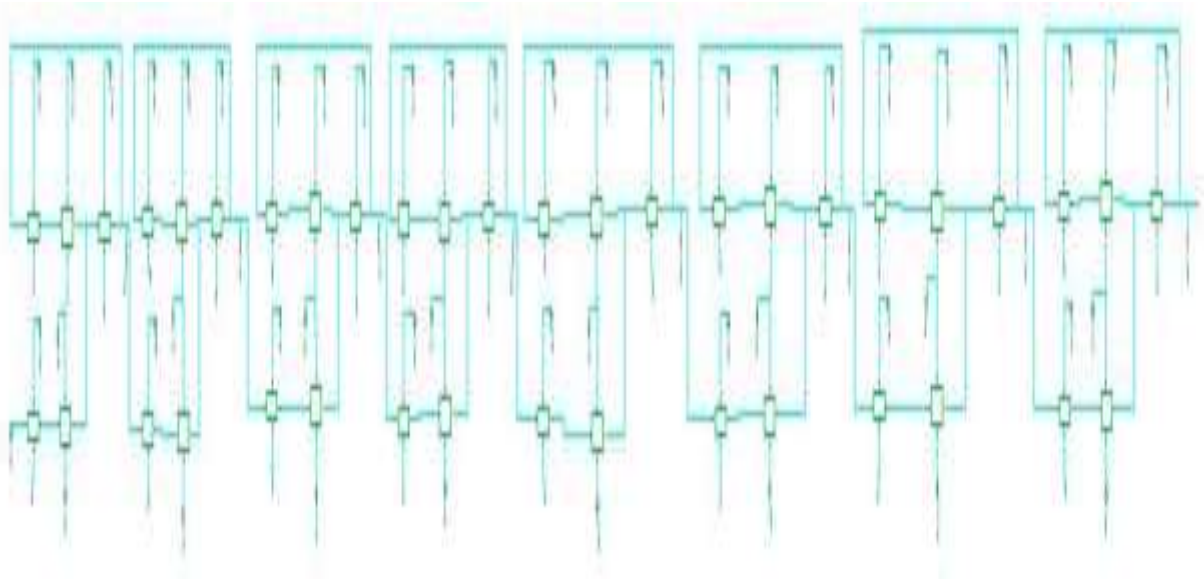


Fig 6.31: SISO in cadence tool using MOSFET

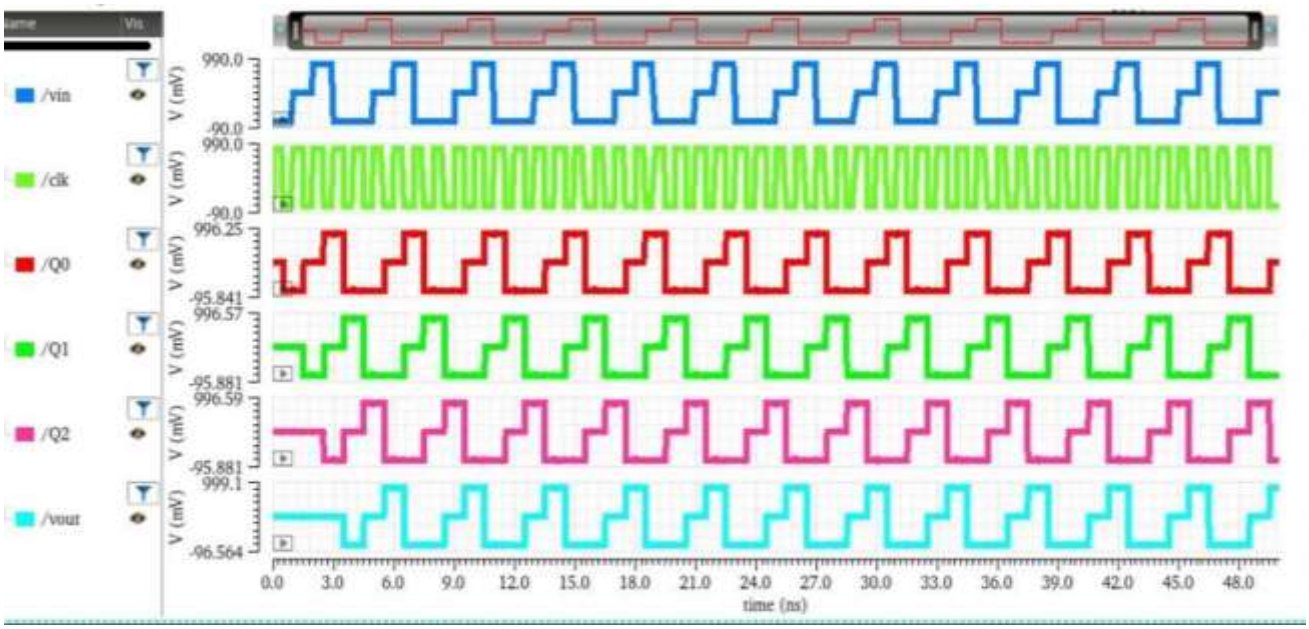


Fig 6.32: Waveforms of SISO in Cadence tool

6.2 Comparative Analysis

6.2.1 Comparison Between MOSFET circuits and CNTFET circuits

MOSFET circuits, composed of a silicon dioxide insulating layer, silicon substrate, and metal gate, have long served as the cornerstone of modern electronics. However, their scalability faces challenges due to issues such as gate leakage and short-channel effects. Over decades, MOSFETs have been strictly optimized for high performance in terms of speed, power consumption, and reliability, making them widespread in various applications. Furthermore, their well-established fabrication processes in silicon technology contribute to lower manufacturing costs. Moreover, MOSFETs are susceptible to reliability issues under extreme conditions, such as high temperatures, radiation, or mechanical stress.

On the other hand, CNTFET circuits represent a promising alternative, leveraging carbon nanotubes as the channel material. These nanotubes offer exceptional electrical properties at the nanoscale, potentially enabling superior scaling compared to MOSFETs. CNTFETs have the potential for higher carrier mobility, leading to faster switching speeds and reduced power consumption. Despite their advantages, the fabrication of CNTFETs involves more intricate processes, including carbon nanotube synthesis and integration, which may contribute to higher manufacturing costs.

6.2.2 Comparison between performance analysis between MOSFET circuits and CNTFET circuits:

Performance analysis between CNTFET circuits and MOSFET circuits reveals notable differences from their distinct material compositions and structural properties. CNTFETs, leveraging carbon nanotubes as the channel material, demonstrate superior carrier mobility compared to silicon-based MOSFETs, potentially leading to faster switching speeds and reduced power consumption. This elevated carrier mobility also grants CNTFETs a promising advantage in scalability, as they can maintain performance at smaller dimensions, whereas MOSFETs face limitations due to issues like gate leakage and

short-channel effects. Additionally, CNTFETs exhibit potential for lower power consumption and enhanced reliability, with carbon nanotubes showing resilience to harsh environmental conditions compared to traditional MOSFET materials. However, the fabrication of CNTFETs involves more intricate processes, potentially leading to higher manufacturing costs compared to the well-established and relatively mature processes of silicon-based MOSFETs.

Table 6.1: Comparative analysis of MOSFET and CNTFET circuits

COMPONENTS	**USING MOSFET**			**USING CNTFET**		
	POWER (mW)	**DELAY (ns)**	**PDP (pJ)**	**POWER (mW)**	**DELAY (ns)**	**PDP (pJ)**
STANDARD TERNARY INVERTER	1.343	2.996	40.23	1.124	149.3E-6	16.78
TRANSMISSION GATE	1.994	1.994	3.97	6.749E-6	60.21E-6	40.63E-6
POSITIVE LATCH	773.1	5.968	4.613	677.7E-3	1.874	0.00127
NEGATIVE LATCH	750.0	3.701	2.775	682.7E-3	2.012	1.378

D-FLIP-FLOP	1.476	3.978	5.871E-3	756.1E-3	501.1E-3	3.788E-3
SHIFT REGISTER(SISO)	400.56	510.76	20.484	332.6	498.66E-3	16.577E-6

By seeing above performance metrics the comparison between MOSFET

circuits and CNTFET circuits can be summarized as

In terms of power consumption, CNTFET circuits generally exhibit lower power consumption compared to their MOSFET counterparts across different circuit configurations. This difference is particularly in standard ternary inverters, where CNTFETs consume notably less power compared to MOSFETs. The reduced power consumption of CNTFETs can be attributed to their higher carrier mobility and improved electrostatic control, allowing for more efficient operation.

Regarding delay, MOSFET circuits tend to have lower delay times than CNTFET circuits for most circuit configurations. This suggests that MOSFETs are capable of faster switching speeds, which can be advantageous in applications requiring rapid signal processing. However, it's important to note that the delay times for CNTFET circuits vary depending on the specific circuit configuration, with some configurations exhibiting comparable delay times to MOSFETs.

When considering the Power-Delay Product (PDP), which serves as a combined metric of power consumption and delay, the comparison between MOSFET and CNTFET circuits becomes more complex. While MOSFET circuits may have lower delay times, the lower power consumption of CNTFET circuits results in competitive PDP values in certain cases.

This highlights the trade-off between power consumption and delay in circuit design, where CNTFETs offer an attractive option for minimizing overall energy consumption without compromising performance significantly.

CHAPTER VII

CONCLUSION AND FUTURE SCOPE

7.1 Conclusion:

Throughout this project, Simulation of CNTFET circuits based on the structure and Average power, Time delay, Power delay product has done and these performance metrics are compared with MOSFET circuits

The design and simulation Studies of these CNTFET circuits based on multi valued logic designs have been implemented using Cadence tool software. The simulation results shows the Average power, Time Delay and Power delay products.

By implementing CNTFET circuits using multi valued logic design the circuits interconnect complexity have been reduced.

Comparison of performance metrics like Average power, Time delay and Power delay product between CNTFET and MOSFET circuits using Cadence tool, it is observed that CNTFET circuits is more efficient as reduced Power consumption and delay.

7.2 Future Scope

In terms of future scope, this project sets the foundation for further exploration and advancements in the field of CNT technology for digital circuit design. Future research could focus on optimizing the design parameters of transmission gates and dynamic shift registers to enhance performance even further. Additionally, investigating the scalability of CNT-based circuits for larger systems and exploring novel applications in emerging technologies like Internet of Things (IoT) and artificial intelligence would be valuable avenues for future development. Overall, the project report not only provides valuable insights into the potential of CNT technology in circuit design but also paves the way for exciting opportunities for innovation and advancement in the field of electronics and communication engineering.

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