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Introduction

The following report is for the Amplifier Design Project. We will design, simulate, analyze, implement, and test a single-supply, multistage, inverting, transistor amplifier which fulfills the specifications listed below.

Specifications

The given specifications are as follows:

- Power supply: $+\mathbf{10}\boldsymbol{V}$ relative to the ground;
- Quiescent current drawn from the power supply: ***no larger than*** $\mathbf{10}\ \boldsymbol{mA}$;
- No-load voltage gain (at $1\ kHz$): $|\boldsymbol{A_{vo}}| = \mathbf{50}\ (\pm\ \mathbf{10\%})$;
- Maximum no-load output voltage swing (at $1\ kHz$): ***no smaller than 8 V peak to peak;***
- Loaded voltage gain (at $1\ kHz$ and with $R_L = 1\ k\Omega$): ***no smaller than*** $\mathbf{90\%}$ ***of the no-load voltage gain;***
- Maximum loaded output voltage swing (at $1\ kHz$ and $R_L = 1\ k\Omega$): ***no smaller than 4 V peak to peak;***
- Input resistance (at $1\ kHz$): ***no smaller than*** $\mathbf{20}\ \boldsymbol{k\Omega}$;
- Amplifier type: ***inverting or non-inverting;***
- Frequency response: ***20 Hz to 50 kHz*** $(-3dB$ ***response);***
- Type of transistors: ***BJT;***
- Number of transistors (stages): ***no more than 3***;
- Resistances permitted: ***values smaller than*** $\mathbf{220}\ \boldsymbol{k\Omega}$ ***from the E24 series***;
- Capacitors permitted: $\mathbf{0.1}\ \boldsymbol{\mu F}$, $\mathbf{1.0}\ \boldsymbol{\mu F}$, $\mathbf{2.2}\ \boldsymbol{\mu F}$, $\mathbf{4.7}\ \boldsymbol{\mu F}$, $\mathbf{10}\ \boldsymbol{\mu F}$, $\mathbf{47}\ \boldsymbol{\mu F}$, $\mathbf{100}\ \boldsymbol{\mu F}$, $\mathbf{220}\ \boldsymbol{\mu F}$;
- Other components (BJTs, diodes, Zener diodes, etc.): ***only from your ELE404 lab kit.***

Circuit Under Test

Figure 1 shows the designed circuit of the amplifier which was simulated in MultiSim. It consists of three states: CC input with high resistance, CE with high voltage gain, CC output with low output resistance. Coupling and bypass capacitors are used in order to block DC voltage and allow the AC signal to pass through.

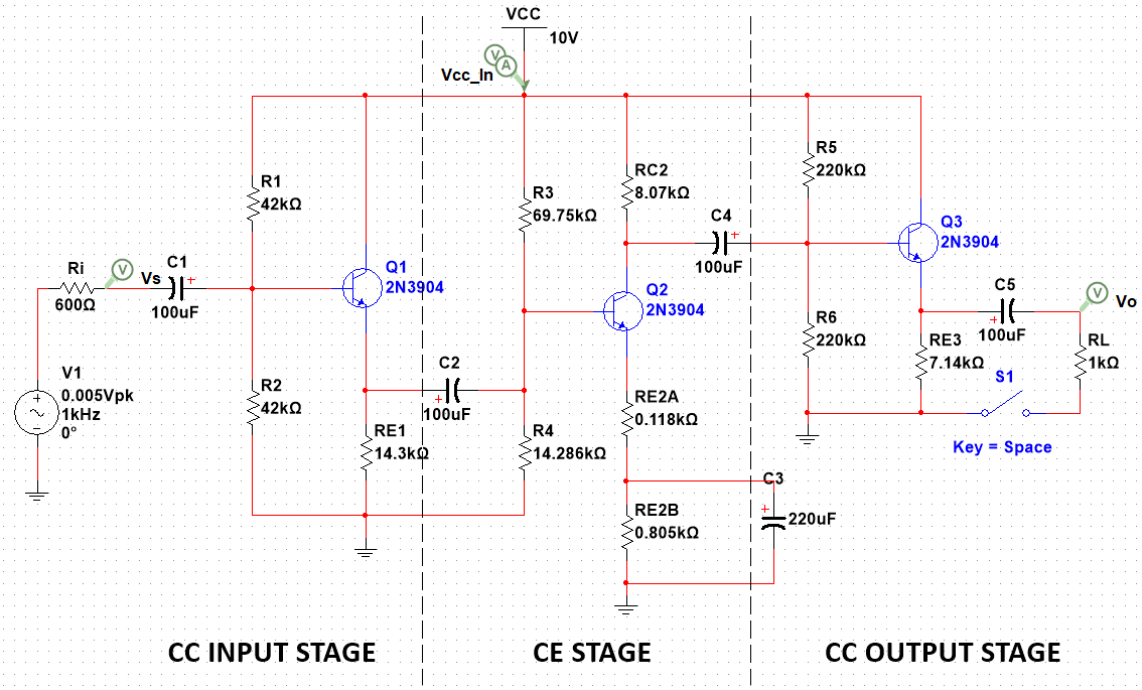


Figure 1

Experimental Results

DC Analysis

Figure 2 and **Figure 3** will be used to calculate the gain of the amplifier. Obtained values upon the simulations of these circuits are listed in **Table 1** below.

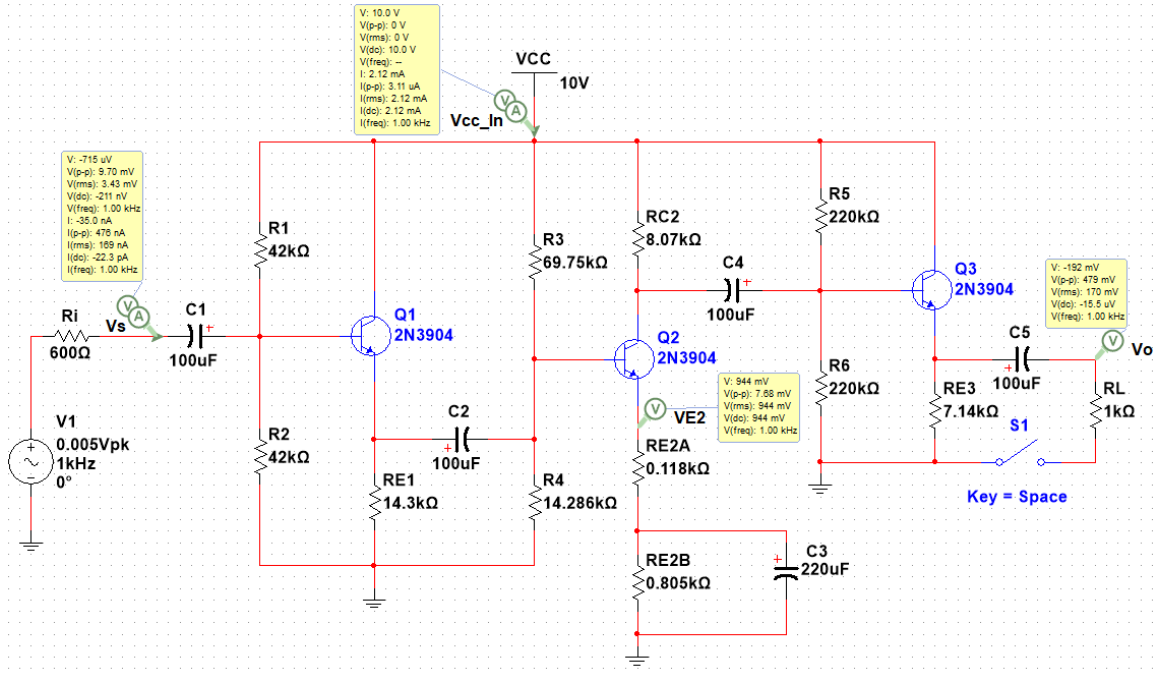


Figure 2 – No Load

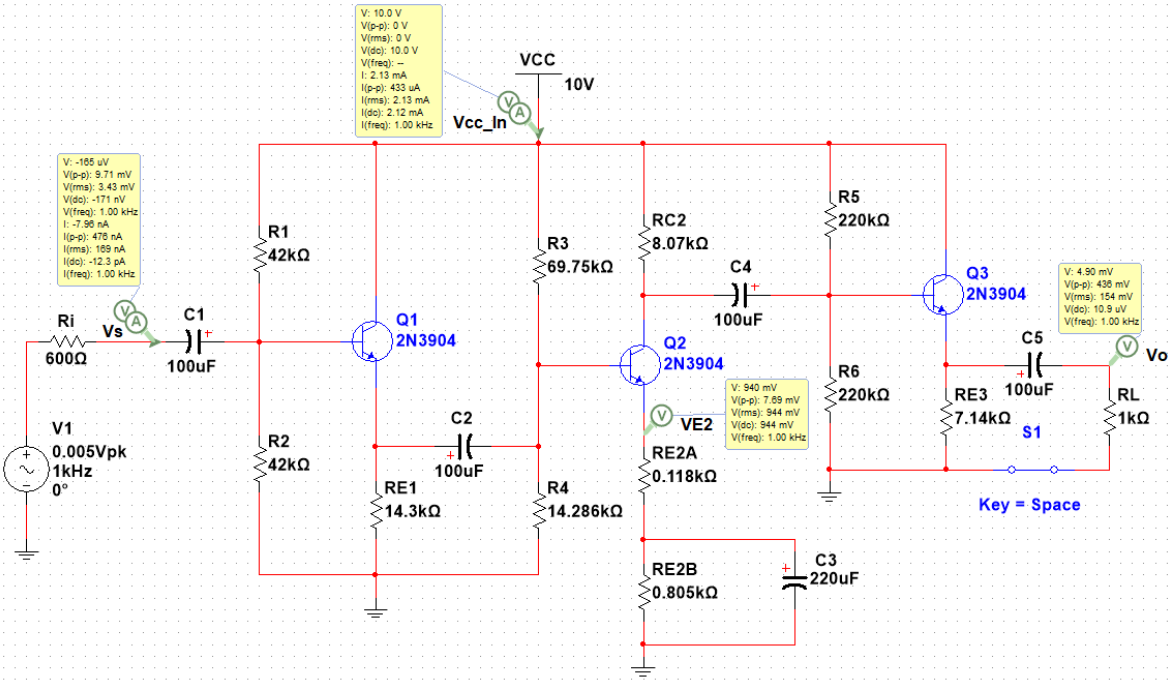


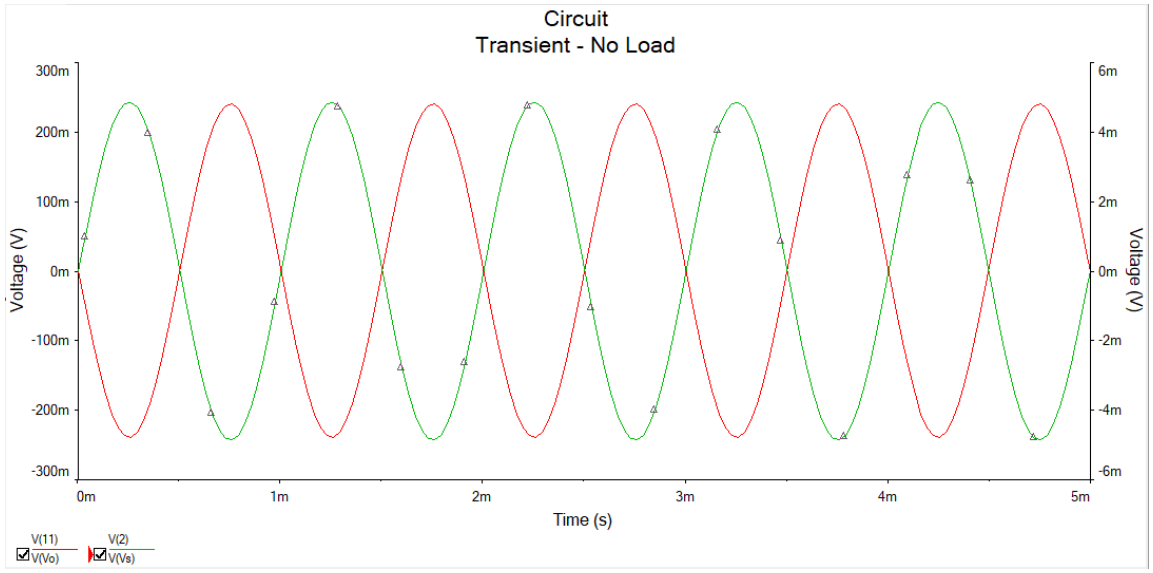
Figure 3 - Loaded

Circuit Type	V_{CC} $[V]$	V_S $[mVp-p]$	V_O $[mVp-p]$	$V_{E2}[V]$
No Load	10	9.70	479	0.944
Loaded	10	9.71	436	0.940

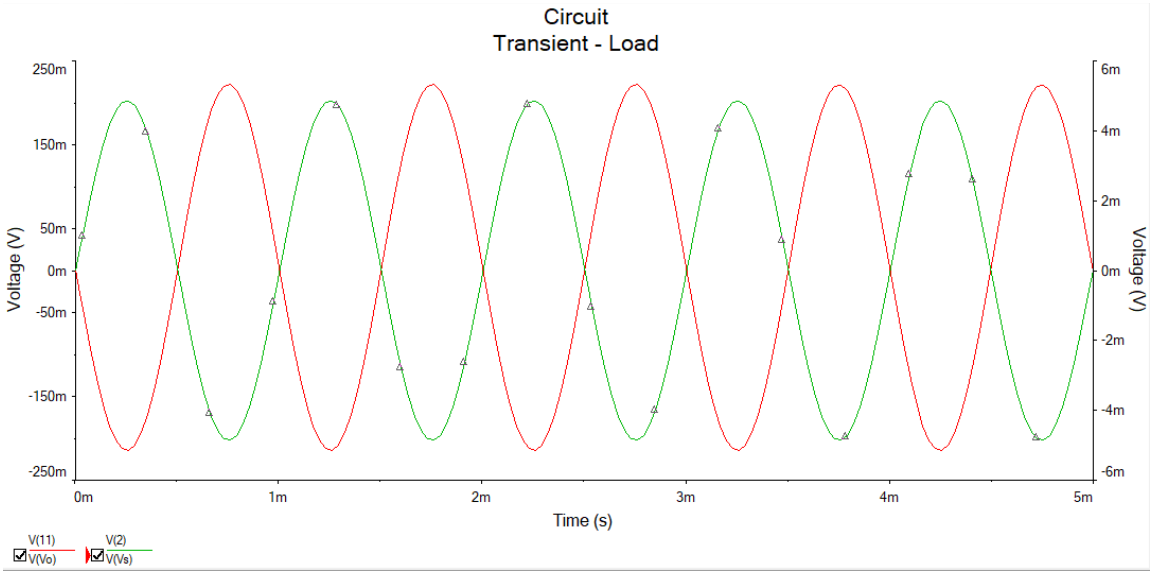
Table 1

Transient Response

Graph 1 and **Graph 2** show the waveforms for V_O vs V_S for the amplifier. Refer to the left axis for V_O and the right axis for V_S.



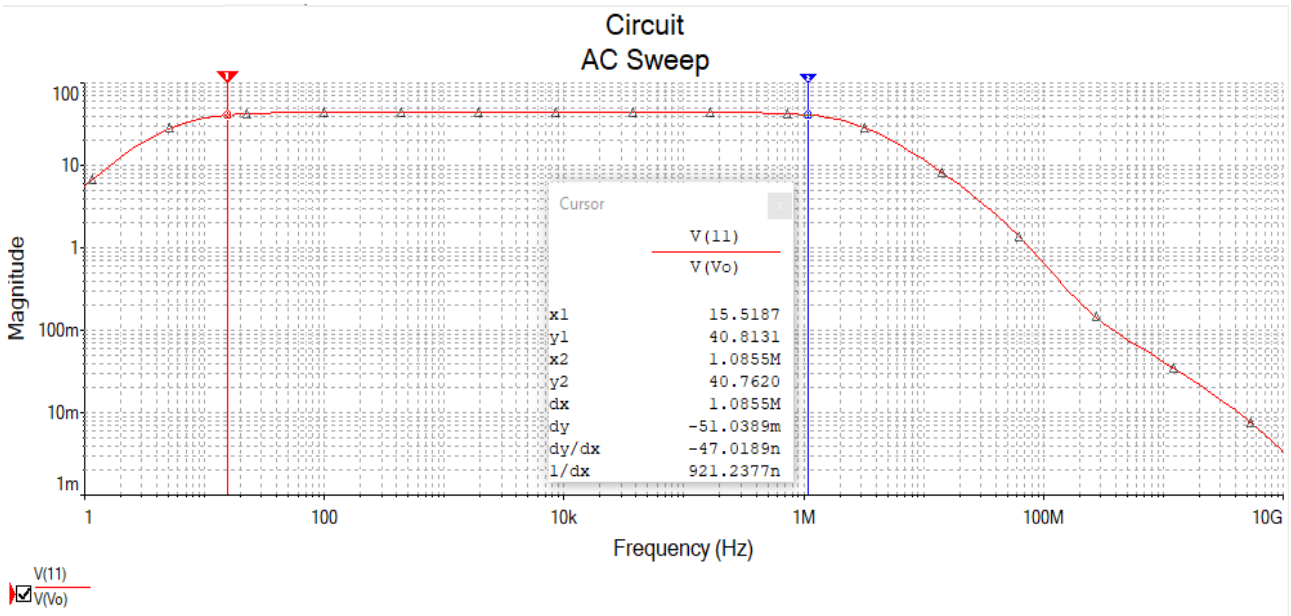
Graph 1 – No Load



Graph 2 – No Load

Frequency Response

The frequency response of the amplifier is shown in **Graph 3**. When the graph increasing and decreasing, the amplifier is not stable however when the line is flat it is stable. The max value for which it is stable was measured to be $43.801\ dB$. Measuring probes are shown $-3\ dB$ below this stable value and the amplifier is at its maximum stable frequency in between these two probes. The two values are $15.52\ Hz$ and $1.09\ MHz$ and the required frequencies of $20\ Hz$ to $50\ kHz$ is fall well between this range.



Graph 3

Analysis

Voltage Gain

The calculations were completed using the values obtained in **Table 1.**

No Load:

$$|A_{VO}| = \frac{V_O}{V_S} = \frac{479}{9.70} = 49.38$$

Within the $\pm 10\%$ of 50 range.
90% of this value is: 44.44

Loaded:

$$|A_V| = \frac{V_O}{V_S} = \frac{436}{9.71} = 44.90$$

44.90 > 44.44

The no-load voltage gain falls within the range given and the loaded voltage gain is larger than 90% of the no-load voltage gain, hence the specifications are met.

Evaluation

Choice of Configuration

The purpose of the CC-CE-CC configuration was to successfully accomplish the specifications given. The CC input stage amplifier allows the circuit to have a high input resistance, the CE stage amplifier gives the circuit a high voltage gain and the CC output stage amplifier provides the circuit with a low output resistance while preventing loss in gain values using a load resistor.

Transient Response

The waveforms in **Graph 1** and **Graph 2** show the V_O vs V_S response of the amplifier. We can see that there is no clipping or any type of distortions in either graph which means that the output voltage is properly centered for each amplifier.

Frequency Response

The C_3 capacitor played the most crucial role in the frequency response portion as it allowed us to achieve a low minimum operating frequency. The other capacitors were similarly kept at a high value to obtain the best results. Overall, the frequency requirements were met based on the specifications.

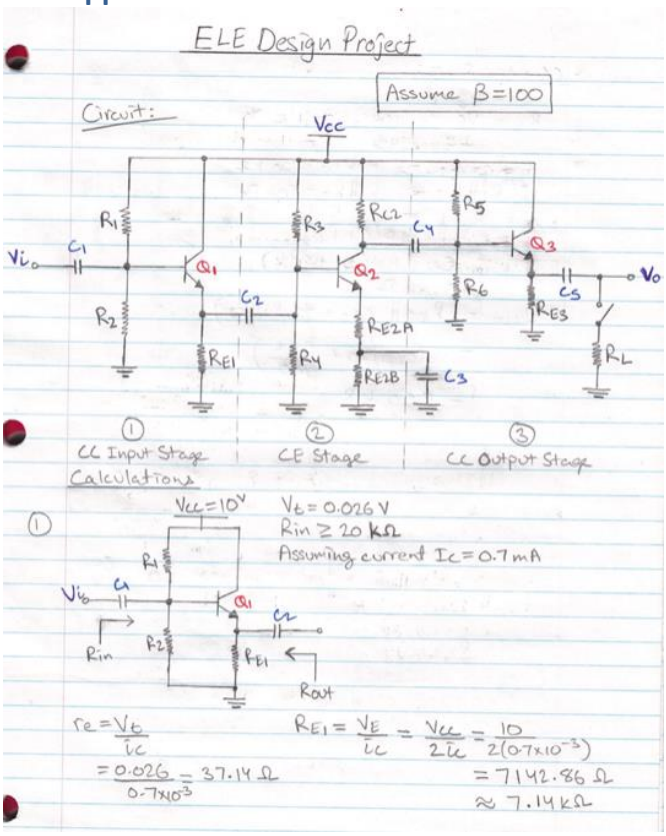
Voltage Swing

The voltage swing was calculated by measuring the value of V_{E2} which was approximately 1V for both no-load and loaded circuits. To this value, the value of $V_{CE,sat}$ was added and this sum was subtracted from V_{CC}. No-load and loaded requirements were both met.

Discrepancies

Most of the discrepancies can be found when calculations are rounded off. The calculations done by hand were theoretical and were rounded to the nearest value. These did not affect the experimental values by much, there were only some slight changes in the final answers. For instance, the required voltage gain was to be 50 and through our experiment, we got 49.38. Even though it was in the $\pm$10% range, it still is a discrepancy. In addition, some resistances/capacitances of the BJTs were ignored for calculation purposes which could have also caused discrepancies. During the simulation of the circuit, the values of various components were played around with in order to obtain the best results. Finally, all the construction of the amplifier was successful, and all the specifications given were fulfilled.

Appendix – Calculations



$V_t = 0.026\ V$

$R_{in} \geq 20\ k\Omega$

Assuming current $I_C = 0.7\ mA$

$$r_e = \frac{V_t}{I_C} = \frac{0.026}{0.7\times10^{-3}} = 37.14\ \Omega$$

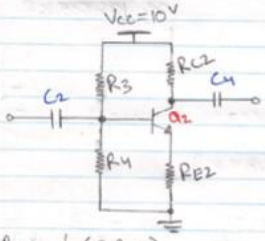
$$R_{E1} = \frac{V_E}{I_C} = \frac{V_{cc}}{2I_C} = \frac{10}{2(0.7\times10^{-3})} = 7142.86\ \Omega \approx 7.14\ k\Omega$$

Assuming $R_1 = R_2 = 42\ k\Omega$

$$R_{in} = R_1 \| R_2 \| \beta(r_e + R_{E1}) = 42 \| 42 \| 100(37.14 + 7142.86) = 20.4032\ k\Omega$$

$$R_{out} = R_{E1} \| \left(r_e + \frac{1}{\beta}(R_1 \| R_2)\right) = 37.14 \| \left(37.14 + \frac{1}{100}(42 \| 42)\right) = 238.878\ \Omega$$

②



Assume $V_{E2} = 1V$ to stabilize β w/o decreasing output.

$$R_{E2} = \frac{V_{E2}}{I_C} = \frac{1}{0.7\times10^{-3}} = 923.517\ \Omega \approx 0.924\ k\Omega$$

Assume $V_{B2} = 1.7V$ & use voltage divider to obtain:

$$\frac{R_3}{R_4} = \frac{V_{cc} - V_{B2}}{V_{cc}} = \frac{10 - 1.7}{1.7} = 4.88 \quad (A)$$

$$R_4 = \frac{1}{10}(\beta R_{E2}) = \frac{100(1428.57)}{10} = 14285.71\ \Omega \approx 14.286\ k\Omega \quad (B)$$

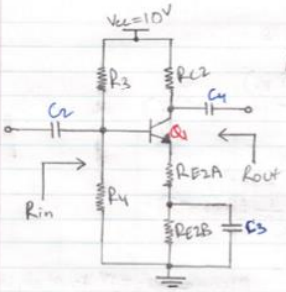
From (A) & (B):

$R_3 = 4.88(14285.71) = 69747.9\ \Omega \approx 69.75\ k\Omega$

For max voltage swing:

$$V_{C2} = \frac{V_{cc} - (V_{E2} + V_{CE,sat})}{2} = \frac{10 - (1 + 0.3)}{2} = 4.35\ V \Rightarrow \text{Voltage swing is } 8.7V.$$

$$R_{C2} = \frac{V_{cc} - V_{C2}}{I_C} = \frac{10 - 4.35}{0.7\times10^{-3}} = 8071.43\ \Omega \approx 8.07\ k\Omega$$



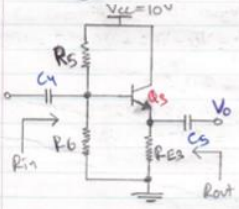
$$R_{E2A} = \frac{R_{C2}}{A_{V0}} - r_e = \frac{8071.43}{50} - 37.14 = 118.374 \approx 0.118\ k\Omega$$

$$R_{E2B} = R_{E2} - R_{E2A} = 923.514 - 118.374 = 1805.143 \approx 0.805\ k\Omega$$

$$R_{in} = R_3 \| R_4 \| \beta(r_e + R_{E2A}) = 69747.9 \| 14285.71 \| 100(37.14 + 124.2857) = 6836.0058\ \Omega \approx 6.84\ k\Omega$$

$$R_{out} = R_{C2} \approx 8.07\ k\Omega$$

③



$$R_{E3} = \frac{V_E}{I_C} = \frac{V_{cc}}{2I_C} = \frac{10}{2(0.7\times10^{-3})} = 7142.857\ \Omega \approx 7.14\ k\Omega$$

Assume $R_5 = R_6 = 220\ k\Omega$

$$R_{in} = R_5 \| R_6 \| \beta(r_e + R_{E3}) = 220 \| 220 \| 100(37.14 + 7142.857) = 95386.47\ \Omega \approx 95.4\ k\Omega$$

$$R_{out} = R_{E3} \| r_e\left(\frac{1}{\beta}R_5 + R_6\right) = 7142.857 \| 37.14\left(\frac{1}{100}(440)\right) = 980.9721\ \Omega \approx 0.981\ k\Omega$$

For the CE stage, an emitter bypass capacitor was used in the circuit reduce the resistances for AC values while keeping the DC resistances the same. The results are shown in the tables below. **Table 1** shows the values obtained from the CC input stage, **Table 2** shows the values obtained from the CE amplifier stage, and **Table 3** shows the values obtained from the CC output stage.

$V_t[V]$	$I_C[mA]$	$R_1[\text{k}\Omega]$	$R_2[\text{k}\Omega]$	$R_{E1}[\text{k}\Omega]$	$r_e[\Omega]$	$R_{in}[\text{k}\Omega]$	$R_{out}[\Omega]$
0.026	0.7	42	42	7.14	37.14	20.4032	238.878

Table 2

$V_t[V]$	$I_C[mA]$	$R_3[\text{k}\Omega]$	$R_4[\text{k}\Omega]$	$R_{E2A}[\text{k}\Omega]$	$R_{E2B}[\text{k}\Omega]$	$r_e[\Omega]$	$R_{in}[\text{k}\Omega]$	$R_{out}[\text{k}\Omega]$
0.026	0.7	69.75	14.286	0.118	0.805	37.14	6.84	8.07

Table 3

$V_t[V]$	$I_C[mA]$	$R_5[\text{k}\Omega]$	$R_6[\text{k}\Omega]$	$R_{E3}[\text{k}\Omega]$	$r_e[\Omega]$	$R_{in}[\text{k}\Omega]$	$R_{out}[\text{k}\Omega]$
0.026	0.7	220	220	7.14	37.14	95.4	0.981

Table 4

Loading Factors are calculated as follows:

LF_1

LF_1 is the loading factor between the CC input stage and the CE amplifier stage

$$LF_1 = \frac{R_{in}[Q_2]}{R_{out}[Q_1] + R_{in}[Q_2]} = 0.966$$

LF_2

LF_2 is the loading factor between the CE amplifier stage and the CC output stage

$$LF_2 = \frac{R_{in}[Q_3]}{R_{out}[Q_2] + R_{in}[Q_3]} = 0.922$$