

ECS 409/609 : Verilog/VHDL

Behavioral Based Assignment

Instructor: Dr. Sukarn Agarwal,
Assistant Professor,
Electrical Engineering and Computer Science Department,
IISER Bhopal

September 1, 2025

Behavioral Module

- The behavioral module contains the functional description of the circuit.
- The functional description is represented with logical and mathematical operators.
- In this module, the level of abstraction is higher than the Gate-level, aka Structural Verilog-based module.

Sample Structure of Behavioral Verilog Coding Style

The sample coding style of behavioral verilog module is as follows:

```
module example (a, b, c, y);
    input a;
    input b;
    input c;
    output y;

    // The circuit description are given as follows

    assign y = ~a & ~b & ~c |
               a & ~b & ~c |
               a & ~b & c
endmodule
```

The hardware implementation of the above behavioral code is given in Figure 1.
Another sample code with bitwise operation is as follows:

```
module gates(input [3:0] a, b,
             output [3:0] y1, y2, y3, y4, y5);
    /* Five different two-input logic
     gates acting on 4 bit buses */

    assign y1 = a & b; // AND
```

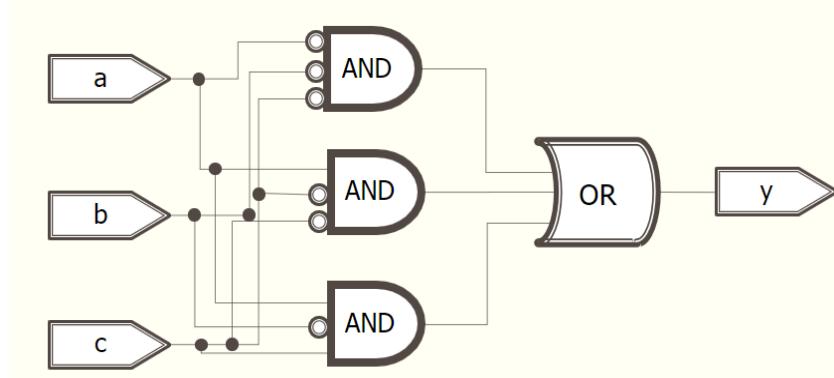


Figure 1: Behavioral HDL: Schematic View

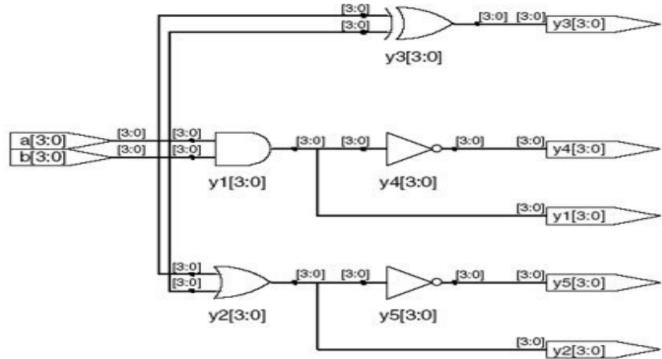


Figure 2: Bitwise based Behavioral HDL: Schematic View

```

assign y2 = a | b; // OR
assign y3 = a ^ b; // XOR
assign y4 = ~(a & b); // NAND
assign y5 = ~(a | b); // NOR

endmodule

```

The synthesized circuit of the above code is given in Figure 2.

With this module in mind, implement the following Verilog programs using behavioral Verilog.

Problem Statements

Level-Easy

Problem 1: Write behavioral verilog code to multiply a 4-bit input by 2.

Problem 2: Implement a behavioral verilog code for a 4-to-2 encoder and 2-to-4 decoder.

Level-Medium

Problem 3: Design an 8-to-1 multiplexer using a case statement in behavioral

verilog.

Problem 4: Design an 8-to-3 priority encoder using the if else statement in behavioral Verilog.

Level-Difficult

Problem 5: Write behavioral Verilog code for a 4-bit Carry Look-Ahead Adder.

Problem 6: Design behavioral Verilog code for a 4-bit Wallace Tree Multiplier.

Submission Format and Deadline: Submit all your source code, test bench code, and output/waveform (if applicable) in a pdf format file by the end of the day of 10-Sep-2025 (IST) at Google Classroom. Please make sure your name should appear on the gtkoutput waveform/terminal screen. Further, any copy case between the assignment(s) results in a zero mark. Note that TA may run the Plagiarism checker to check if the code is not copied from any other online source(s), if the tool found more than a 30% match percentage, it results in a zero mark.