STEPHEN F. AUSTIN STATE UNIVERSITY

CSC 214

LAB 4

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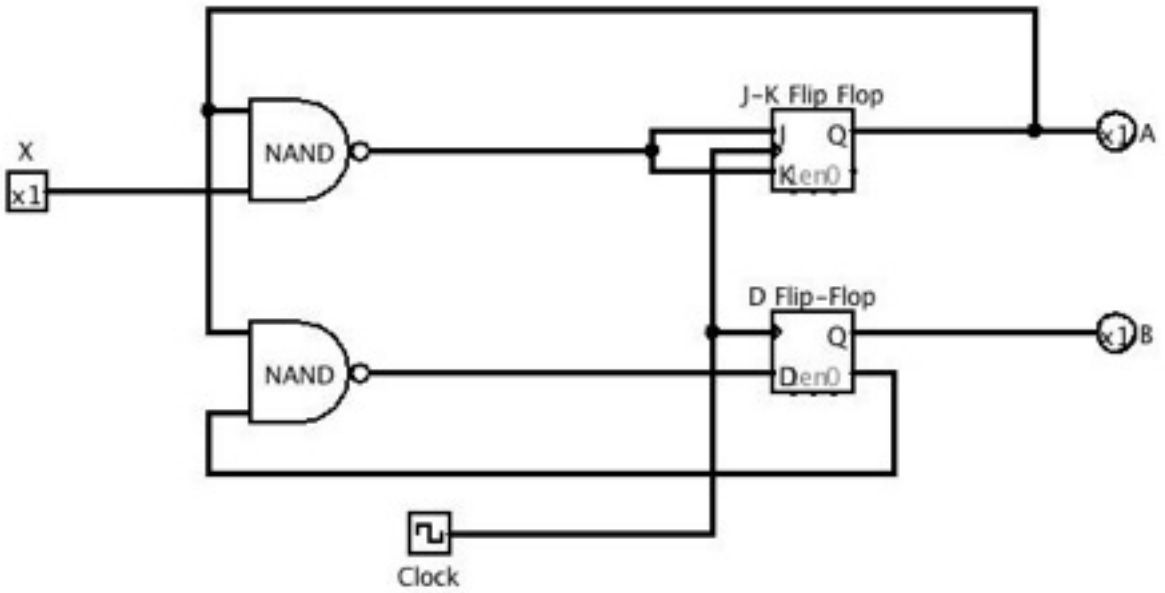

The initial process of designing the circuit from exercise 54 was relatively straight forward. I experimented with Logisim while reviewing chapter 3 to gain a better understanding of J-K Flip-Flops, so the initial process of selecting components (combinatorial and sequential) and wiring the components together was familiar. I encountered a few issues while implementing the circuit.

My first issue involved adding input to Logisim. I had utilized the clock in my previous experiments with Logisim, but hadn't introduced an additional input. Initially I tried adding the 0 or 1 input for the X input to the NAND gate with a button, this didn't seem to be the correct approach, so I did so more research into the correct way to implement the behavior I was looking for using Logisim's libraries.

After reading more Logisim documentation and a beginner tutorial, I found that input in Logisim is handled through "pins". Values for these pins can be switched between 0 and 1 using the "poke" tool while testing the circuit. The pin I placed to act as my X input was initially a 3 state pin. I altered my input pin to be 2 state (0 or 1) instead of 3 state (0, x, or 1), to remove the "unknown" state.

After a bit of trial and error, I found out there are two different pin tools. A square pin tool that allows for the input state to be changed between 0 and 1, and a circle pin tool that actually displays the value (0 or 1) being transmitted to the pin by the circuit. I decided to use the square pin tool for my input value, X, and the circle pin tools to display the state of the circuit's outputs A and B. I also altered the output pin to be 2 state (0 or 1) instead of 3 state (0, x, or 1).

Hand Verification for Circuit

Present State		Input	Next State	
A	B	X	A	B
0	0	0	1	1
0	0	1	1	1
0	1	0	1	1
0	1	1	1	1
1	0	0	0	0
1	0	1	1	0
1	1	0	0	1
1	1	1	1	1

The next issue I encountered was with my D Flip-Flop, at first glance it didn't appear to be altering the value of its output (Q) or the complement of its output (Q') when the state of the circuit changed. I decided to try rewiring that portion of the circuit to see if I had made an error when placing the wires originally. I rewired the portions of the circuit connected to the D Flip-Flop. Rewiring seemed to result in the same behavior, so I moved on to verifying that this was indeed the correct output for the circuit.

While trying to work out the issues with the D Flip-Flop and verifying the output, I discovered that Logisim can output the truth tables for circuit simulation to a text file that can be used to cross reference the circuit behavior with the hand verified truth table for the circuit. I completed the hand verification for the circuit in exercise 54 to use as a reference for the circuit simulation in Logisim. The hand verified truth table for the circuit is shown in the table at the top of the page.

To test the circuit, I changed the logging settings in Logisim to output to a text file and added my input X, and my outputs A and B, to the table to track for simulation. To test each state of the truth table for exercise 54, I followed the same process for each row:

1. Reset the simulation
2. Change values to match truth table (set X, A, and B to correct states).
3. Step through simulation (clock tick).
4. Record the next states for A and B output to the file.
5. Add text describing the process for each state change in the output file.

Applying the process just described, the values I obtained for the circuit for each row in the truth table are described and summarized below. Along with the actual process of obtaining the data of the truth table from the simulation.

Stepping through the simulation for each row of the truth table:

X	A	B	
0	0	0	STATE 1
0	1	1	NEXT STATES
0	0	0	RESET
1	0	0	SET X- STATE 2
1	1	1	NEXT STATES
0	0	0	RESET
0	0	1	SET B- STATE 3
0	1	1	NEXT STATES
0	0	0	RESET
0	0	1	SET B
1	0	1	SET X- STATE 4
1	1	1	NEXT STATES
0	0	0	RESET
0	1	0	SET A- STATE 5
0	0	0	NEXT STATES
0	0	0	RESET
1	0	0	SET X
1	1	0	SET A- STATE 6
1	1	0	NEXT STATES
0	0	0	RESET
0	1	0	SET A
0	1	1	SET B- STATE 7
0	0	1	NEXT STATES
0	0	0	RESET
1	0	0	SET X
1	1	0	SET A
1	1	1	SET B- STATE 8
1	1	1	NEXT STATES

The values obtained by stepping through the simulation in this manner yielded the following values:

Summarization of Simulation Values

Present State		Input	Next State	
A	B	X	A	B
0	0	0	1	1
0	0	1	1	1
0	1	0	1	1
0	1	1	1	1
1	0	0	0	0
1	0	1	1	0
1	1	0	0	1
1	1	1	1	1

The values obtained through the circuit simulation are identical to those obtained through hand verification of the circuit.

In conclusion, the only truly surprising results were in the initial testing with the D Flip-Flop. The majority of the time the output for B, and therefore the D Flip-Flop, were indeed 1 so the simulation was actually initially correct. After some research, working through tutorials, the output for the circuit was verified using the hand verified truth table from exercise 54. The output for the simulations corresponds with the verification, so the simulation appears to accurately represent the circuit being modeled. Issues regarding input were solved in a similar fashion. By reading about available tools in the Logisim libraries, finding the correct components to simulate the behavior desired for the circuit input and output was straight forward as well.