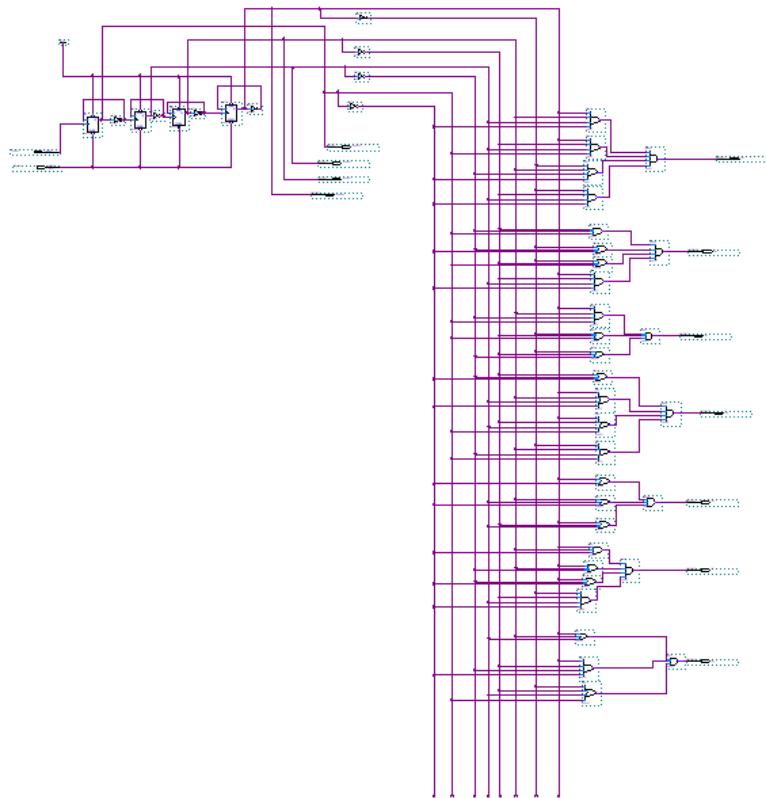


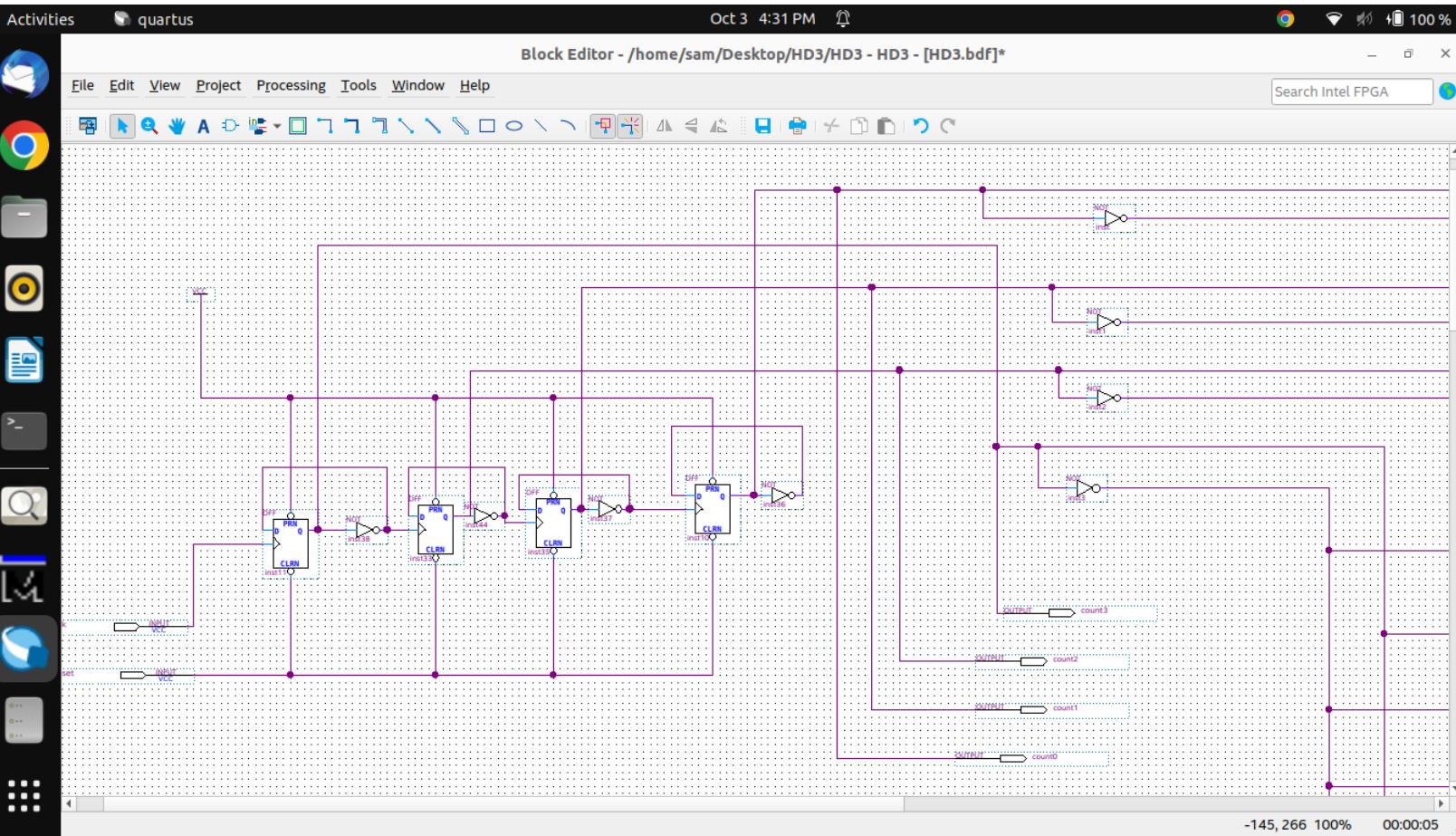
Time to complete this lab:

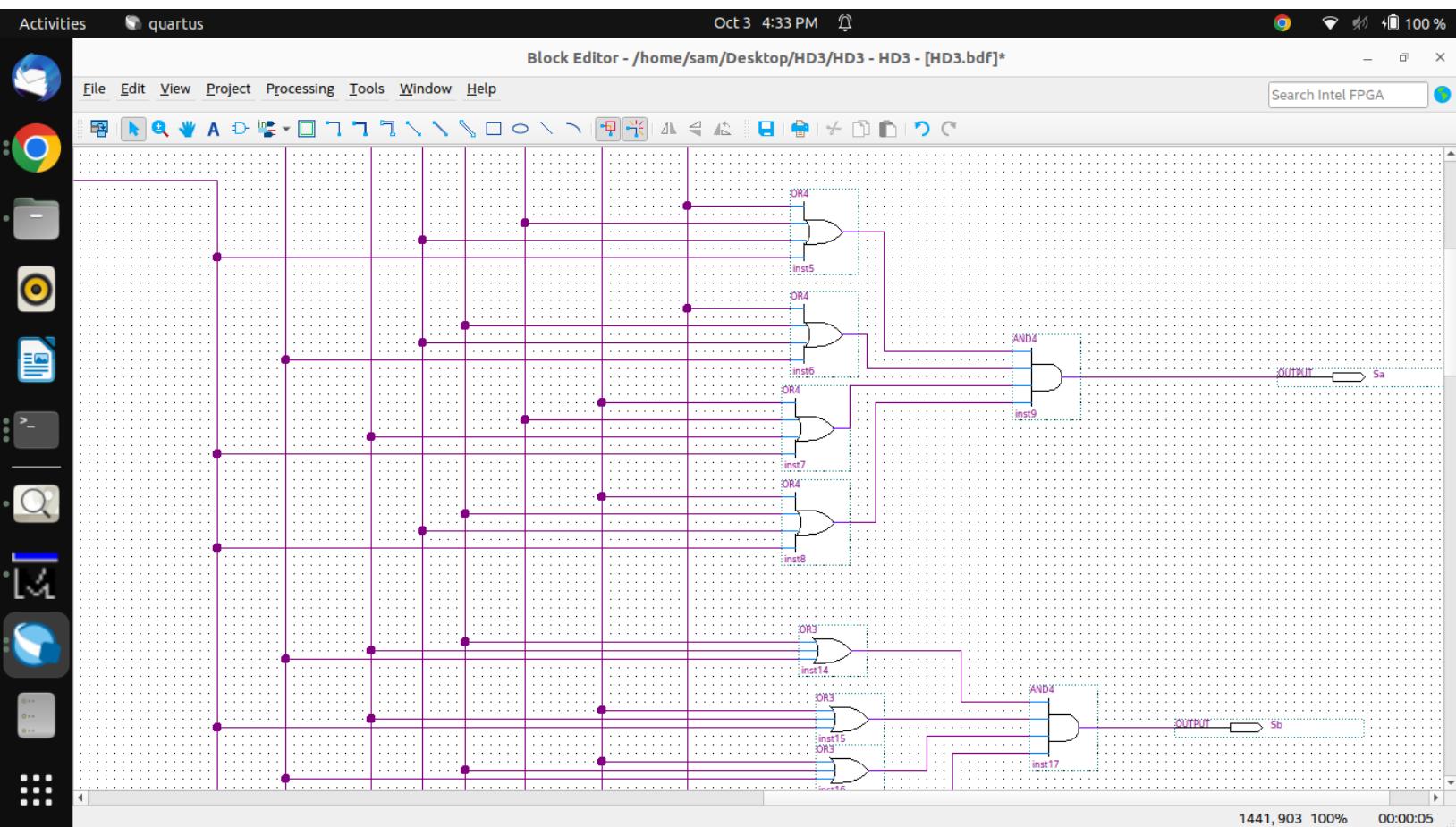
5 hours!

An image of Quartus schematic showing ripple counter logic:



Images of Quartus schematic:





Activities

quartus

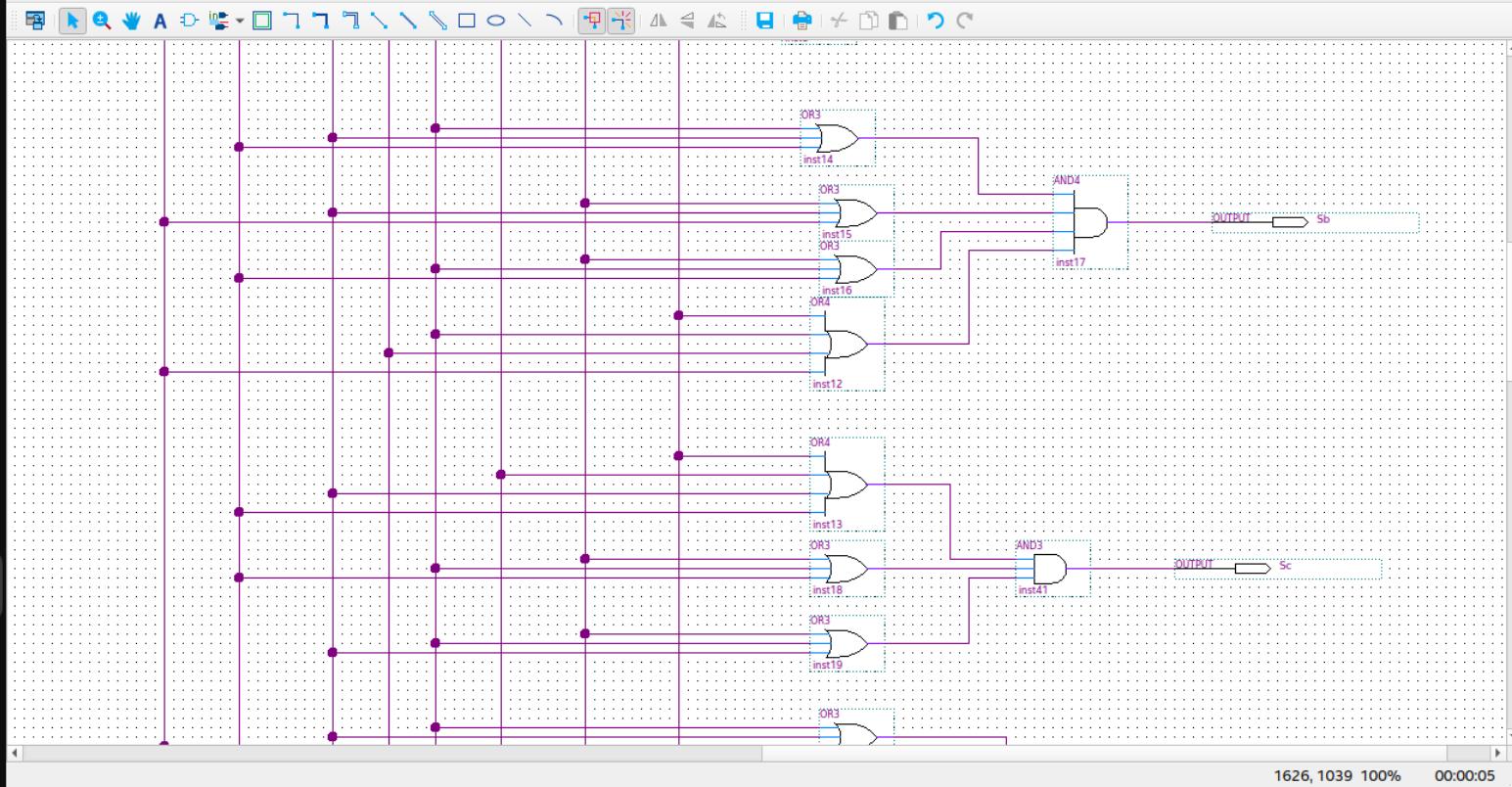
Oct 3 4:34 PM

100 %

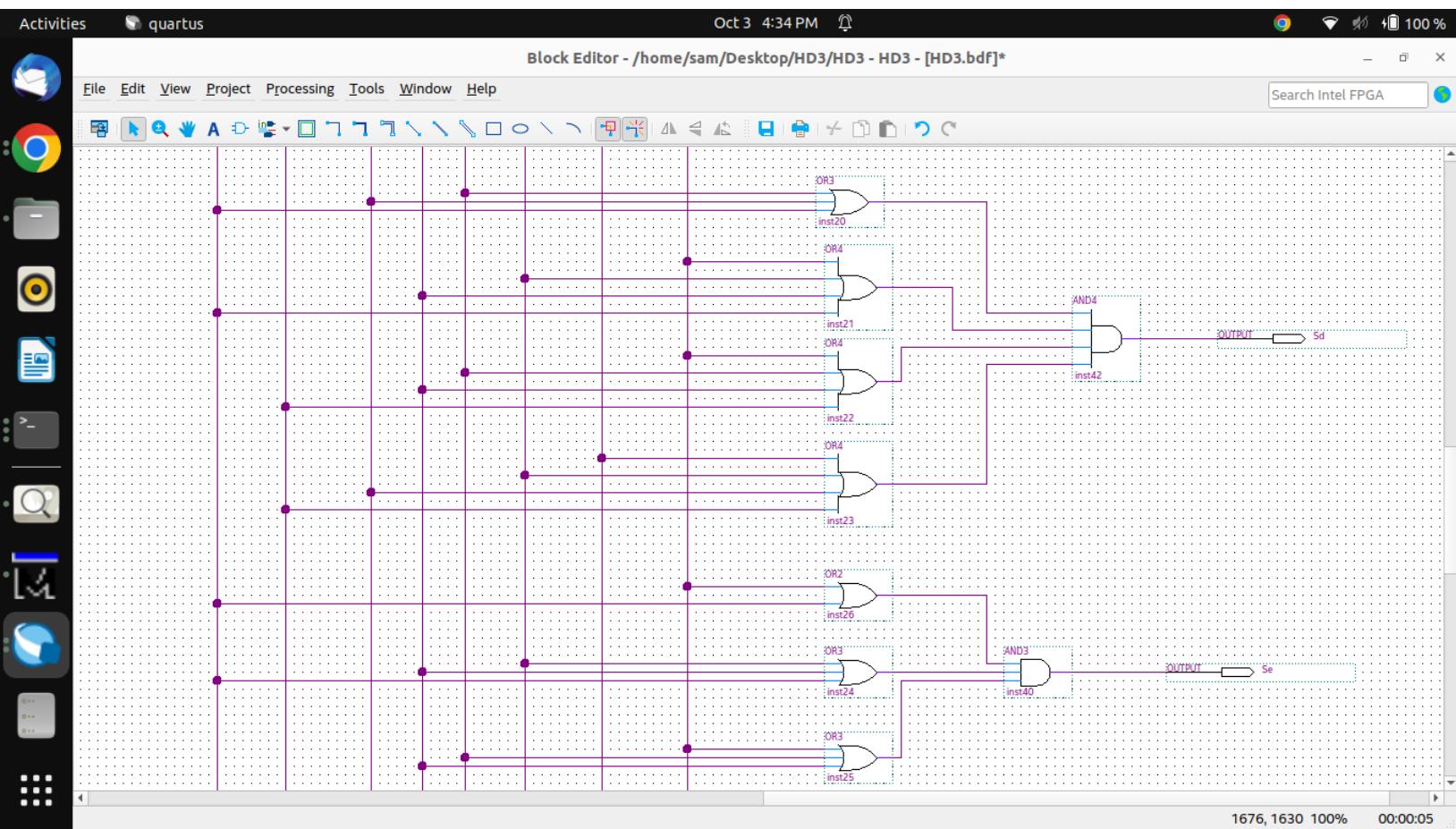
Block Editor - /home/sam/Desktop/HD3/HD3 - HD3 - [HD3.bdf]*

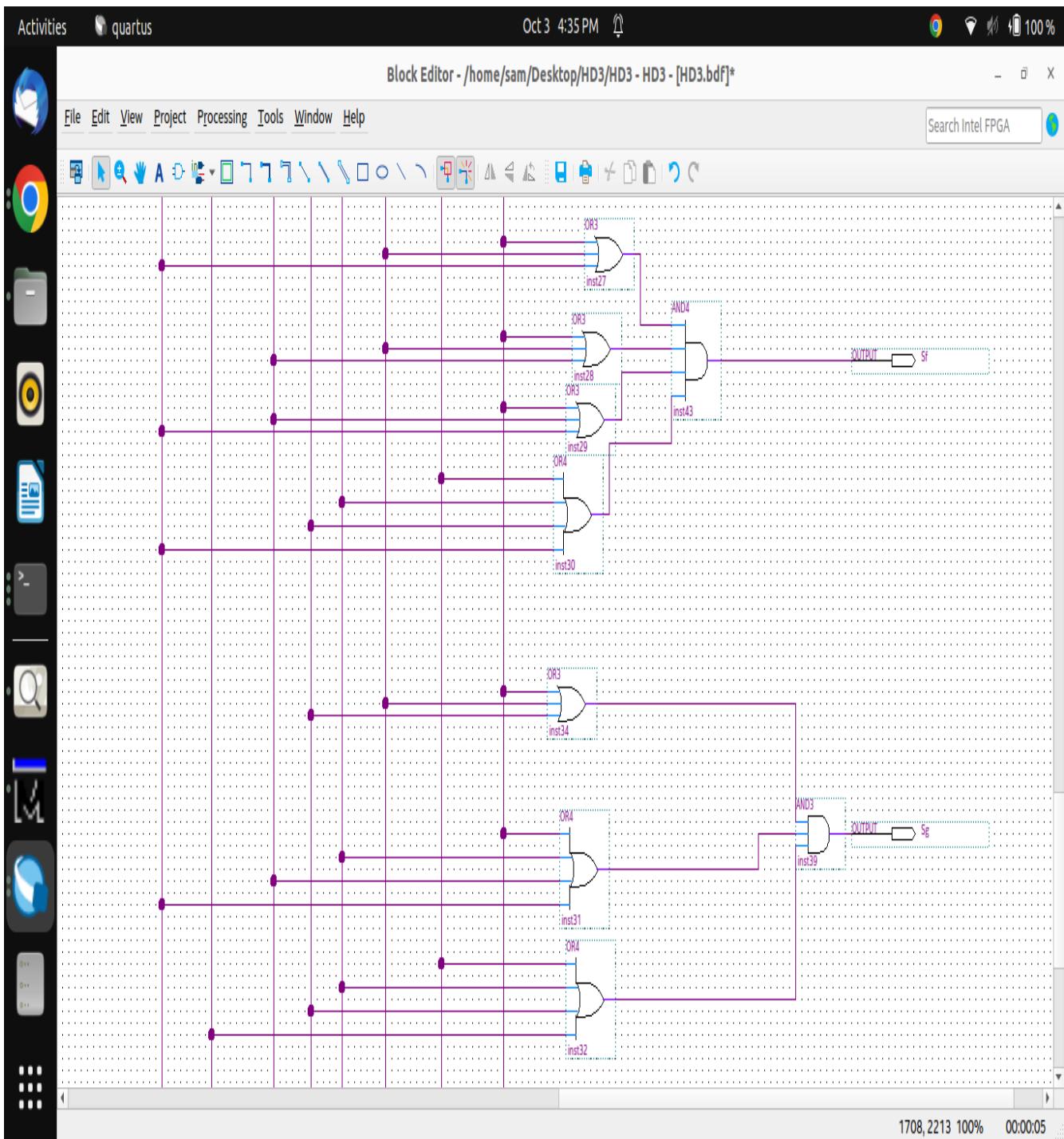
File Edit View Project Processing Tools Window Help

Search Intel FPGA

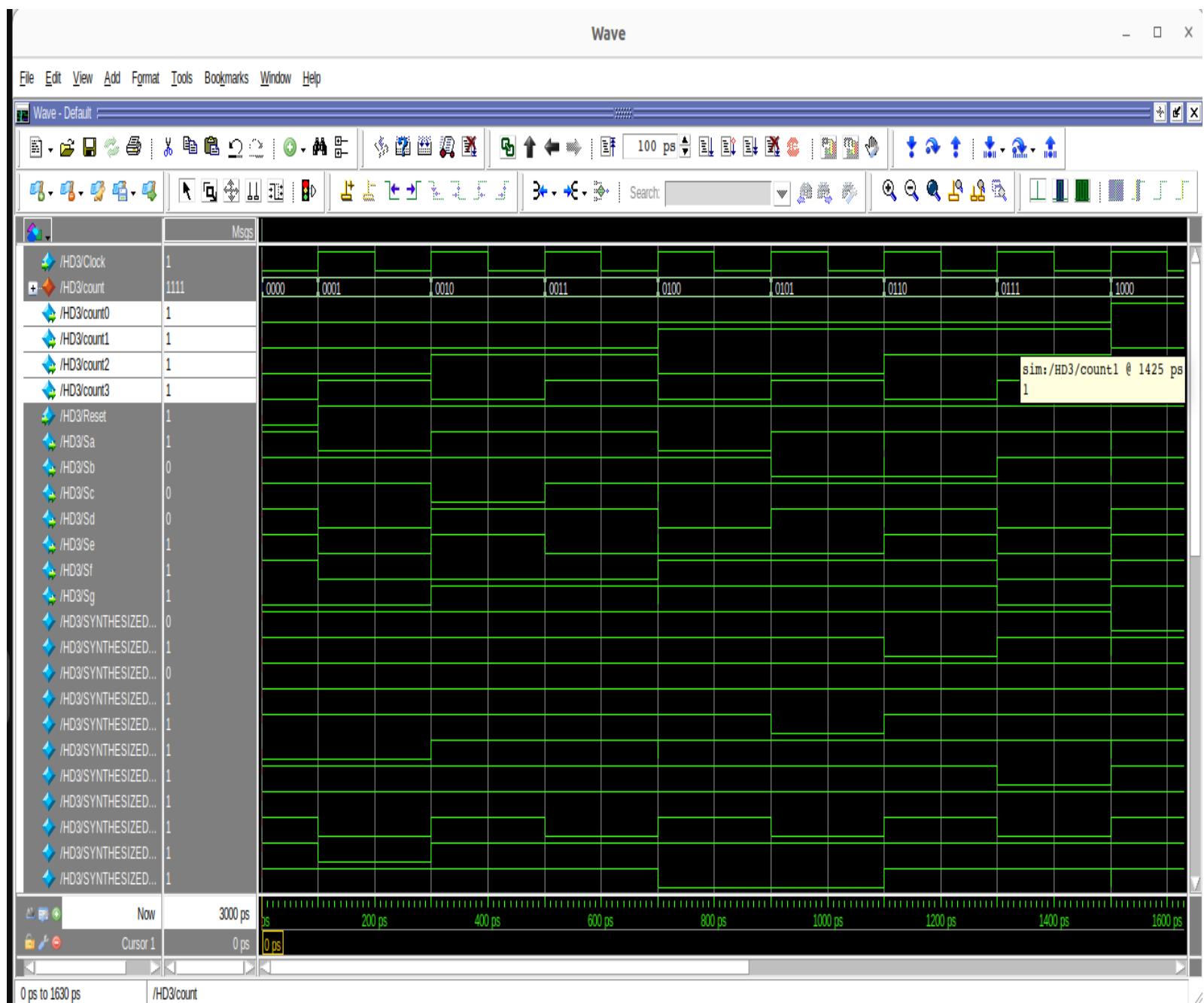


1626, 1039 100% 00:00:05

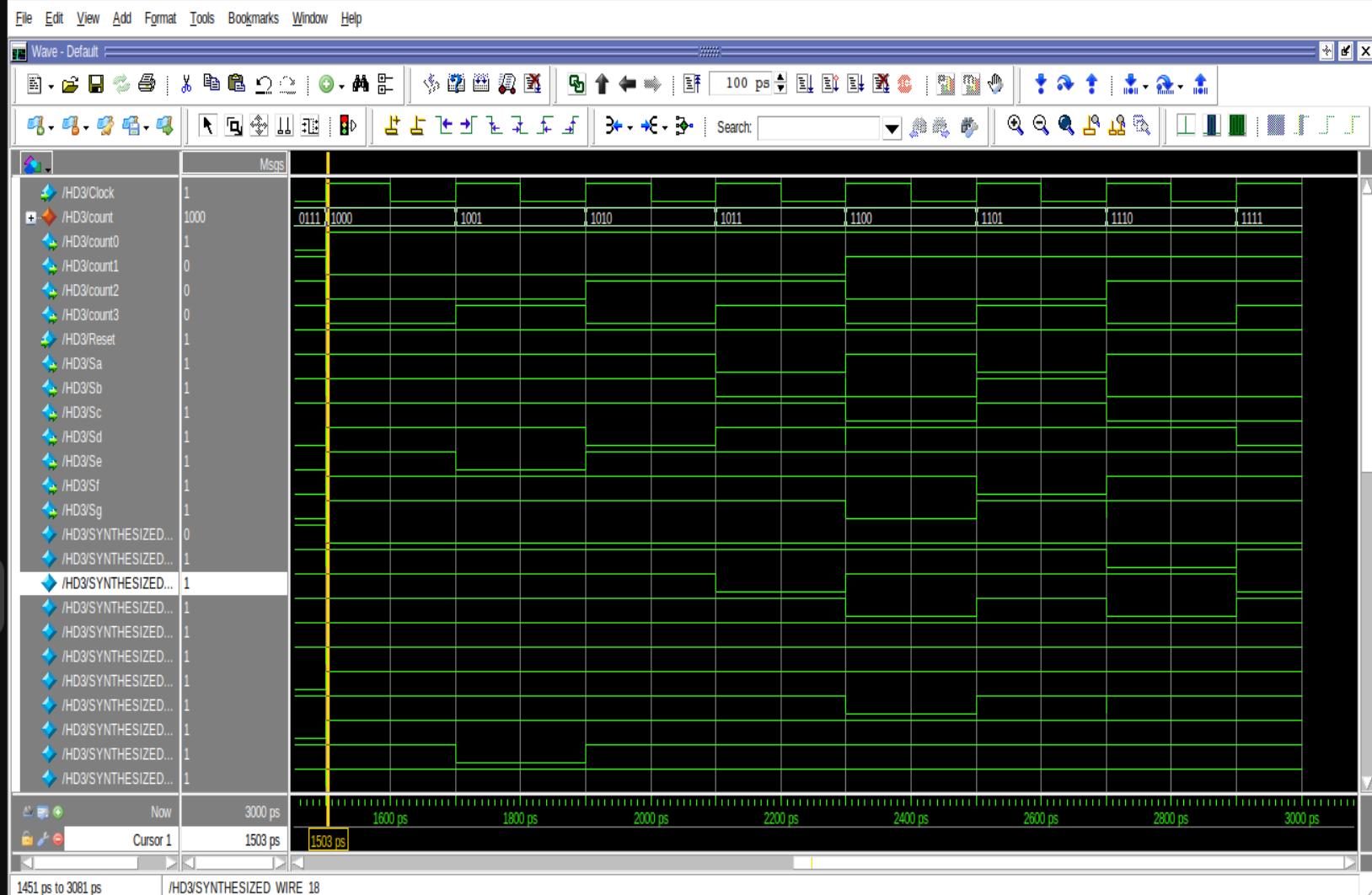




Images of simulation waveforms showing correct operation of the ripple counter:



Wave



Yes, Hardware Implementation works.
Snapshots attached below:

