

## Hours i spent on this lab:

25 hours!

## Complete Truth table for the 7 segment display :

Hexadecimal Digit	Inputs				Outputs					In Hex	
	A	B	C	D	Sg	Sf	Se	Sd	Sc	Sb	
0	0	0	0	0	0	1	1	1	1	1	3F
1	0	0	0	1	0	0	0	0	1	1	6
2	0	0	1	0	1	0	1	1	0	1	5B
3	0	0	1	1	1	0	0	1	1	1	4F
4	0	1	0	0	1	1	0	0	1	1	66
5	0	1	0	1	1	1	0	1	1	0	6D
6	0	1	1	0	1	1	1	1	1	0	7D
7	0	1	1	1	0	0	0	0	1	1	7
8	1	0	0	0	1	1	1	1	1	1	7F
9	1	0	0	1	1	1	0	1	1	1	67
A	1	0	1	0	1	1	1	0	1	1	77
B	1	0	1	1	1	1	1	1	1	0	7C
C	1	1	0	0	0	1	1	1	0	0	39
D	1	1	0	1	1	0	1	1	1	1	5E
E	1	1	1	0	1	1	1	1	0	0	79
F	1	1	1	1	1	1	1	0	0	1	71

## **Output equations for each of the 7 segments:**

### **For Sa:**

$$y = (A + B + C + D') (A + B' + C + D) (A' + B + C' + D') (A' + B' + C + D')$$

### **For Sb:**

$$y = (B' + C' + D) (A' + C' + D') (A' + B' + D) (A + B' + C + D')$$

### **For Sc:**

$$y = (A' + B' + D) (A' + B' + C') (A + B + C' + D)$$

### **For Sd:**

$$y = (B' + C' + D') (A + B + C + D') (A + B' + C + D) (A' + B + C' + D)$$

### **For Se:**

$$y = (A + D') (B + C + D') (A + B' + C)$$

### **For Sf:**

$$y = (A + B + D') (A + B + C') (A + C' + D') (A' + B' + C + D')$$

### **For Sg:**

$$y = (A + B + C) (A + B' + C' + D') (A' + B' + C + D)$$

## **Describing design method and design choice:**

### **Software requirement:**

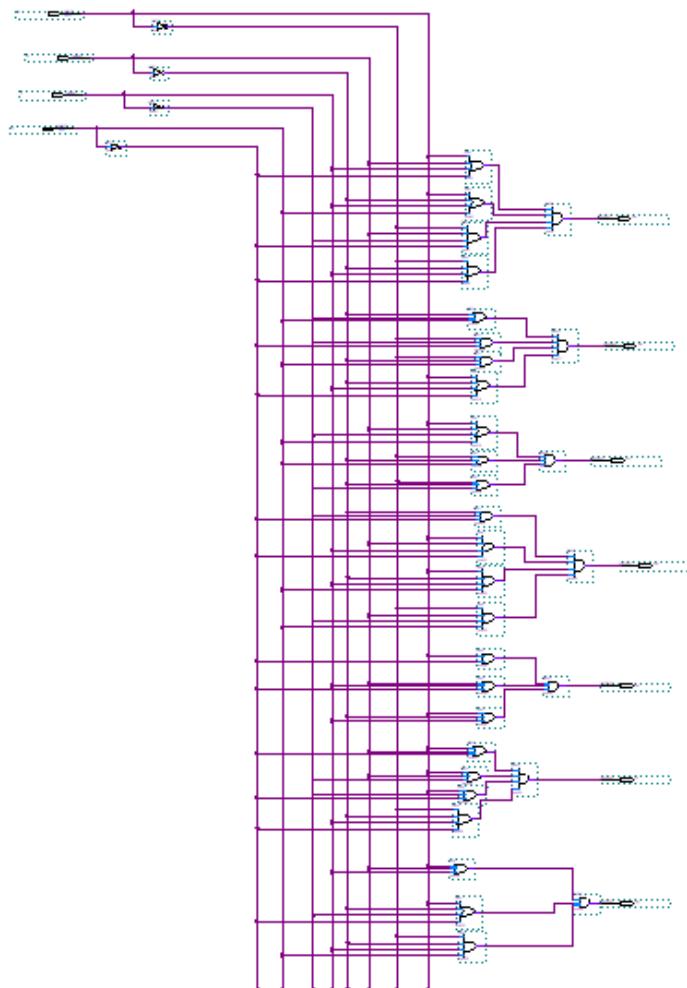
- 1.Quartus Prime
- 2.Modelsim

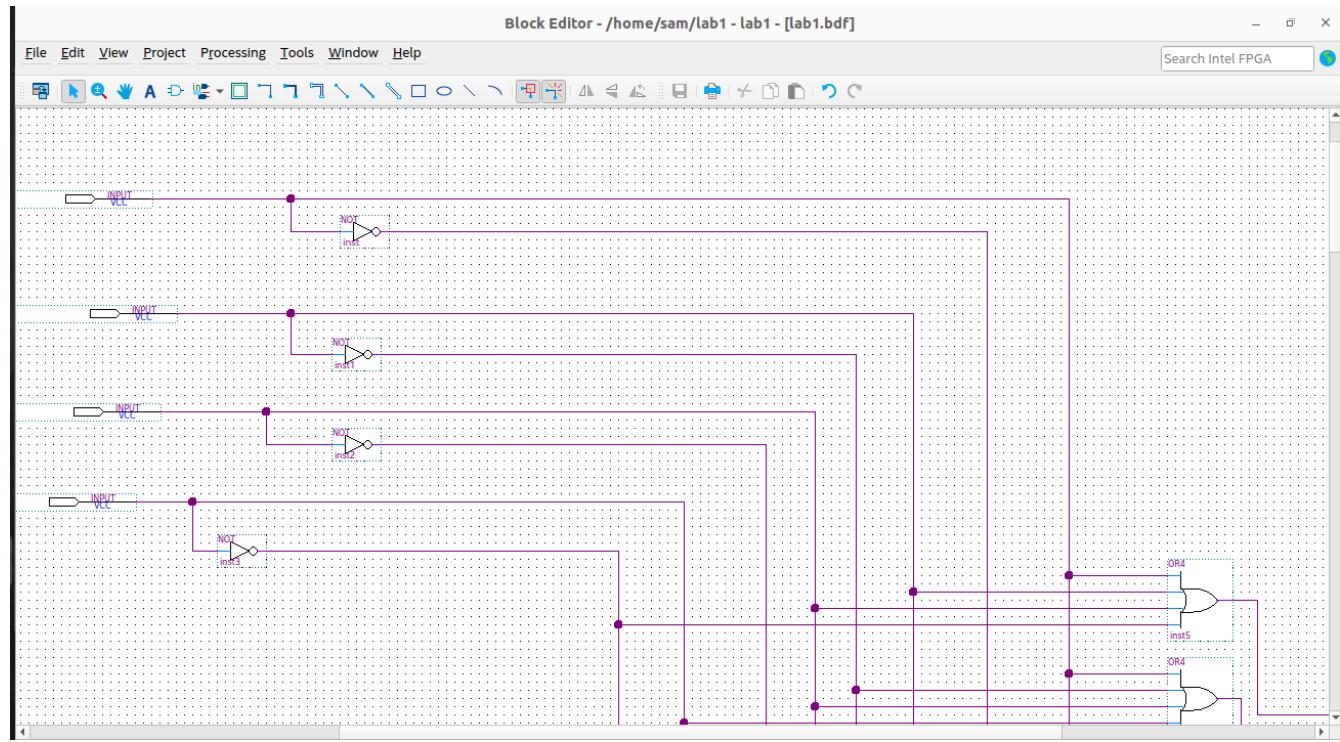
### **Hardware Requirement:**

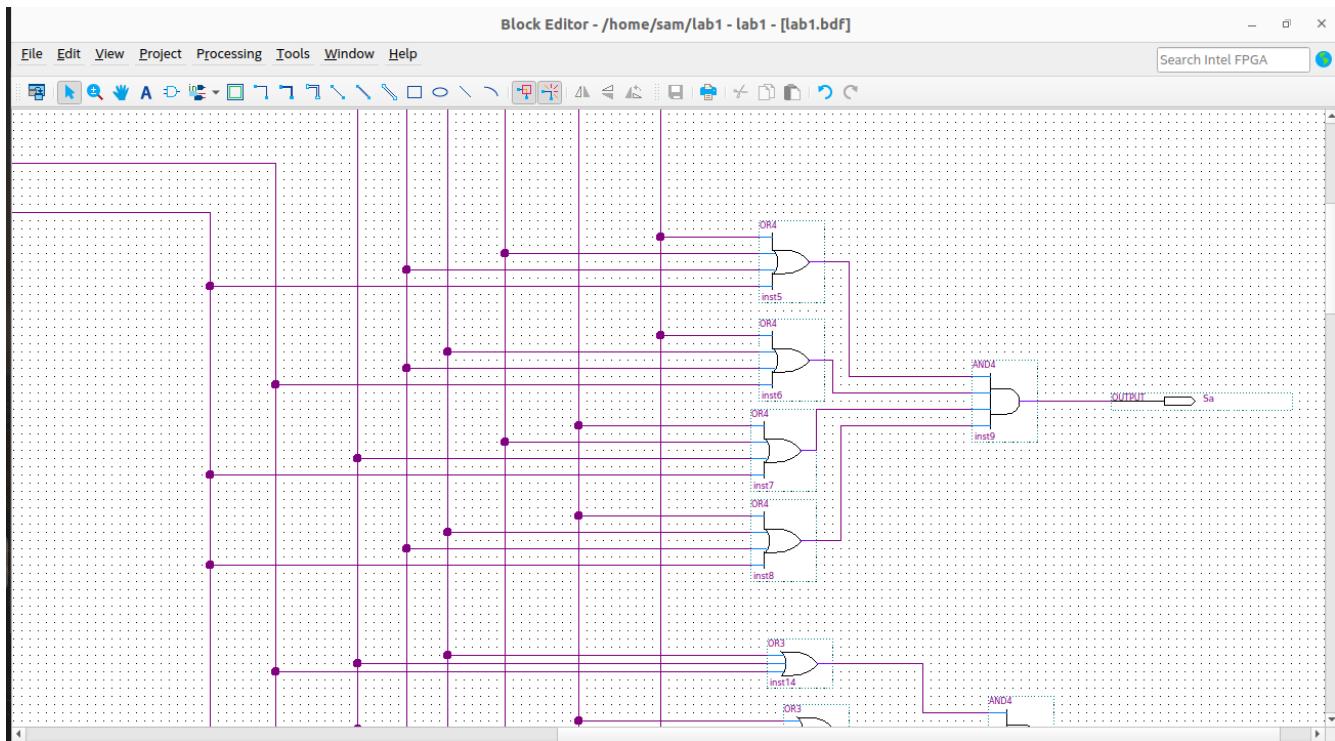
- 1.DE 10 nano
- 2.Breadboard
- 3.5161AS
- 4.220R register
- 5.Jumperwires

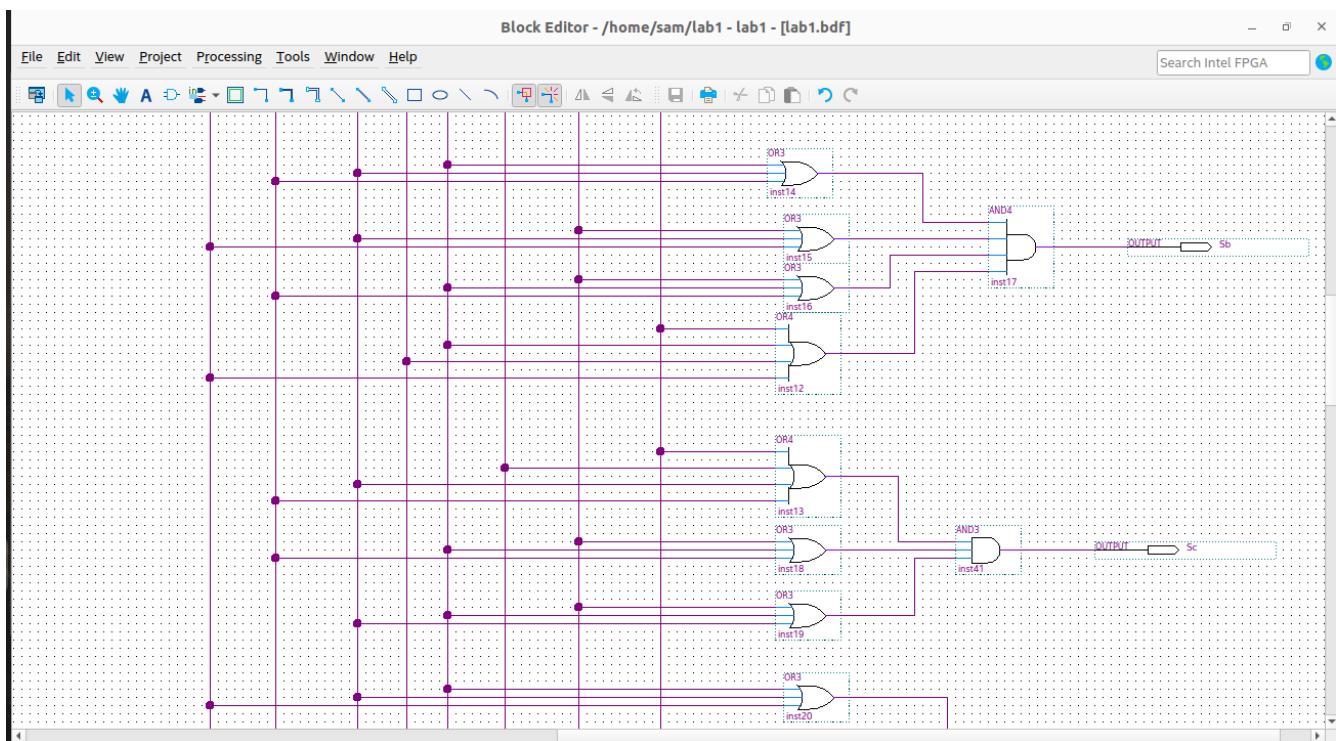
In the process of designing a 7-segment display circuit,I made so many mistakes and ,At last I opted for a Max-Term (Positive) approach within Quartus Prime as the foundation for my design. This choice was made due to its suitability for simplifying the logic required to drive a 7-segment display efficiently. The Max-Term representation allows for a more straightforward and optimized design by focusing on the high logic levels that need to be present in order to light up specific segments of the display. Before proceeding to hardware implementation on the DE10 Nano platform, I conducted extensive simulation using ModelSim to verify the correctness and functionality of the design.

**An image of Quartus schematic showing 7-segment display decoder logic:**



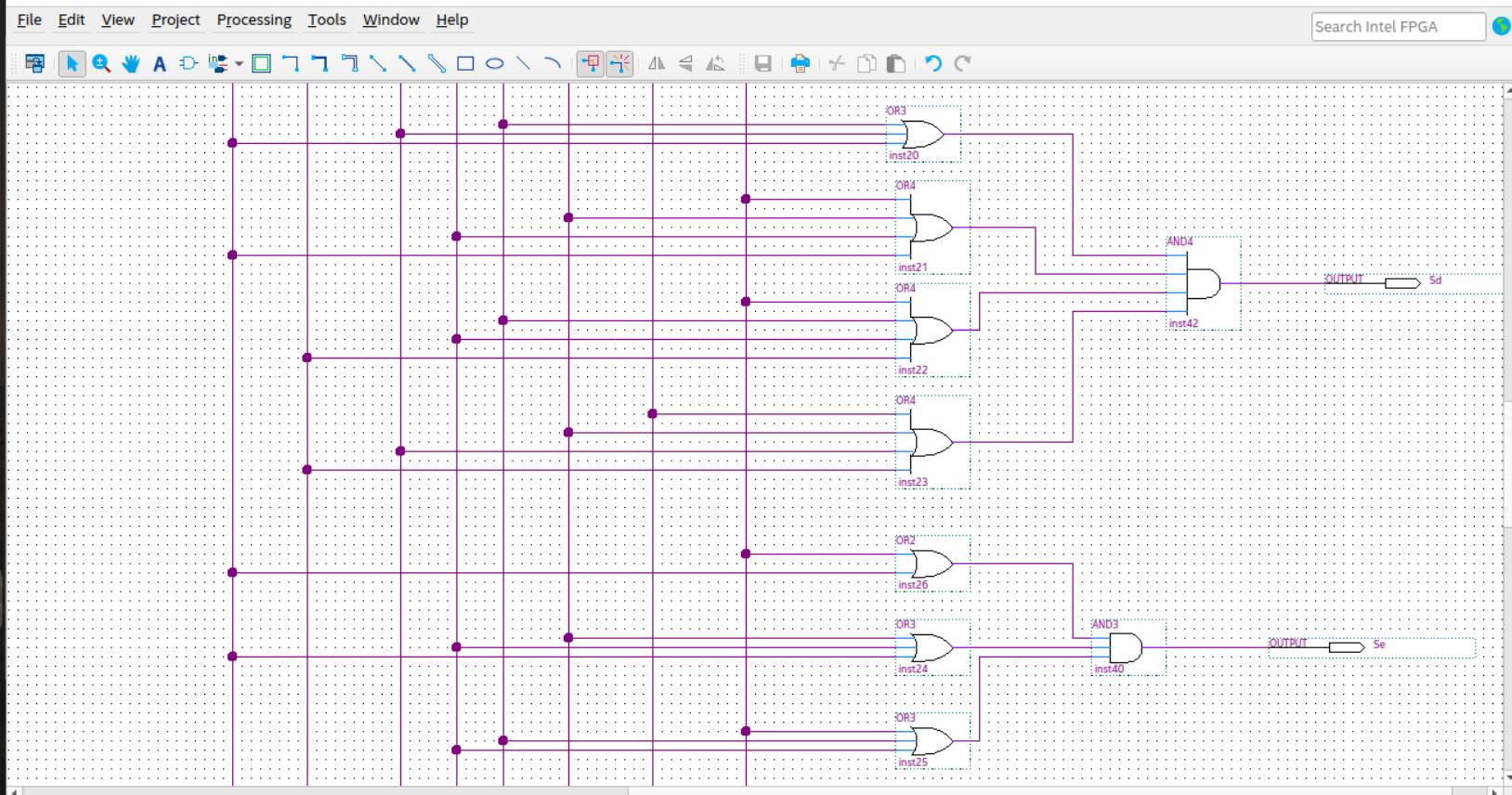


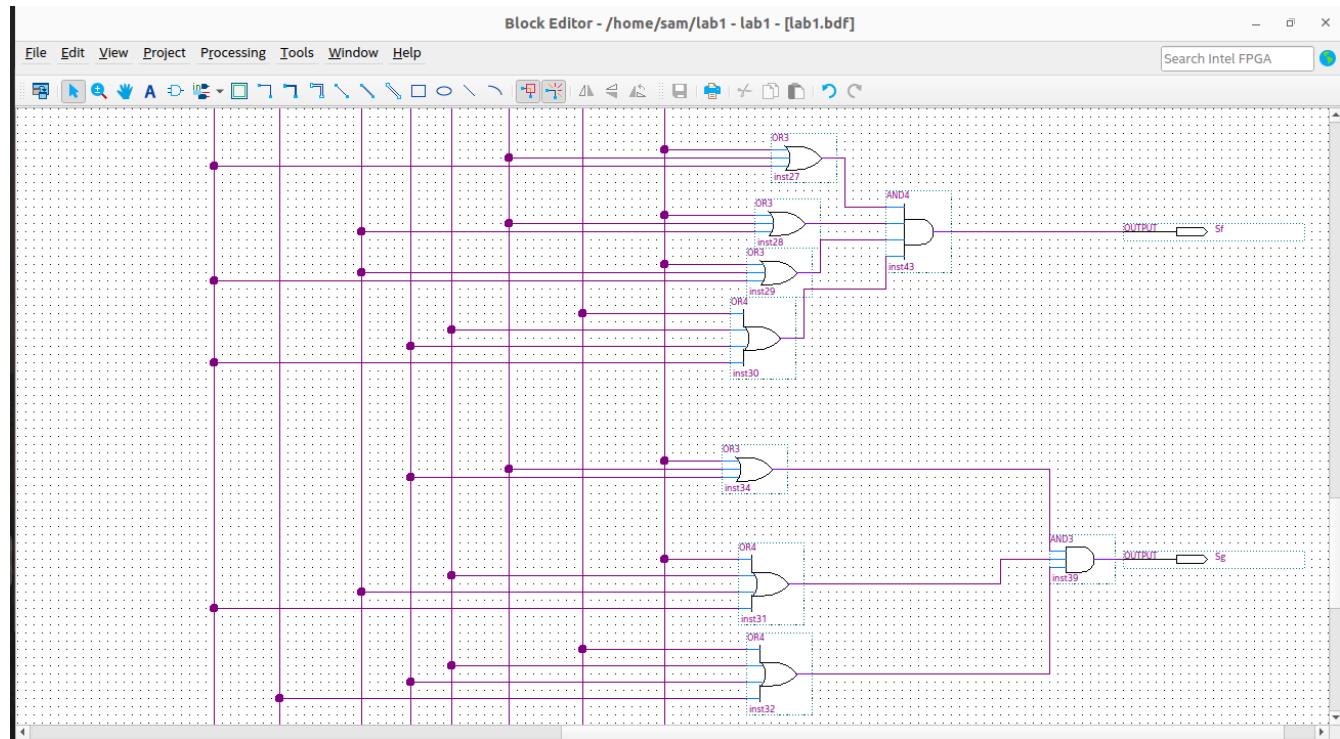


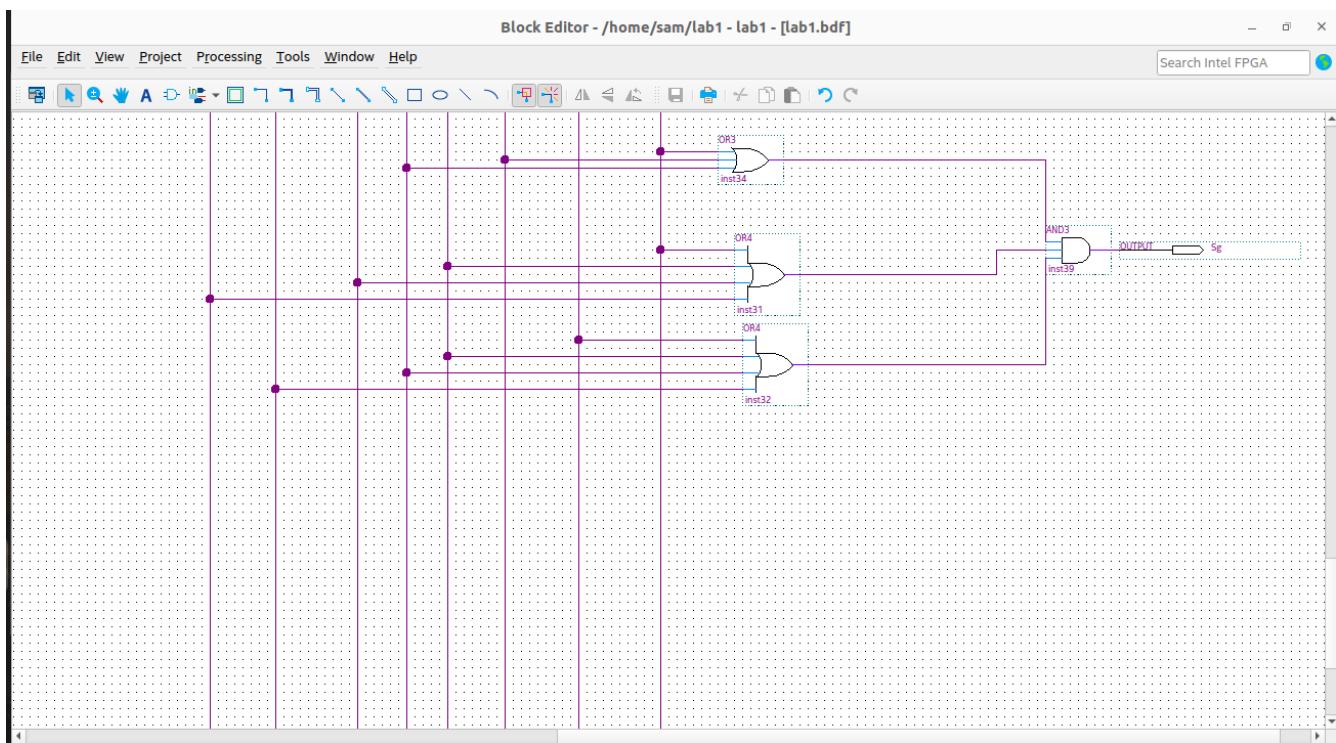


## Block Editor - /home/sam/lab1 - lab1 - [lab1.bdf]

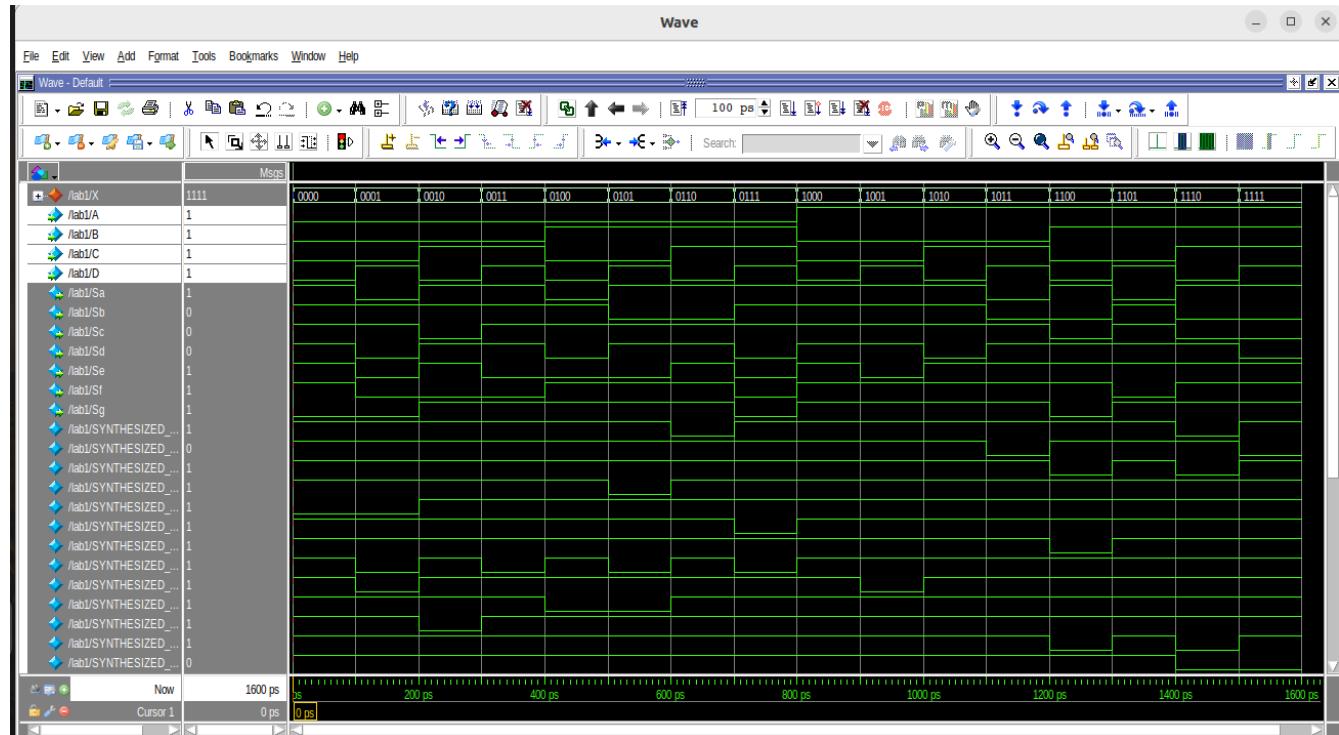
Search Intel FPGA







## An image of simulation waveforms :



## Snapshots:

Yes ,Circuits Works!

