

Demystifying Speed: Exploring the 4-Bit Carry Lookahead Adder

Introduction to advanced adder architectures
for faster arithmetic operations

EEM410 - IC DESIGN

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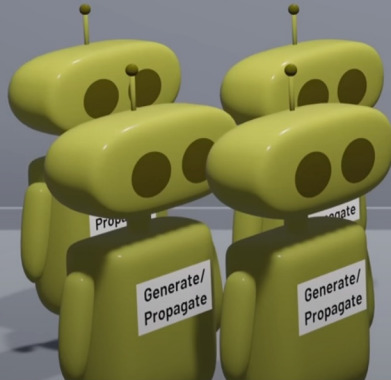
NAZIM

$$C_1 = G_0$$

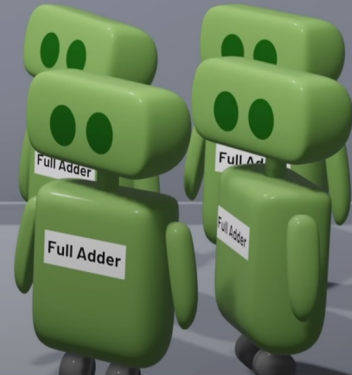
$$C_2 = G_1 \text{ or } G_0 P_1$$

$$C_3 = G_2 \text{ or } G_1 P_2 \text{ or } G_0 P_1 P_2$$

$$C_4 = G_3 \text{ or } G_2 P_3 \text{ or } G_1 P_2 P_3 \text{ or } G_0 P_1 P_2 P_3$$



$$C_{n+1} = G_n \text{ or } C_n P_n$$



$$P_i = A_i \oplus B_i$$

$$G_i = A_i \cdot B_i$$

$$C_{i+1} = P_i \cdot C_i + G_i \quad i = 1, 2, 3, 4 \quad Sum_i = P_i \oplus C_i$$

$$C_1 = P_0 \cdot C_0 + G_0 = P_0 \cdot C_{in} + G_0$$

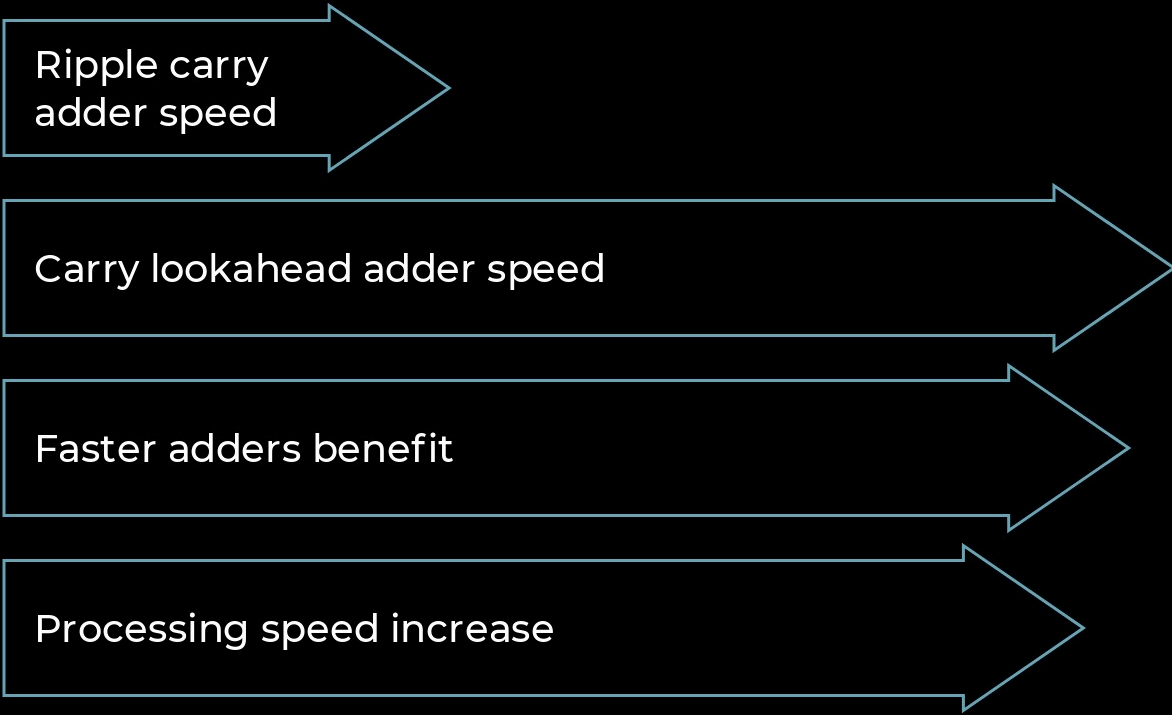
$$\begin{aligned} C_2 &= P_1 \cdot C_1 + G_1 = P_1 \cdot (P_0 \cdot C_0 + G_0) + G_1 \\ &= P_1 \cdot P_0 \cdot C_0 + P_1 \cdot G_0 + G_1 \end{aligned}$$

$$\begin{aligned} C_3 &= P_2 \cdot C_2 + G_2 = P_2 \cdot (P_1 \cdot C_1 + G_1) + G_2 \\ &= P_2 \cdot P_1 \cdot C_1 + P_2 \cdot G_1 + G_2 \\ &= P_2 \cdot P_1 \cdot (P_0 \cdot C_0 + G_0) + P_2 \cdot G_1 + G_2 \\ &= P_2 \cdot P_1 \cdot P_0 \cdot C_0 + P_2 \cdot P_1 \cdot G_0 + P_2 \cdot G_1 + G_2 \end{aligned}$$

$$\begin{aligned} C_{out} &= P_3 \cdot C_3 + G_3 = P_3 \cdot (P_2 \cdot C_2 + G_2) + G_3 \\ &= P_3 \cdot P_2 \cdot C_2 + P_3 \cdot G_2 + G_3 \\ &= P_3 \cdot P_2 \cdot (P_1 \cdot C_1 + G_1) + P_3 \cdot G_2 + G_3 \\ &= P_3 \cdot P_2 \cdot P_1 \cdot C_1 + P_3 \cdot P_2 \cdot G_1 + P_3 \cdot G_2 + G_3 \\ &= P_3 \cdot P_2 \cdot P_1 \cdot (P_0 \cdot C_0 + G_0) + P_3 \cdot P_2 \cdot G_1 + P_3 \cdot G_2 + G_3 \\ &= P_3 \cdot P_2 \cdot P_1 \cdot P_0 \cdot C_0 + P_3 \cdot P_2 \cdot P_1 \cdot G_0 + P_3 \cdot P_2 \cdot G_1 + P_3 \cdot G_2 + G_3 \end{aligned}$$

$$C_{i+1} = P_i \cdot C_i + G_i = (A_i \oplus B_i) \cdot C_i + A_i \cdot B_i$$

The Need for Speed



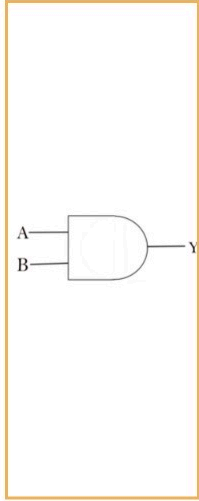
Ripple carry
adder speed

Carry lookahead adder speed

Faster adders benefit

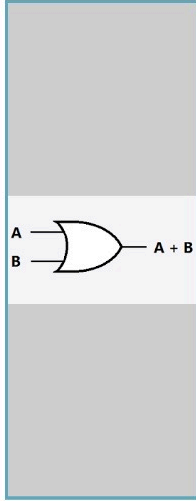
Processing speed increase

Building Blocks: Logic Gates



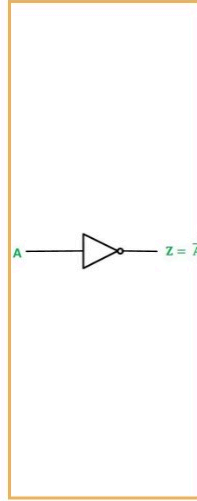
AND gate symbol

The AND gate outputs 1 only if both inputs are 1, otherwise outputs 0.



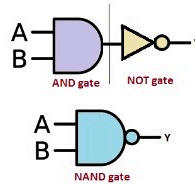
OR gate symbol

The OR gate outputs 1 if one or both inputs are 1, otherwise outputs 0.



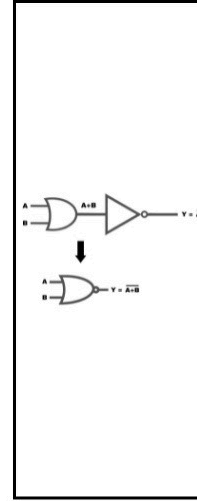
NOT gate symbol

The NOT gate outputs the opposite of its single input.



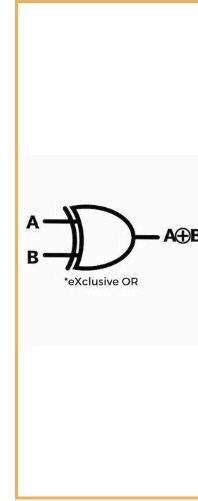
NAND gate symbol

The NAND gate outputs the opposite of the AND gate.



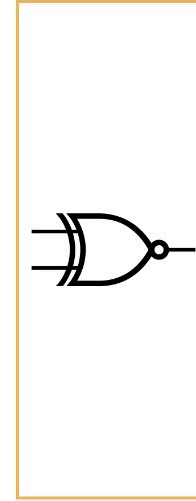
NOR gate symbol

The NOR gate outputs the opposite of the OR gate.










XOR gate symbol

The XOR gate outputs 1 if inputs differ, otherwise outputs 0.



XNOR gate symbol

The XNOR gate outputs the opposite of the XOR gate.

Symbol & notation	Explanation
 \bar{A}	The inverse NOT simply accepts and outputs the
 AB	All inputs must be before the output is 1
 \overline{AB}	Same as AND, but the inverse (NOT) So, perform AND first, then the output
 $A+B$	At least one input must to give a positive out All inputs could also
 $\overline{A+B}$	Same as OR, but the inverse (NOT) So, perform OR first, then to the output
 $A \oplus B$	Only one input can be to give a positive out If both are positive, the negative (0 or 1)
 $\overline{A \oplus B}$	All inputs must be the high or low for a positive Otherwise, the output or OFF

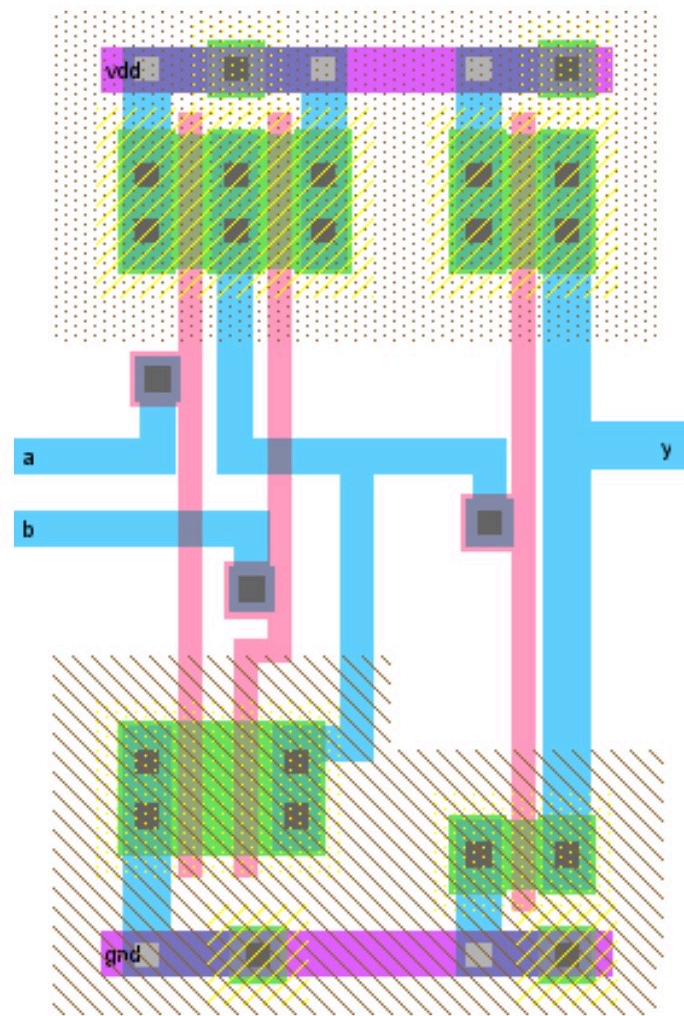
Logic gate circuit

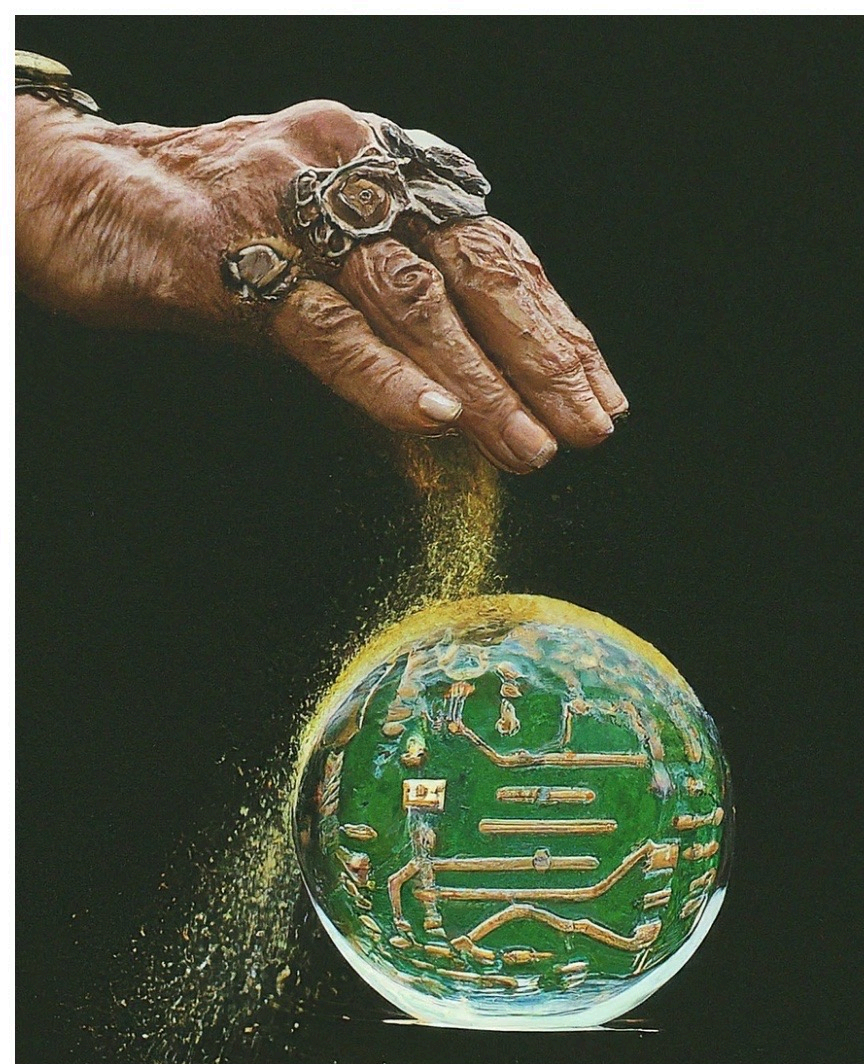
A simple logic gate circuit combining AND, OR, and NOT gates.



A Look Inside: Electric VLSI

VLSI (Very Large Scale Integration) enables complex digital circuits by packing millions of transistors onto a single integrated circuit chip. This high level of integration allows for greater functionality and performance. The carry lookahead adder explored in this presentation takes advantage of VLSI to quickly perform 4-bit addition in a single clock cycle.





CLA

carry lookahead adder

image generated by Gemini.

Introducing the Carry Lookahead Adder

What is a Carry Lookahead Adder?

A CLA calculates carries ahead of time to overcome limitations of ripple carry adders.

How Does it Work?

A CLA uses propagate and generate signals to determine carries before the sum.

Advantages Over Ripple Carry

Faster computation by reducing wait time for carries to ripple through each full adder.

Implementation

CLAs can be implemented with basic logic gates like AND, OR, and Inverters.

Applications

Used in CPUs and other digital circuits needing fast addition.

Challenges

More complex logic and circuitry than ripple carry adders.

Demystifying P and G Signals



P signals allow carry-in propagation

The diagram consists of four horizontal arrows pointing to the right, stacked vertically. The first two arrows are shorter and point to the right. The third arrow is longer and points to the right. The fourth arrow is the longest and points to the right. The text is contained within the rectangular part of each arrow.

G signals enable carry generation

Reduces carry delay by carry lookahead

Faster operation due to reduced carry delay

Benefits and Applications



Faster clock speeds for CPUs

Since the CLA performs carry propagation faster, it enables CPUs to operate at higher clock frequencies.



Lower latency for operations

The CLA reduces the latency for arithmetic logic unit (ALU) operations involving carries.



Faster processing

By reducing operation latency, the CLA boosts overall processing speed for applications like video encoding, 3D rendering, scientific computing, etc.

The 4-bit carry lookahead adder enables higher CPU clock speeds and faster processing for compute-intensive applications by accelerating carry propagation.

Where..?

- **CPUs (Central Processing Unit)**

The ALU (arithmetic logic unit)in CPUs uses CLAs to speed up addition, subtraction, etc.

- **DSPs (Digital Signal Processors)**

CLAs improve speed and efficiency of addition/multiplication in DSPs

- **Cryptography**

- **HPCs (High-performance computing)**

Supercomputers use CLAs for fast scientific/engineering computations

- **CLAs assist in error correction**

for fast encoding/decoding



Conclusion

The 4-bit carry lookahead adder allows for faster addition by pre-computing the carry bits. This enables all the sum bits to be calculated in parallel, significantly speeding up the addition operation. The key takeaways are that carry lookahead reduces delay by avoiding rippling carries, and parallelizes the addition process by calculating multiple sums simultaneously.