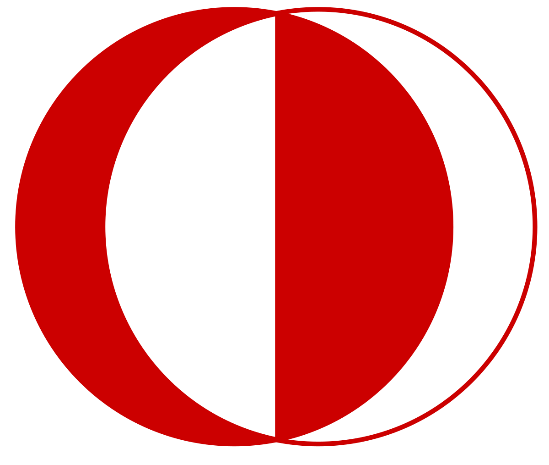
**EE463 STATIC POWER**

**CONVERSION-I**

**TERM PROJECT**

**FINAL REPORT**



Date: 07.02.2022

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# INTRODUCTION

In our term project we were required to build a motor driver circuitry which will run a DC motor via AC grid. In this report, the topology we have chosen and the reason behind it is discussed. Necessary analytical calculations are given. Simulation of the circuitry is talked upon, and component selection is presented. Next, thermal calculations and the implementation are provided. Finally, demonstration results are talked upon, both rated operation and kettle test.

# PROJECT DEFINITION

In this project, as mentioned in introduction, we are asked to build a motor driver supplied from the grid -either single or three phase- that can drive an industrial shunt motor with a rated 1500 rpm speed, 220 V and 23.4 A. Field excitation is given by an external DC source. There are several bonus requirements, among which we have chosen Tea Bonus, Analog Controller Bonus and Industrial Design Bonus to implement. For Tea Bonus, the motor that is run with our driver is coupled to a generator which is used to supply voltage to a kettle drawing around 1.5 kW. Our design should be able to withstand until the water is boiled. For Analog Controller Bonus, as the name suggests, the driver needs to be implemented with an analog controller rather than digital. And for Industrial Bonus, the driver should be encased within a box with all ports labeled.

# TOPOLOGY SELECTION

For this project, basic topologies that we considered are as follows:

* *Center-tap transformer:* This topology turned out to be way expensive compared to others (~300 TL), therefore it is automatically eliminated. Besides this, in the small scale it has only one tap at the secondary, decreasing the flexibility of the output voltage, if used as a single component.
* *Single phase full bridge diode rectifier with buck converter:* This topology is comparably cheaper compared to others. However maximum output voltage that a single-phase diode rectifier can provide is 207 V, when variac is at 100%. That means for a maximum operational output of 180 V, duty cycle (DC) of the buck converter should be around 90%, which is not desired since as DC gets closer to the edges, its output becomes instable and non-reliable.
* *Single phase thyristor rectifier:* Similarly with the previous topology, maximum output this can provide is 207 V. For 180 V output, 30° of firing angle is required, which is reasonable. However, compared to the next topology especially, two gate driver circuitry is needed, complicating the matters. Even though pricewise being comparable with the three phase full bridge diode rectifier with buck converter, this topology is found to be more error-prone due to this multiple gate driver requirement and hence is not chosen.
* *Three phase full bridge diode rectifier with buck converter:* This topology is decided upon at the end, due to it being cheap and its ease of implementation. Since the motor acts like a capacitive load in addition with its series parasitic inductance, two components of the buck converter is not necessary, decreasing the cost even further and simplifying the circuitry. Only a gate driver is basically needed, which is doable.
* *Three phase thyristor rectifier:* Compared with the single phase case, cost and complexity is tripled, thus this topology is, too, eliminated.

# SOLUTION

Graphical user interface, application

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Figure 1. Schematic model of the selected topology

First of all, the LC filter at the output of the buck converter will not be used because the DC motor has a very large inductance that can filter the current in the square waveform. In other words, the DC machine will be driven with the square wave.

Secondly, transient current must be diminished to obtain a soft start operation. There are two ways: designing a controller (closed-loop operation) or designing a gate driver circuit such that the duty cycle starts from very low values and rises up to the maximum limit manually (open-loop operation). At first, a closed-loop PI controller is tried via TL494 IC; however, it is not ended with success. Therefore, due to lack of time, the open-loop operation is selected, and the following gate-driver circuit is designed.

Finally, the input voltage is desired according to the limited maximum duty cycle, which is 0.65. The duty cycle is limited in order to decrease the conduction loss, and the switching frequency is limited to 1 kHz to reduce the switching loss. So, the required input voltage for obtaining 180 V output voltage is calculated as


## Gate Driver Circuit

As previously mentioned, the open-loop operation with soft start is aimed. The PWM is generated via 555 timer. So, after brief research, the following gate driver circuit is designed, schematic of which is given in Figure 3. The numbers represent the ports of the timer in pin diagram. The pin diagram and appearance of the 555 timer is also presented below in Figure 2.

A picture containing electronics, circuit

Description automatically generatedDiagram, schematic

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Figure 2. 555 timer photograph and pin diagram

Diagram

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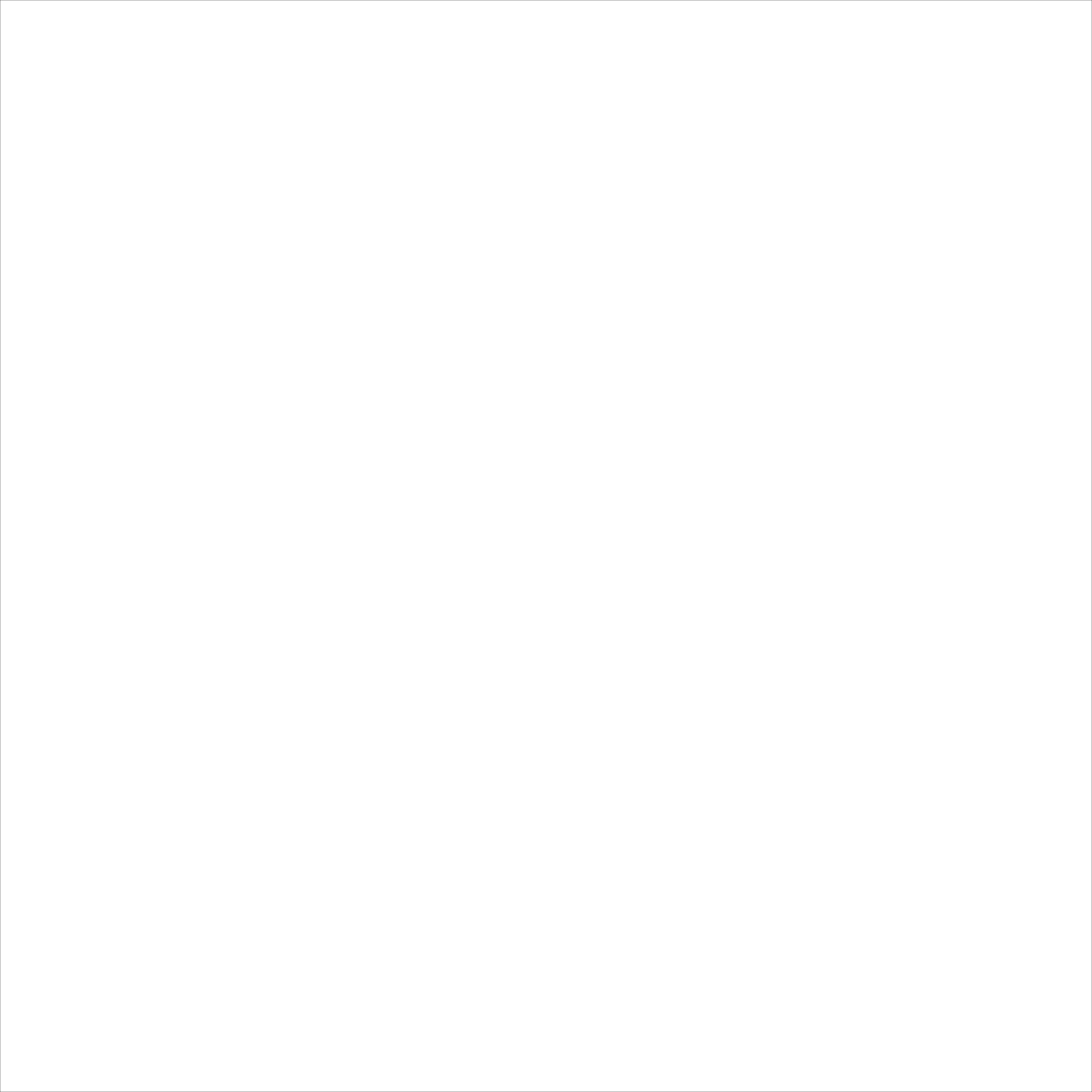


Figure 3. Gate driver circuitry

According to this topology, the duty cycle can be expressed as . Furthermore, the switching frequency is calculated as . Then, in order to achieve the desired duty cycle and switching frequency, resistor and capacitor parameters are tuned as , , and . RA will be composed of two series potentiometers in order to change the duty cycle. Specifically speaking, RA will be consisting of 100 kΩ and 10 kΩ resistors, which are series. The soft-start operation is achieved via 10 kΩ POT while the 100 kΩ POT is set as zero. After the start, duty cycle is adjusted via 100 kΩ POT.

After the 555 timer, the optocoupler is needed to isolate the gate driver circuit, i.e., prevent the gate driver circuit. For that purpose, the internal schematic of a typical optocoupler is presented to illustrate its working principle.

Diagram, engineering drawing, schematic

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Figure 4. Schematic of optocoupler

The optocoupler utilizes the light to isolate one side from another, that’s what their name comes from. The picture above is the inside of the optocoupler. So, a 1 kΩ resistor will be placed to the pin 2 in order to limit the LED current in the input side of the optocoupler. Also, the PWM signal generated by the timer circuit is also connected to the second pin. Then, at the 6th or 7th pin, the same PWM signal will also be obtained. The 5th pin will be connected to the switch’s low voltage pin, which is the emitter.

Also, according to the datasheet of the switch (for reasoning of component selection please refer to the preceding simulation results and component selection sections), there must be at least a 10 Ω resistor placed in the gate of the IGBT. However, this value is for nearly perfect applications. Since it is not possible to design such a circuit, a 50 Ω resistor is used to increase the opening time of the switch, i.e., it is used to decrease the switching speed. There is also a 20 kΩ resistor for discharging the junction of the switch when it is turning of. Final version of the gate driver circuit including the IGBT is presented in Figure 5.

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Figure 5. Schematic of the resultant gate driver

## Buck Converter

Buck converter is a basic step-down converter, and it will be utilized to drop the DC link voltage to the at most 180 V depending on the duty cycle. The basic buck converter topology is presented in Figure 6.

Diagram

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Figure 6. Schematic model of the basic buck converter

It can be easily seen that whenever switch is on, the output voltage is equal to DC link voltage, and whenever the diode is conducting, output voltage will be zero. Mathematically speaking



If the mean value of the output voltage is calculated, it can be seen that it is equal to 180 V at the maximum duty cycle which is the desired output voltage according to the project definition. In more detail,


In the preceding section, this solution procedure will be implemented in Simulink environment except the gate driver circuit because the components in gate driver circuit are not available in Simulink. So, gate driver topology will be implemented and simulated in LTSpice environment.

# SIMULATION RESULTS

The desired topology is simulated via Simulink environment. The Simulink model can be seen in Figure 7. According to the model, steady state switch current and voltage, diode current and voltage, and output voltage and current are given in Figures 8-10.

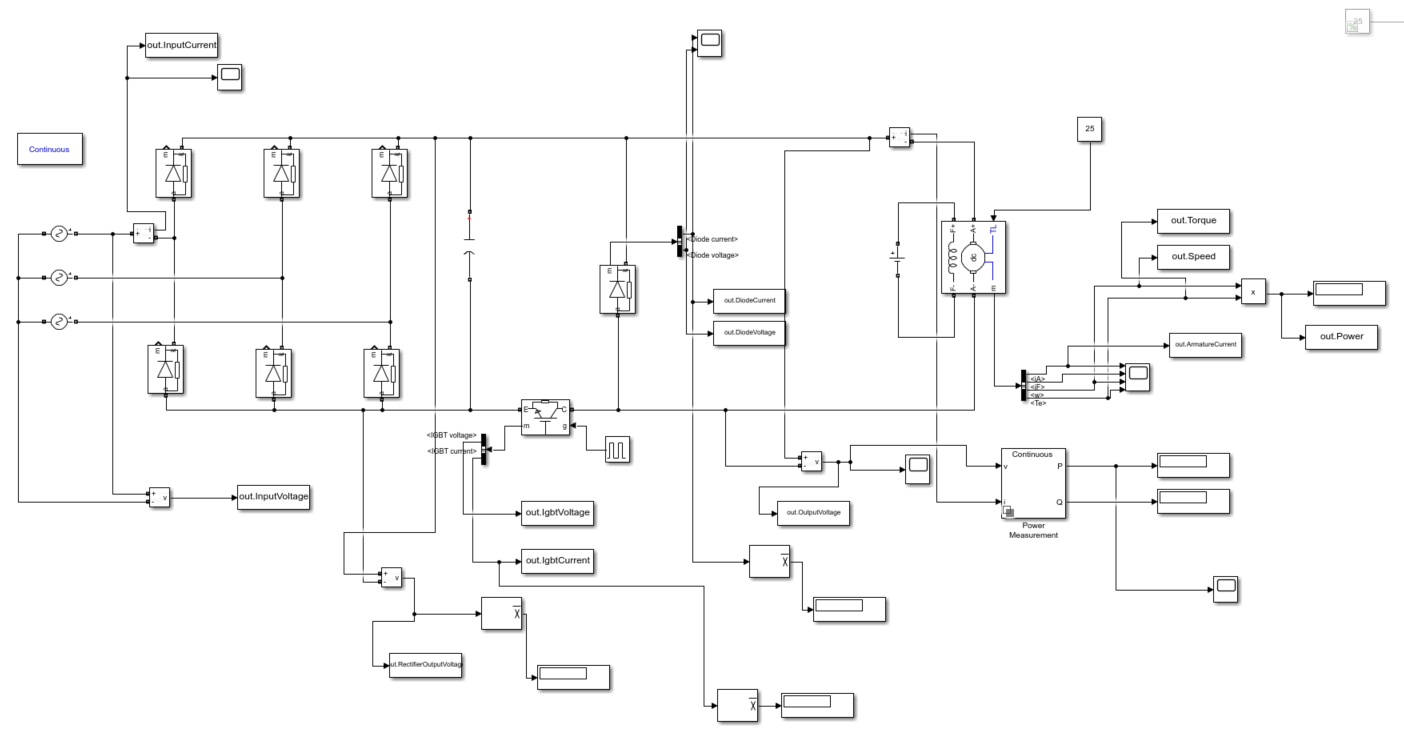


Figure 7. Simulink model

Chart

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Figure 8. Output voltage and armature current waveforms

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Figure 9. IGBT voltage and current waveforms

Chart

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Figure 10. Freewheeling diode voltage and current waveforms

However, during transient, current flows through the circuit is extremely high that has capability of damaging the components, which can also be seen from the Figures 11-13.

Chart, bar chart

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Figure 11. Input current waveform

Chart, histogram

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Figure 12. IGBT current waveform

Chart

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Figure 13. Freewheeling diode current waveform

The inrush current in transient part will be eliminated with the help of the gate designed gate driver circuit.

The simulation result of the gate driver circuit is presented in Figure 14, excluding the optocoupler because it has no effect on the output of the gate driver circuit.

Background pattern

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Figure 14. Output waveform

# COMPONENT SELECTION

According to the simulation results and calculations, the components are decided as follows.

* As a rectifier, a 50 Hz three-phase rectifier module is chosen. The specific model of this rectifier is IXYS VUO36-16NO8. It is bought from a local electronic store in Ankara.
* The DC link capacitor must withstand at least 276.75 V. Also, in the simulation model, various capacitor values are tried and according to price and performance, two 330 μF 400 V electrolytic capacitors are chosen. It is bought from *“direnc.net”*. Its specific model and datasheet are not available on the seller’s site.
* At first, the switch is thought of as MOSFET whereas due to global chip shortage, MOSFETs with higher voltage ratings were too expensive, even are not in stock. So, IGBT present in the laboratory is chosen since it meets the requirements, which are withstanding around 300 V and must carry a 10 A in average, and gives a safety margin. The specific model of the IGBT is IXGH24N60C4D1.
* Freewheeling diode is chosen as MUR3060PT because it satisfies the values obtained from the simulation, which should carry around 10 A in average, and it is available in a local electronic store in Ankara.
* TLP250 optocoupler is chosen since it is available in the laboratory.

Datasheets of all the components can be seen in [GitHub Repository.](https://github.com/sametyakut/EE463-TERM-PROJECT)

# THERMAL CALCULATIONS

It is known that thermal calculation is necessary for providing suitable conditions for the temperature vulnerable circuit components. Otherwise, generally, because of the overheating components can be defected or can be harmed. The main reason of the heat increase in a circuit is power losses. These power losses occur as heat in the components so, doing power loss calculations before the thermal calculations is necessary.

## Power Losses:

Semiconductors can be heated to the high temperatures due to the losses inside of them. If the temperature exceeds the limit, semiconductor device can be broken. Hence, it must be considered the losses in the semiconductor devices:

* Switching losses
* Conduction losses

**-Switching Loss formula (Reverse Recovery Loss):**

**-Conduction Loss Formula**

### **Three-phase rectifier module VUO36-16NO8:**

From the simulation report, it was indicated that switching loss for this component was unsignificant. So, let’s check for the conduction loss:

(Maximum average current that passes through a diode in our design)



Figure 15. Thermal resistance of the three-phase rectifier module

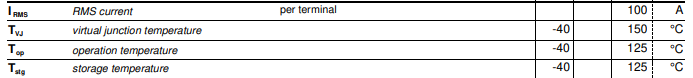


Figure 16. Temperature specifications of the three-phase rectifier module

Let’s assume Tambient = 40˚C. Then, calculate the temperature of the rectifier module.

Actually, this temperature is in the range of the device’s operation temperature. However, we were also decided to implement a heatsink to this device too. We planned to implement HBT254 to the rectifier.

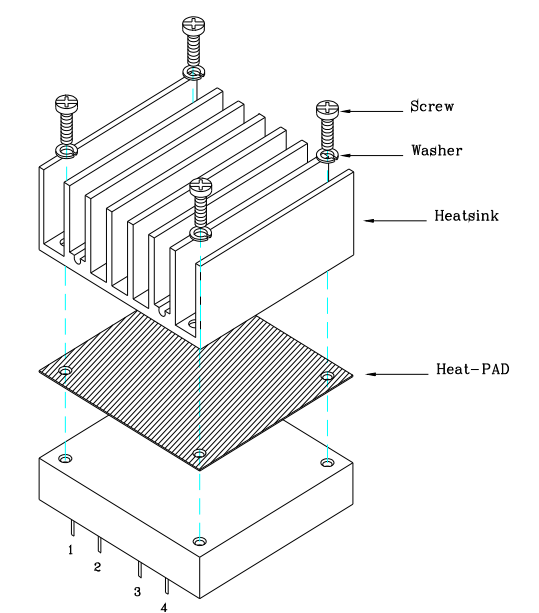


Figure 17. Possible implementation of the heatsink to the rectifier module

This heatsink has thermal resistance as RHA = 3 (. Hence, by using this heatsink,

### **Freewheeling Diode DSEP30-06B:**

Beside of the three-phase rectifier module, for the freewheeling diode, it was indicated that switching loss for this component was unsignificant in the simulation report. So, let’s check for the conduction loss:

(Current that passes through this diode in our design)

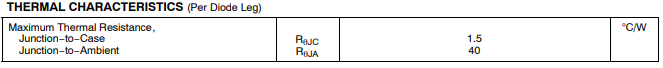


Figure 18. Thermal resistance of the diode



Figure 19. Operating temperature of the diode

Again, assume Tambient = 40˚C. Now, calculate the temperature of the diode.

As it can be observed, temperature of the diode exceeds the operating temperature range. Hence, heatsink and fan usage is necessary. For the heatsink, we have decided to use HBT254.

This heatsink has thermal resistance as RHA = 3 (. On the other hand, it will be used a 12V DC San Ace 80 fan.

A close-up of a mechanical device

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Figure 20. Possible fan selection

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Figure 21. DC fan specifications

It was planned to use 77−6020D12 and it has CFM = 22.43, which equal to LFM = 578.83. Besides, heatsink’s thermal resistance is 0.95 ( under 400 LFM. Hence, by using this heatsink and fan,

### **IGBT IXGH24N60C4D1:**

The IGBT used as a switch in the buck converter is IXGH24N60C4D1. For this IGBT, let’s do the loss calculations:

(Switch on energy of the IGBT)

(Switch off energy of the IGBT)

(Collector-Emitter voltage in saturation)

(Current passes through this IGBT when it is conducting)

Hence,

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Figure 21. Temperature specifications of the IGBT



Figure 22. Thermal resistance of the IGBT

We have decided to use the same fan and same heatsink that we planned to use for the diode. Hence, same calculations are valid for the IGBT.

Assume Tambient = 40˚C.

So, for the worst case, IGBT can stand and work properly.

# DEMO RESULTS

In the demo day, procedure was like the following:

1. Make all the necessary connections.
2. Set the field excitation to 150 V.
3. Set the variac to a level that motor can receive rated voltage (~50%).
4. Give the dc input to start the switching.
5. Manipulate the POTs to change the speed of the motor.

Initially, these procedures were done, and the results are noted, given in Figures 23-30.

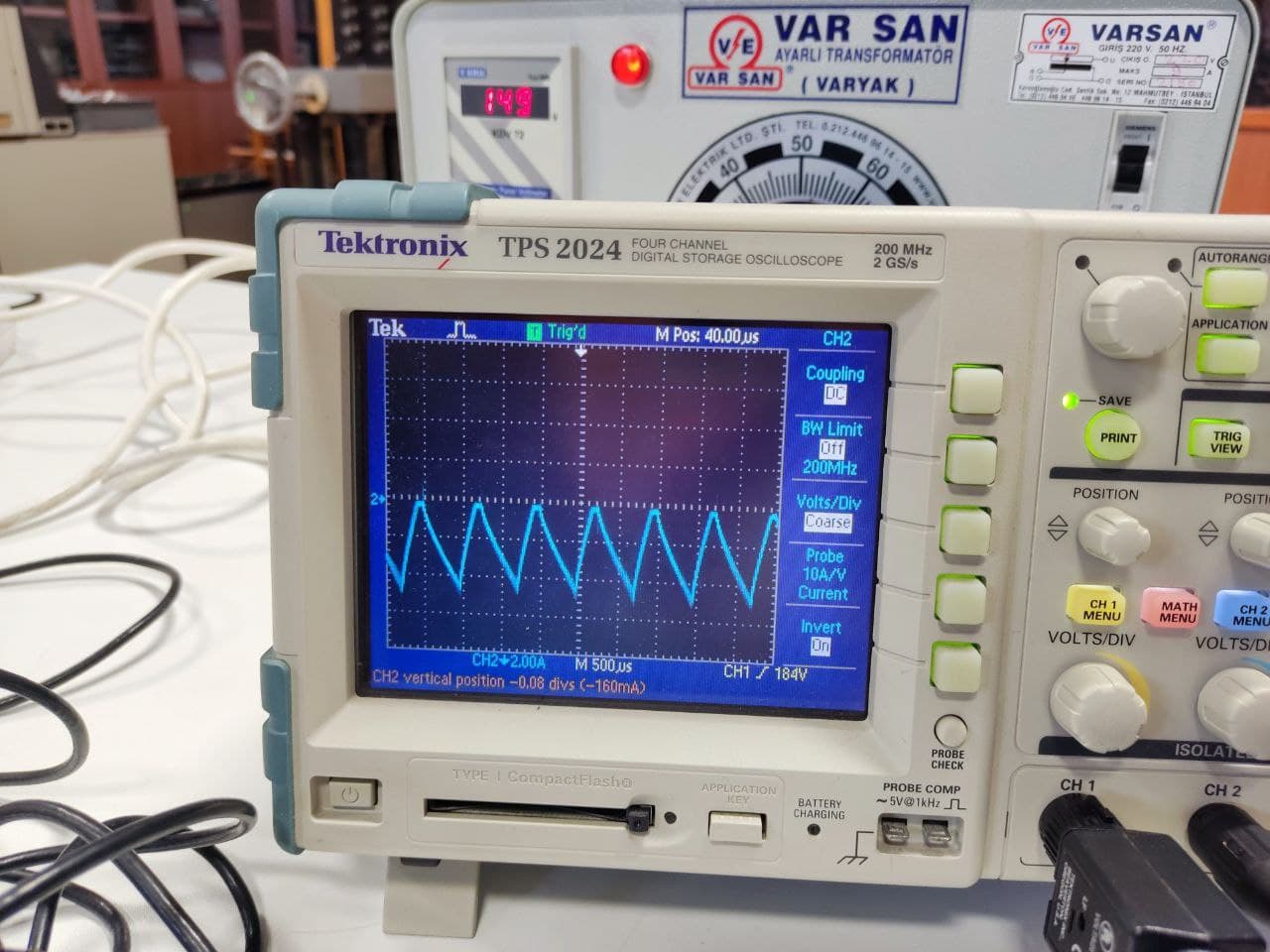
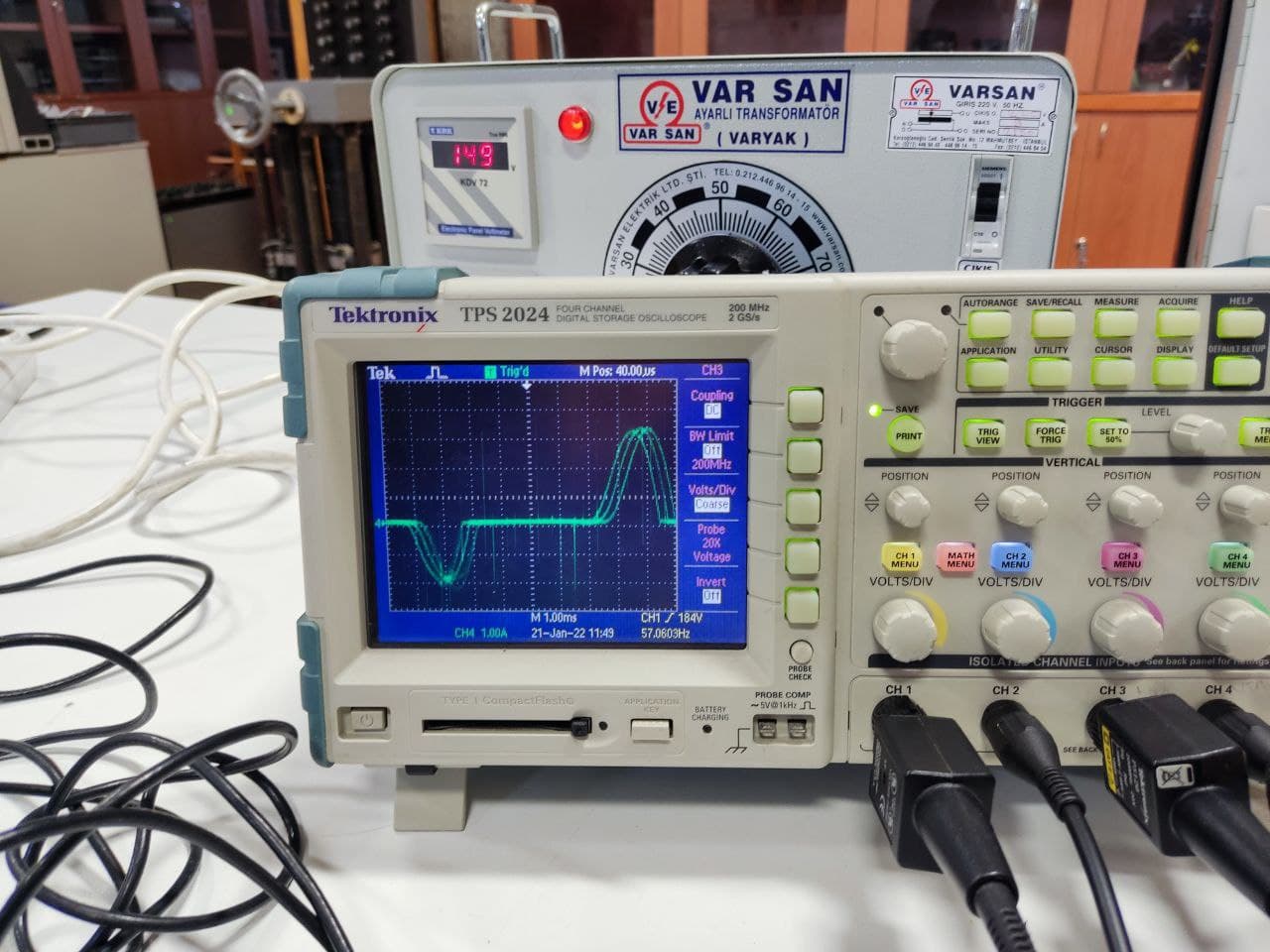
 

Figure 23. Input current Figure 24. Output current

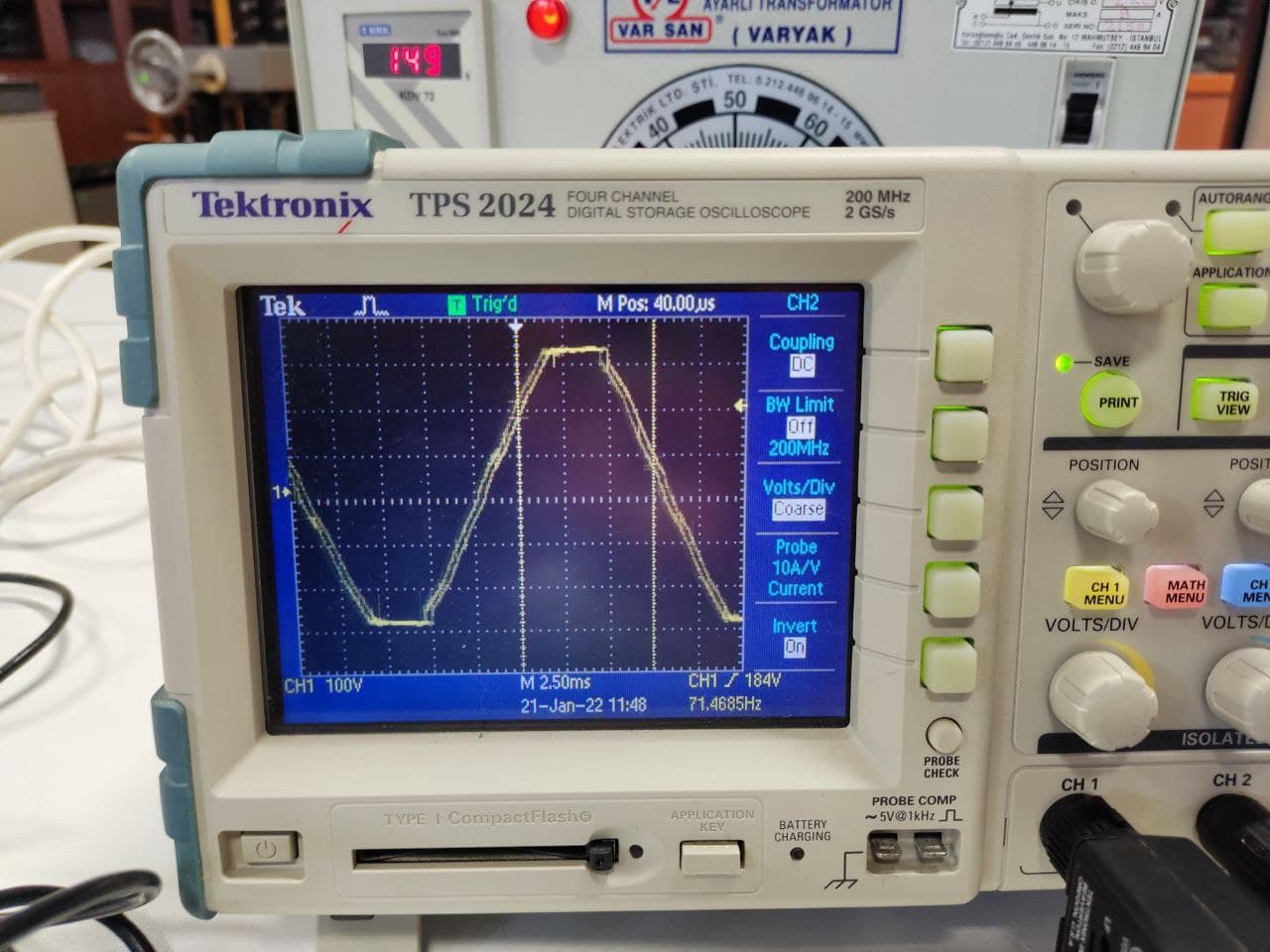
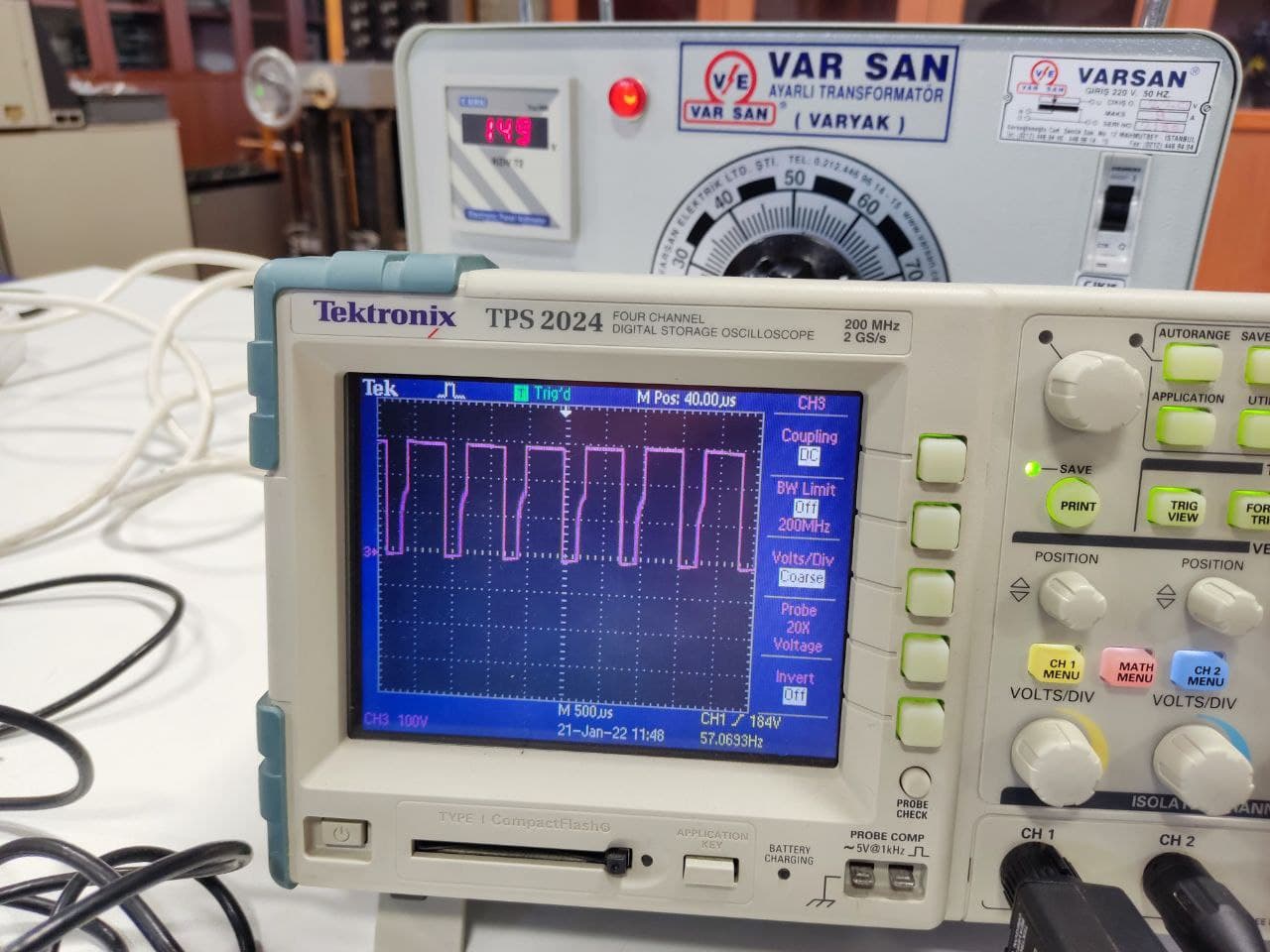
 

Figure 25. Input voltage Figure 26. Output voltage

First peculiar thing noticed was the clipping of the input voltage waveform, as seen in Figure 25, which was assumed and used to be sinusoidal. After brief research, it is found to be either a result of the core saturation of the transformer within variac, or a natural output of capacitor voltage transformer (CVT), which uses an initial capacitive voltage divider, that may cause this behaviour. From the photos we have taken, we could not see the model of the variac, therefore could not further elaborate on which is the cause. But it is not something affecting the operation of the driver; therefore, it is not examined further.

Figure 23 is better analyzed if one imagines it as inverted with respected to x axis, our probe connection was the other way around. Current has a ripple of around 4 A, just touching DCM boundary. Approximating the waveform as triangular, its rms is around , which can be verified by the power meter measurement seen in Figure 27, in Channel 4.

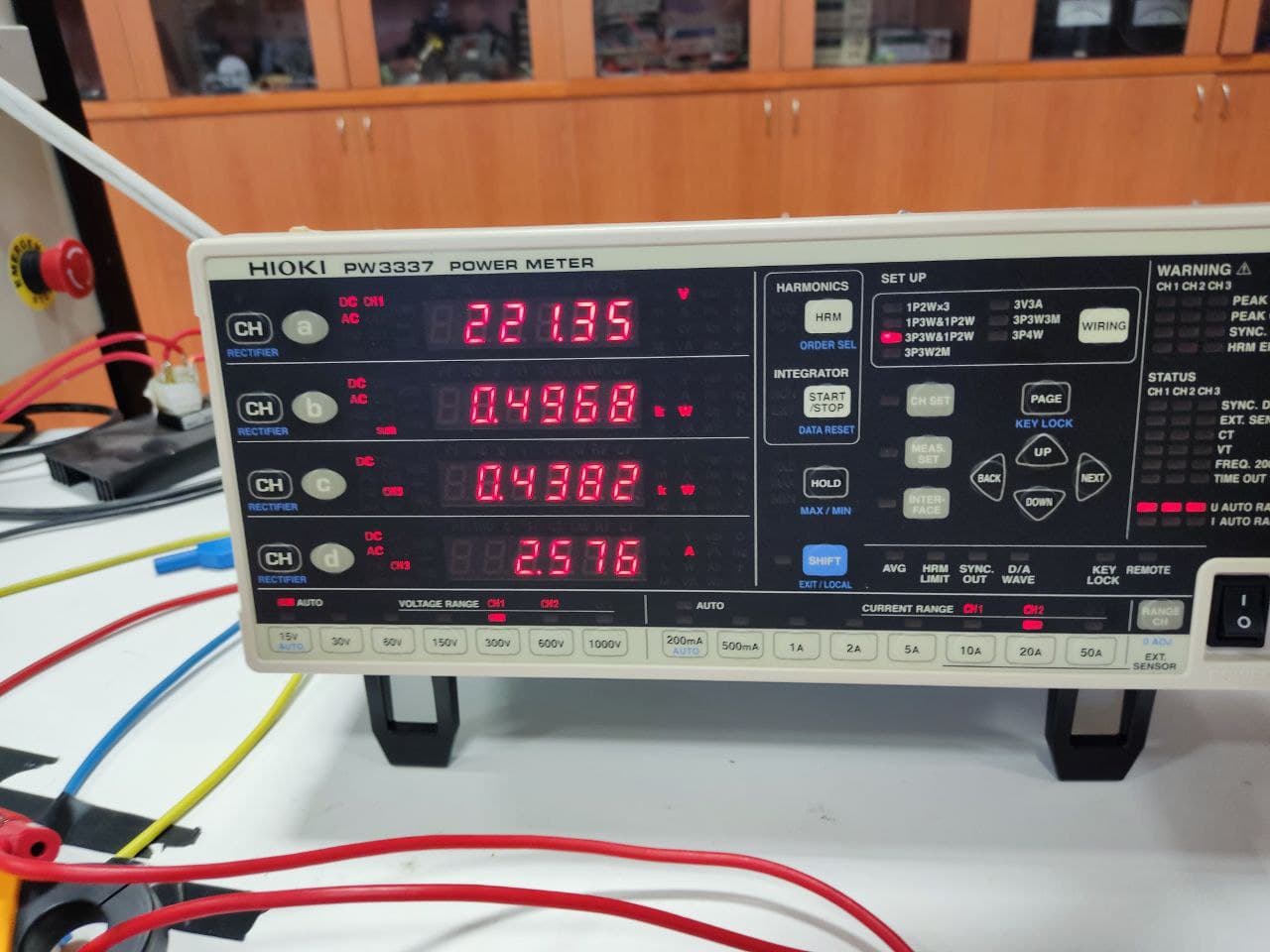


Figure 27. Power meter results

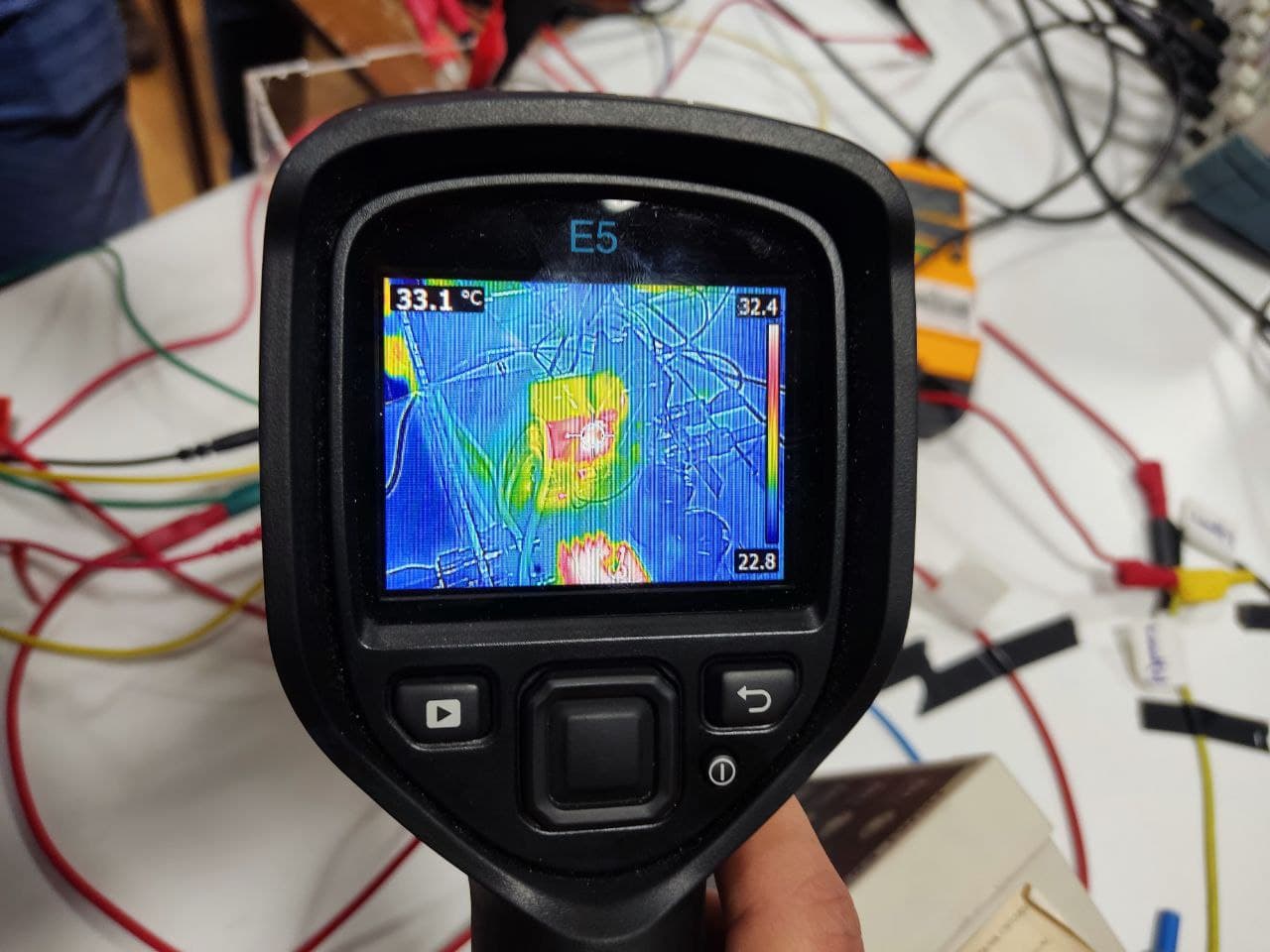


Figure 28. Temperature of the IGBT

Since we planned to get the tea bonus, a test with the kettle had to be done too. Kettle test was done with the following procedure:

1. Motor is stopped by arranging the duty cycle to 0%
2. Kettle is connected
3. Duty cycle is increased by arranging the POTs
4. After obtaining 1.8kW at the output, duty cycle is fixed
5. Wait till the water boils.

After this procedure was done, results are noted too.

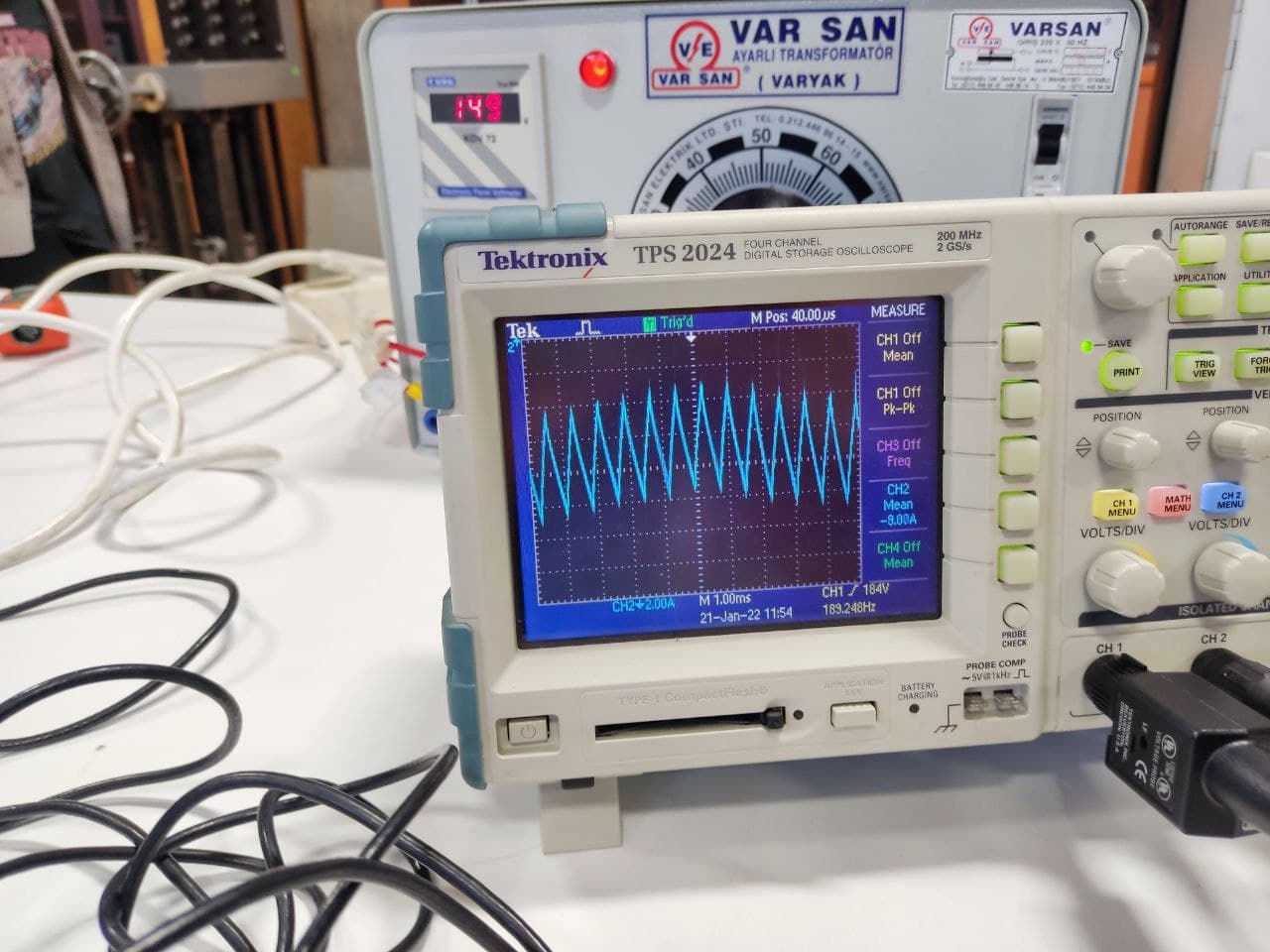


Figure 18:Input current of the kettle test

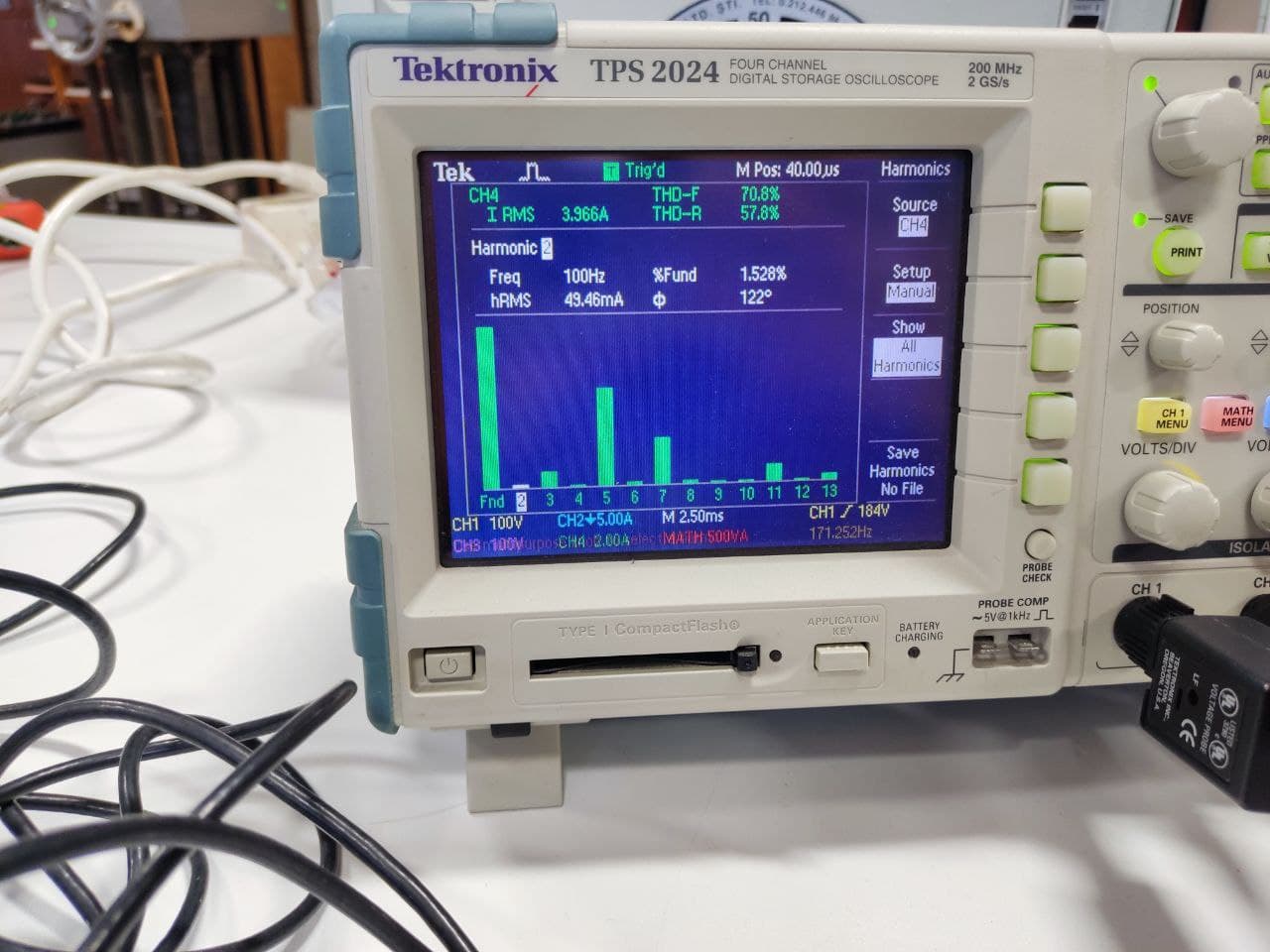


Figure 19:Output current THD of the kettle test

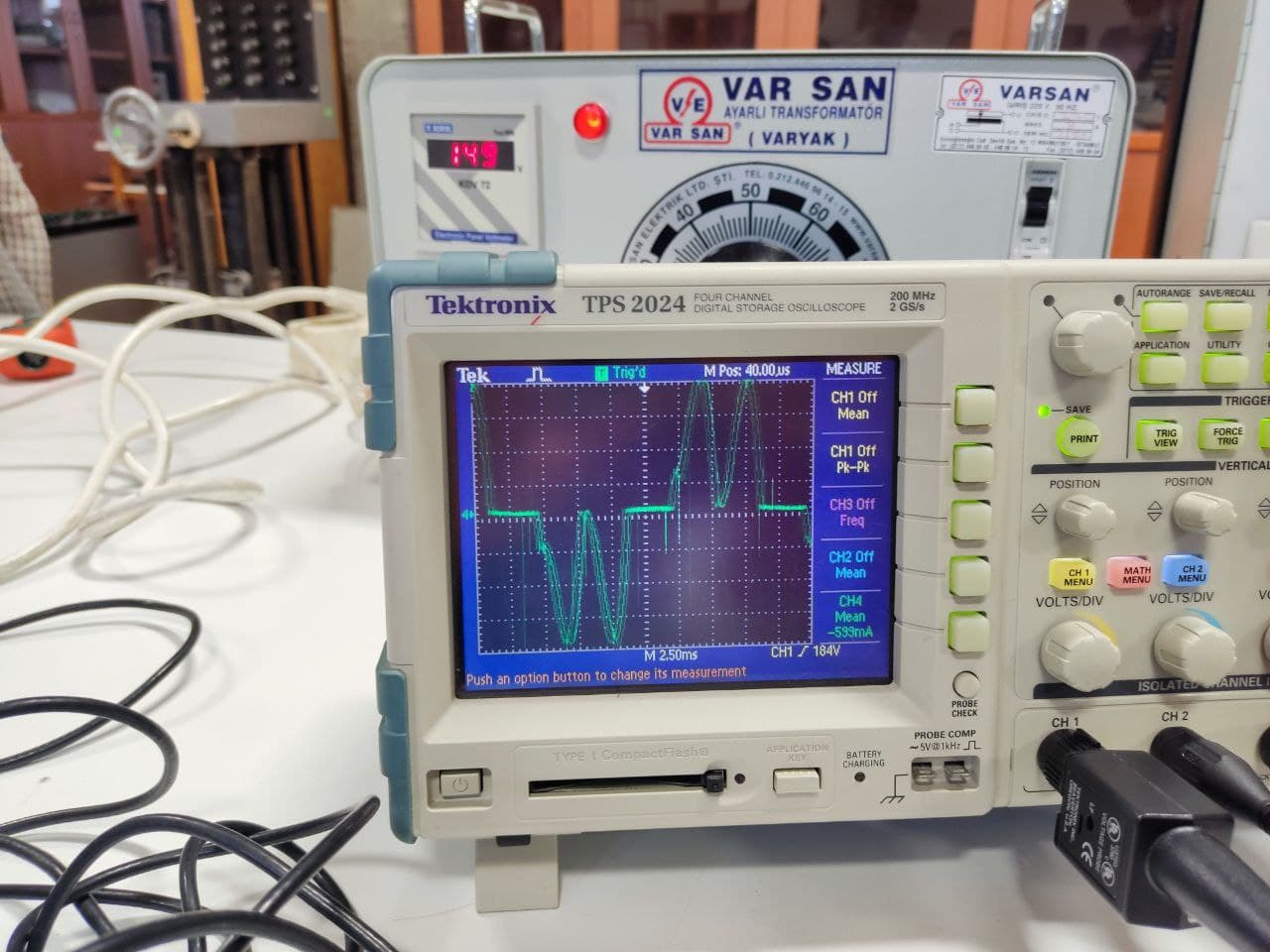


Figure 20:Output current of the kettle test

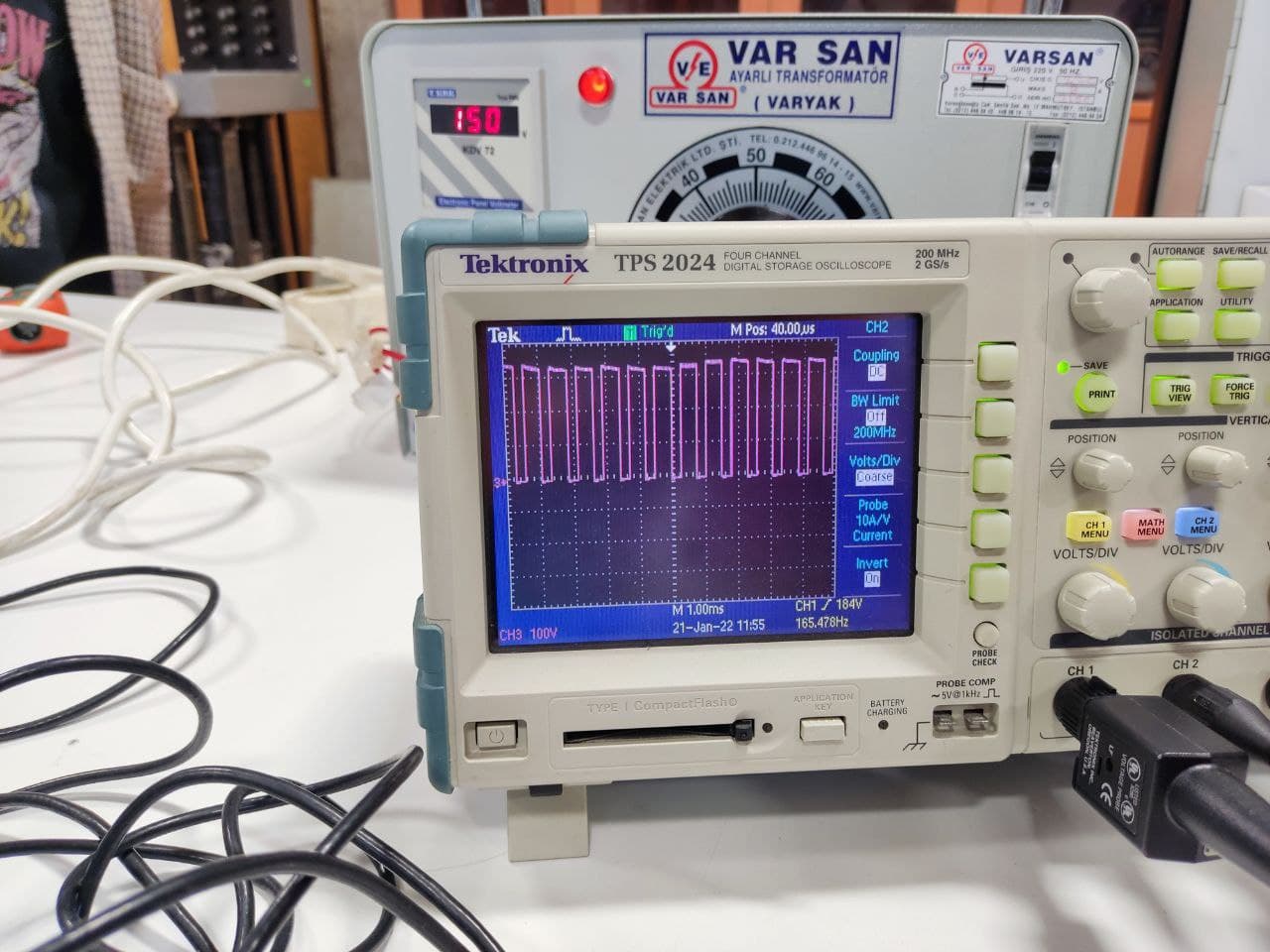


Figure 21:Output voltage of the kettle test

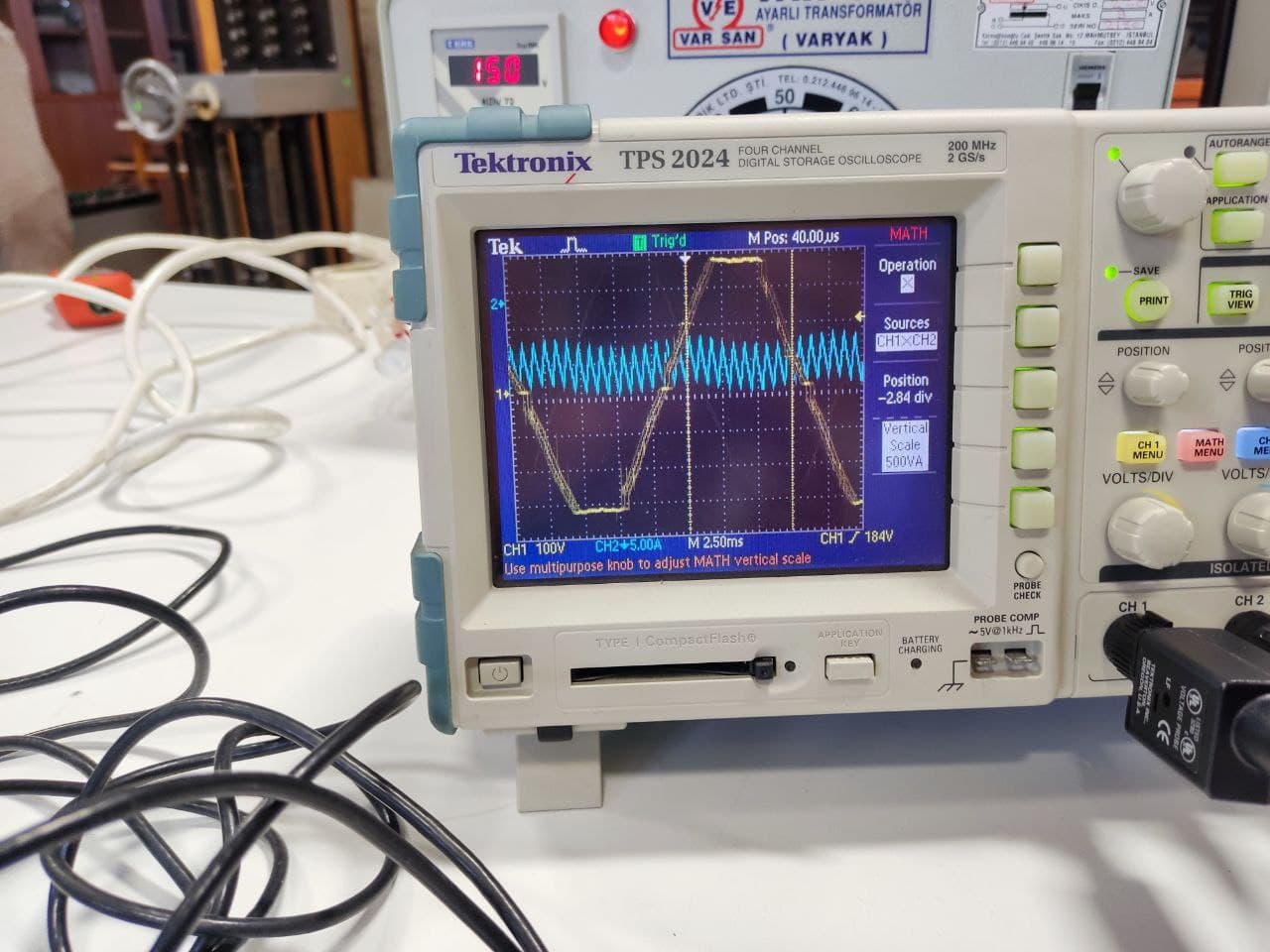


Figure 22:Input voltage and current of the kettle test in the same graph

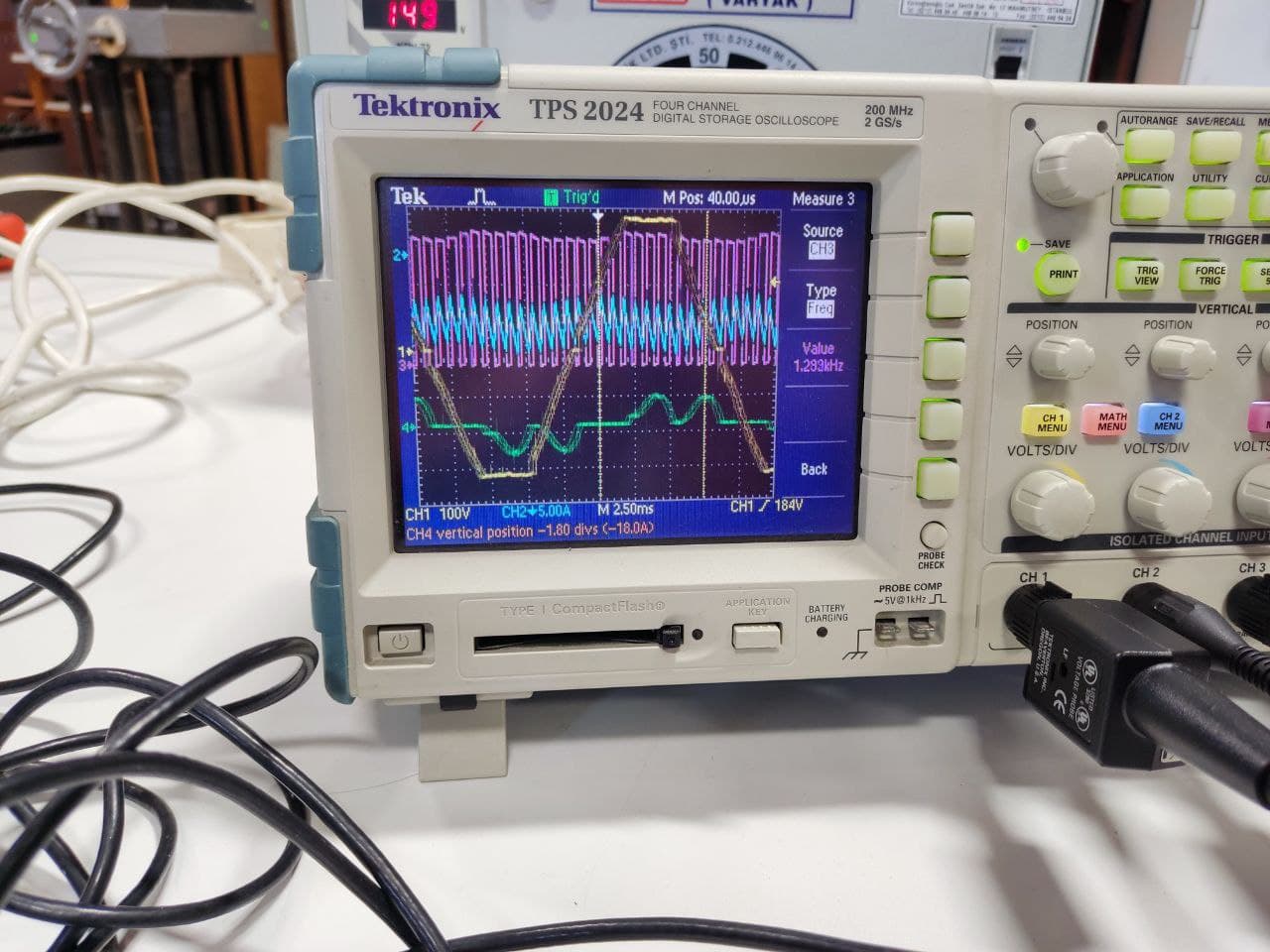


Figure 23:All the signals in the same graph



Figure 24:Current of the generator

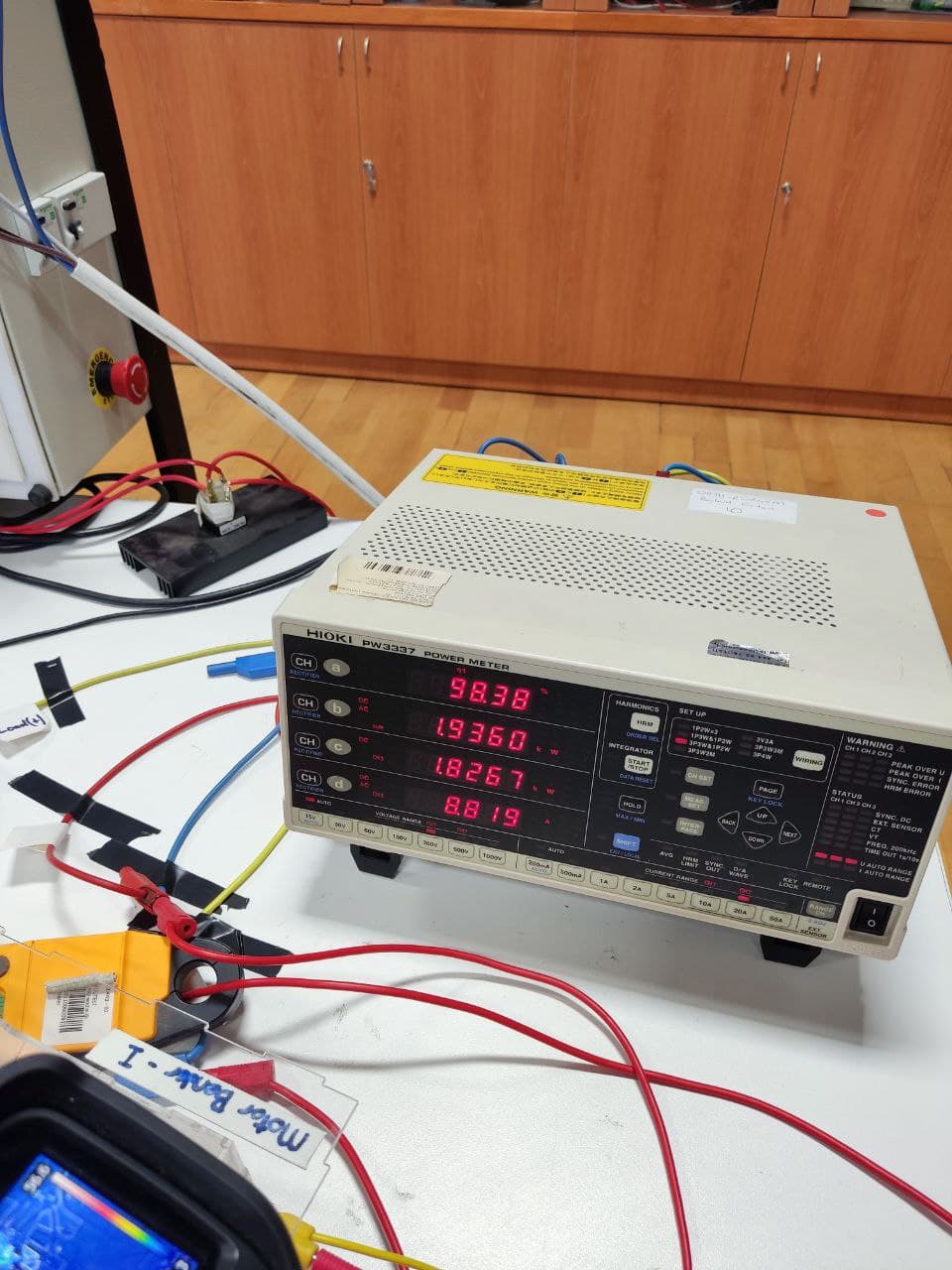


Figure 25:Power meter results for the kettle test

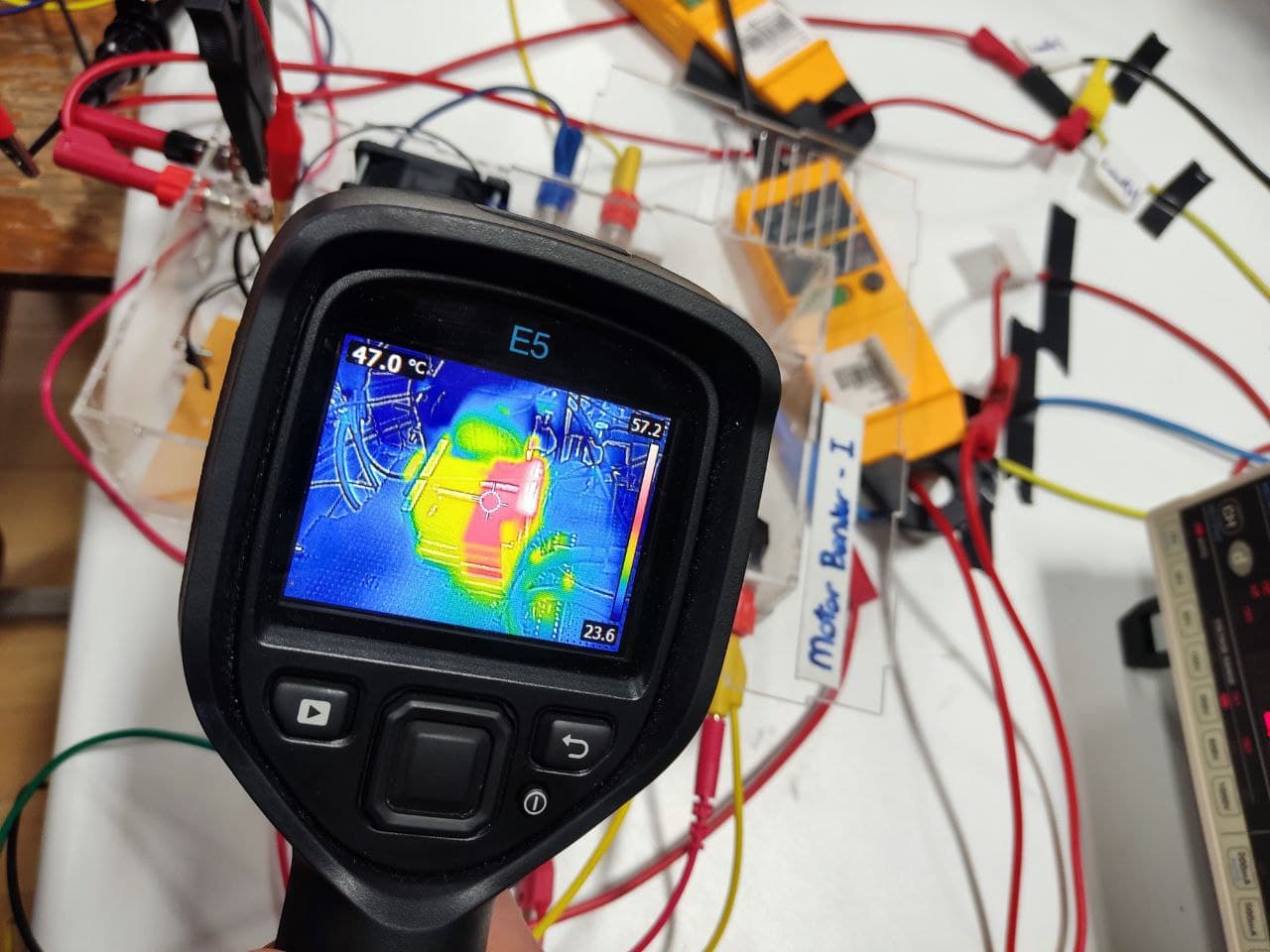


Figure 26:Temperture of the IGBT for the kettle test

**VIII. CONCLUSION**

In this report, our implementations, calculations and simulation results are given up to this point. Our main focus afterwards, is the gate driving circuitry as mentioned. Once we manage to generate the expected PWM waveform via that circuitry, we can say that the project is done.

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