MIDDLE EAST TECHNICAL UNIVERSITY

ELECTRICAL & ELECTRONICS ENGINEERING

EE464 – STATIC POWER CONVERSION 2

TERM PROJECT – SIMULATION REPORT

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Introduction

In this project, the design of isolating converter is investigated. Firstly, the topology selection is done by checking the desired ratings. Then, the component selection is explained for switch and diodes. The magnetic design of the transformer is described deeply based on the determined properties. The controller selection is done after this because the project requires closed-loop, isolated controlling. In the end, the simulation is done by LTSpice with calculated features and selected components.

Topology Selection

We are asked to design an isolated DC/DC converter fulfilling the following specifications:

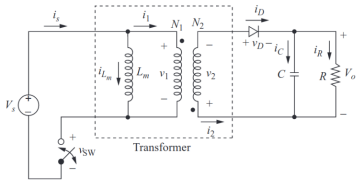
$V_{in,min}$	24V
$V_{in,max}$	48V
V_o	15V
P_o	45W
$\frac{\Delta V_o}{V_o}$	3%
Line regulation	3%
Load regulation	3%

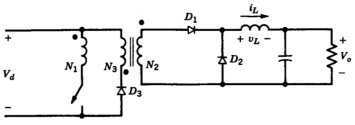
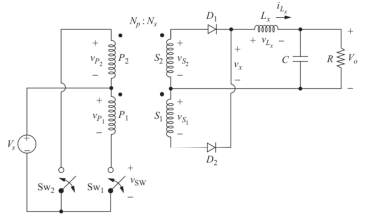
Table 1. Project specifications.

Five topologies come to mind:

- ❖ Flyback converter
- ❖ Forward converter
- ❖ Push-pull converter
- ❖ Full bridge converter
- ❖ Half-bridge converter

Accordingly, we can compare them according to their strengths and weaknesses.

	Advantages	Disadvantages
Flyback converter $\frac{V_o}{V_{in}} = \frac{N_2}{N_1}\frac{D}{1-D}$ 	☐ Single switch. ☐ No additional inductor. ☐ No center-tapped windings. (a smaller core can be used) ☐ No cap on the duty cycle. (not strictly less than 0.5 as in the below topologies) ☐ Albeit inefficient, an RCD snubber can easily be used to limit $\frac{di}{dt}$ losses in cases where power cannot be sent back to the input.	☐ Need to watch out for MOSFET ratings. ☐ Non-linear D dependence in the voltage transfer function. ☐ Cannot use a Kool MU toroid due to increased leakage inductance when wound.

Forward converter $\frac{V_o}{V_{in}} = D\frac{N_2}{N_1}$ 	☐ Linear D dependence. ☐ Output current waveform enhanced with the presence of an output inductor. ☐ No center-tapped windings. ☐ The magnetic return path for magnetizing inductor current.	☐ Need to watch out for MOSFET ratings. ☐ More challenging in terms of magnetic design with the second inductor. ☐ Additional core losses and copper losses due to the inductor. Note that the output inductor's core losses will happen at twice the frequency. ☐ Fill factor challenge if a third winding is employed. ☐ Two switch forward converter would have to be used in the absence of a third winding, which could lead to increased switching losses. ☐ Duty cycle capped at: $\frac{1}{1+\frac{N_3}{N_1}}$
Push-pull converter $\frac{V_o}{V_{in}} = 2D\frac{N_2}{N_1}$ 	☐ A better utilization of the core with operation in the 3rd quadrant. ☐ A smaller variation in D can help achieve the desired output voltage with twice the gain compared to a forward converter. ☐ Linear D dependence. ☐ Output current waveform enhanced with the presence of an output inductor. ☐ No center-tapped windings.	☐ Two switches will have to be controlled with a phase shift of half a period. More difficult control. Deadtime adjustment may be required. ☐ Center tapped transformer (at both primary and secondary) will challenge the fill factor, Larger core is required. ☐ Difficult to come up with a counteracting measure to limit $\frac{di}{dt}$ losses at the input side, with twice the number of primary terminals. ☐ More components. (more diodes, an inductor, longer wire lengths for the transformer). ☐ Increased core losses due to the third quadrant. ☐ Inductors' core losses will happen at twice the frequency of operation.

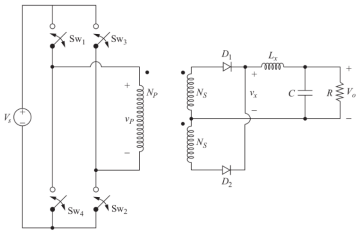
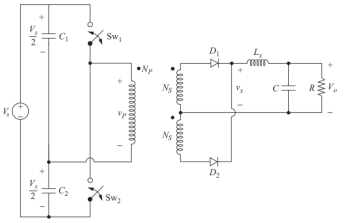
		☐ Duty capped at 0.5.
Full bridge converter $\frac{V_o}{V_{in}} = 2D\frac{N_2}{N_1}$ 	Same as a push-pull converter, but also: ☐ Fill factor challenge eased compared to a push-pull converter since there is a single primary.	Same as a push-pull converter, but also: ☐ Four switches at the primary. No added difficulty in terms of control, but switching losses will increase.
Half-bridge converter $\frac{V_o}{V_{in}} = D\frac{N_2}{N_1}$ 	Same as a full-bridge converter.	Same as a push-pull converter, but also: ☐ Practically, capacitance values may not be the same. Then, the voltage division over the two capacitors will not be identical.

Table 2. Topology comparison.

On the whole, in terms of implementation convenience, the flyback converter seems to be more advantageous compared to the remaining topologies. Two distinct control signals to be sent to switches renders implementation difficult, and a compulsory third winding (inherently existing in the topology – not part of the control circuit) or a center tap renders fill factor more challenging. A flyback converter is free of such problems, making it our design decision.

Magnetic Design

Before starting with magnetic design, it is needed to identify the maximum, average and RMS values of the magnetizing inductance in order to design a suitable transformer. At first, it is already known that average value of the magnetizing inductance can be calculated as

$$I_{m,avg} = \frac{I_{in,avg}}{D} = \frac{P_{out}}{V_{in}D}$$

Assuming the turns ratio being equal to 1 for simplicity,

$$D = \frac{V_o}{V_{in}+V_o}$$

This equation yields a duty cycle of 0.385 when the input is 24 V, and 0.238 for 48 V input. Then, average magnetizing inductance current becomes 4.875 A for 24 V input case and 3.938 A for 48 V input case.

$$\Delta i_m = \frac{V_{in}DT_s}{L_m}$$

It should be noted that the switching frequency will be 100 kHz because several current mode analog controllers are operating at that frequency. Since we are aiming to operate in CCM, $I_{m,avg} \geq \Delta i_m/2$, which results in a minimum inductance requirement of 20.32 µH, for the input case of 48 V. Note that magnetizing inductance requirement is higher in higher input voltage because the ripple current is higher in that case. Thus, if the inductor is designed for this case, it can be guaranteed that at low input voltages converter will also operate in CCM. Moreover, to ensure the CCM operation a safety factor of 1.5 is chosen for the minimum inductance value, i.e., the minimum magnetizing inductance requirement is considered as approximately 30 µH.

It comes to magnetic components and wire selection. At first, a MATLAB script is created for magnetic design with EE cores for their easiness of winding. However, there should be an airgap placed inside the ferrite cores in order to limit the magnetic flux density inside the core for not saturating the core and increasing core losses. Afterward, data of the cores are inserted into the script to select a suitable core. Then, the following design procedure is applied to all the ferrite EE cores.

$$\frac{N_{pri}^{\ 2}}{R} = L_m$$

$$\frac{N_{pri}}{R} = \frac{B_{core} A_{core}}{I_{max}}, \text{ where } I_{max} = I_{m,avg} + \Delta i_m/2$$

Rearranging the above equations give

$$N_{pri} = \frac{L_m I_{max}}{B_{core} A_{core}}$$

After this point, it is required to choose a core. From the MATLAB script, possible candidates are identified by utilizing the area product formula with a fill factor of 0.3 and the 0P44022EC core is chosen, which has an effective area of 233 mm2 and an effective length of 67 mm. The core material is specified as P material on the Magnetics website, which has 2500 relative permeability. Then, solving the above equation for worst-case conditions and magnetic field intensity of 0.1 T yields a turn number of 12 and a magnetizing inductance of 60 μH on the primary side so is the secondary side. Afterward, it is required to calculate the airgap length. To calculate the airgap length,

$$R = \frac{N_{pri} I_{max}}{B_{core} A_{core}} = \frac{l_e}{\mu_0 \mu_r A_e} + \frac{2g}{\mu_0 A_e}$$

which yields

$$g = \mu_0 \frac{N_{pri} I_{max}}{2B_{core}} - \frac{l_e}{2\mu_r} \approx 0.4\, mm$$

After all, calculating the magnetic flux density throughout the core for double check will give the accuracy of the design. If we calculate the magnetic flux density by utilizing the magnetic circuit, it is seen that the magnetic flux density is 0.11 T. Thus, we are done with the magnetic design. Let's select the number of parallel branches at the primary and secondary sides.

RMS of a pulsating current can be calculated as $\sqrt{D} I_{peak}$. The RMS current is calculated via the MATLAB script and it is seen that 3.8 A RMS of current should be maintained on the primary side and 5.7 A RMS current should be transmitted on the secondary side. Taking the current density being between 3 - 4 A/mm^2 yields a number of parallel conductors of at least 7 and 9 at the primary and secondary sides, respectively. So, they are chosen as 8 and 10 for being safe.

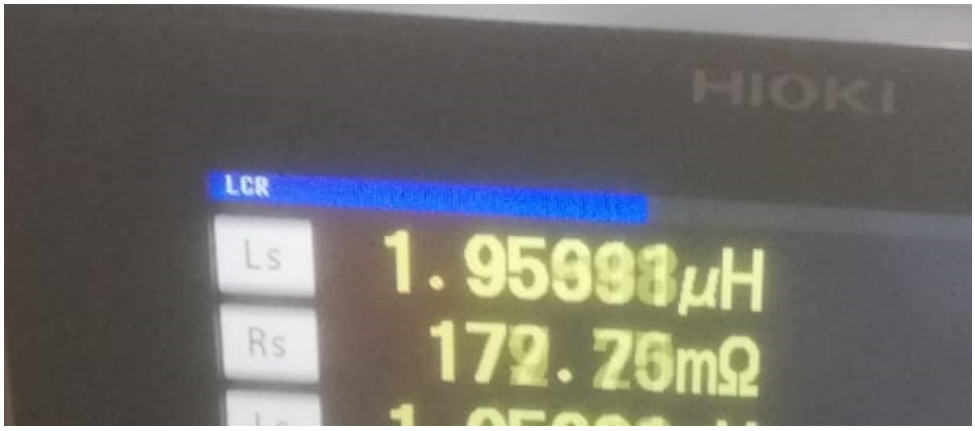


Figure 1. Leakage inductance measurement.

Figure 2. Magnetizing inductance measurement.

Controller Selection

In this part, the selection of the controller will be explained.

Firstly, the input, output voltage, and power ratings are noted for a proper controller. Then, using this rating, the search for the controller is done on the analog devices website. Also, another desired feature is being a no-Opto controller for us to make the implementation easier. Results can be seen in figure 3.

☐	LT8316	1	16	600	100	Buck, Flyback, No-Opto Flyback
☐	LT3748	1	5	100	80	Flyback, No-Opto Flyback
☐	LT3825	1	14	75	80	Flyback, No-Opto Flyback

Figure 3. Searching results on Analog Devices.

The LT8316 and LT3825 have extra windings and too complicated example circuits. Hence, LT3748 had been chosen. However, when the datasheet is deeply investigated, we saw that the controller is working on critical conduction mode. The selection was canceled because this would cause a problem for the magnetic design.
The searching continued on the Texas Instruments website. Again, the rating-based research was done. Then, UC3845 was found. Also, the frequency is arrangeable which is a good feature. The only negative feature is a third winding is needed for an isolating control.

The switching frequency is chosen as 60kHz for magnetic design, this value is also proper for this controller. Moreover, the controller is working in continuous conduction mode. However, the spice model is not working properly on the LTSpice. After this, we saw that the LT1241 is working the same way on the simulation. Hence, we used the LT1241 in our simulations. Also, we discussed the change UC3845 for LT1241, however, the provision of the LT would not be easy in Turkey.

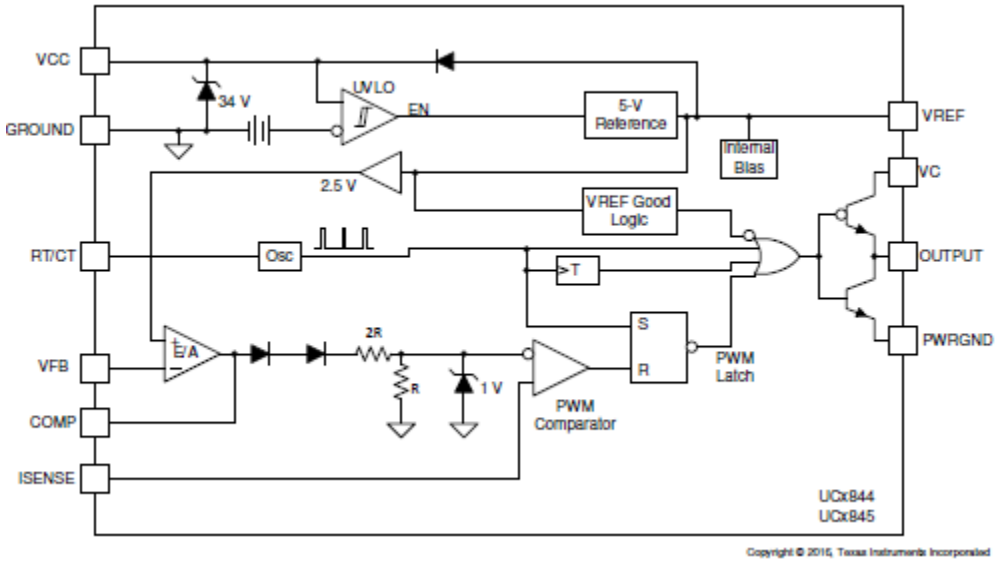


Figure 4. Functional Block Diagram of UC3845.

Losses

Core Losses

To calculate the core losses, material core loss density graph provided by the manufacturer can be utilized, which can be seen below.

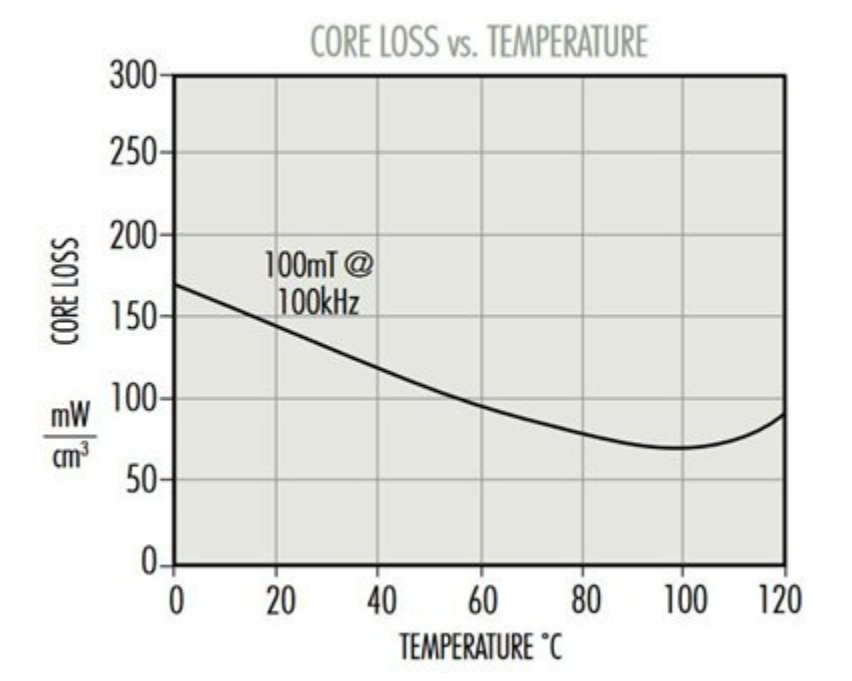


Figure 5. Core loss graph of our core.

It is seen that as the temperature of the core increases, core loss decreases. Calculating for the worst case of room temperature will roughly give a loss density of 140 mW/cm^3. The volume of the core is 22.7 cm^3. Hence, this will yield a core loss of 3.178 W for the worst conditions. When the core reaches a temperature of 60 or 80 ℃, the core loss becomes 2.27 W.

Copper Losses

Since the cable is chosen according to the frequency (diameter is 0.425 mm), there will be a negligible skin effect, i.e., the DC resistance will be equal to the AC resistance. Moreover, the number of parallel cables will decrease the equivalent resistance of the cables. Equivalent resistance can be calculated as

$$R = \rho\frac{l}{A_{cu}}$$

ρ is the resistivity of the copper, which is 1.68×10-8 Ω.m. Length can be calculated by using the MLT, however, MLT is not specified in the datasheet. Taking the average of the possible largest turn length and smallest turn length will give an MLT of 81.7 mm. The single copper area is calculated from the diameter as 0.14 mm^2 . Then,

$$R_{pri,DC} = \frac{\rho l}{8A_{cu}} = 14.7\ m\Omega \approx R_{pri,AC}$$

$$R_{sec,DC} = \frac{\rho l}{10A_{cu}} = 11.7\ m\Omega \approx R_{sec,AC}$$

Calculating the losses at the primary and secondary sides by the formula $I^2_{rms}R$, yields a total copper loss of 0.59 W.

Simulations

Open-Loop Simulation

Prior to a closed loop simulation, an open-loop simulation was conducted at V_{in} = 24V, 36V, and at 48V. Normally, a simulation of the circuit at the limits should suffice, but we wanted to depict that the circuit should still comply with the ripple condition at intermediate points. Since our turns ratio is “1” and our input voltage is always larger than the output voltage (at 15V), we will be operating the converter as if it were a buck-boost converter with buck operation. As the duty cycle decreases (when V_{in} approaches from 24V to 48V) we expect that MOSFET losses should decrease and diode losses should increase,

We will be using the open loop characteristics as a way to select the components that do not have to do with the controllers, but inherently exist in the circuit. Since our magnetic design has been done already, this implies the diode and MOSFET selection.

No efficiency calculations will be done for the open loop characteristics as we do not include any countermeasures for the practically existing MOSFET ringings with the sudden deactivation of the switch (that is, no snubber is included for the open loop simulations). In addition, with the addition of our controller, we expect that losses should increase. The efficiencies in Simulink are expected to depict a better estimate than the real efficiency, anticipated to be around 80%.

For the open loop simulations, only the effect of the magnetizing inductance will be considered. The remaining secondary effects will be reserved for the closed loop simulation,

with the controller. This is due to the weaker representation power of the open loop simulations compared to the practical circuit we will be employing with a controller.

The output capacitance should be calculated to ensure that the desired ripple ratio is satisfied for all four of the limit cases:

- Input V_{in}=24V
  - High load (3A)
  - Low load (0.3A)
- Input V_{in}=48V
  - High load (3A)
  - Low load (0.3A)

We know that D can be expressed in the form below when the turns ratio is “1”:

$$D = \frac{V_o}{V_{in}+V_o}$$

When the input is at its maximum, the duty cycle is at its minimum for a fixed output voltage as can be seen in the expression. Therefore,

$$D_{max} = \frac{15V}{V_{in,min}+15V} \simeq 0.3846 \text{ and } D_{min} = \frac{15V}{V_{in,max}+15V} \simeq 0.2381$$

With the flyback converter’s output having no dependence on its input during the switch ON cycle with the reverse biased diode, the capacitor will supply the load. Assuming a constant current,

$$\Delta V_{out} = \frac{i_o DT_s}{C}$$

$$\frac{\Delta V_{out}}{V_{out}} = \frac{i_o DT_s}{CV_{out}} < 0.03 \Rightarrow C > \frac{i_o DT_s}{0.03V_{out}}$$

Applying the limit scenarios,

Case	C_{min}
V_{in}=24V, i_o = 3A	25.64μF
V_{in}=24V, i_o = 0.3A	2.564μF
V_{in}=48V, i_o = 3A	15.87μF
V_{in}=48V, i_o = 0.3A	1.587μF

Table 3. Output capacitance values for load and input combinations.

Of course, low load configurations should not exert a limiting constraint since the higher load is expected to do so. However, for the sake of visualization, they were included as well.

To be on the safe side, we can choose C_{out}=47μF, about twice the limit for the V_{in}=24V, i_o = 3A configuration.

For V_{in} =24V, D = 0.3846:

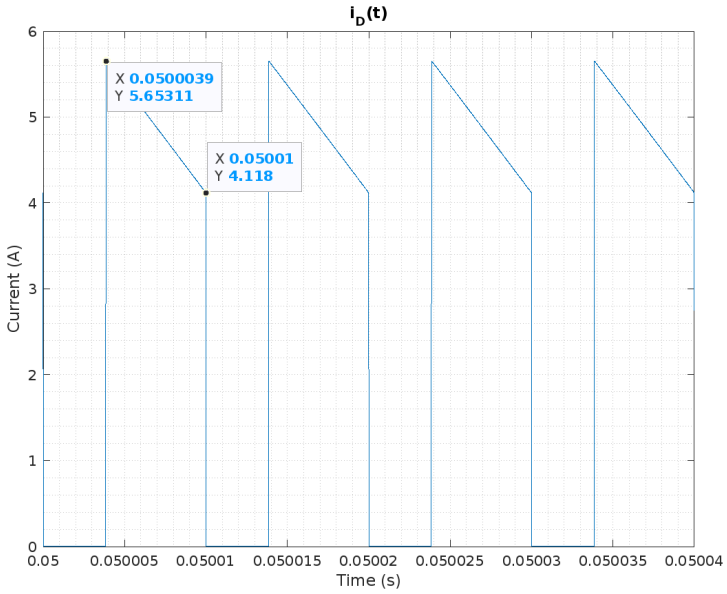


Figure 6. Diode current for V_{in} =24V.

The average diode current is 3.007A.

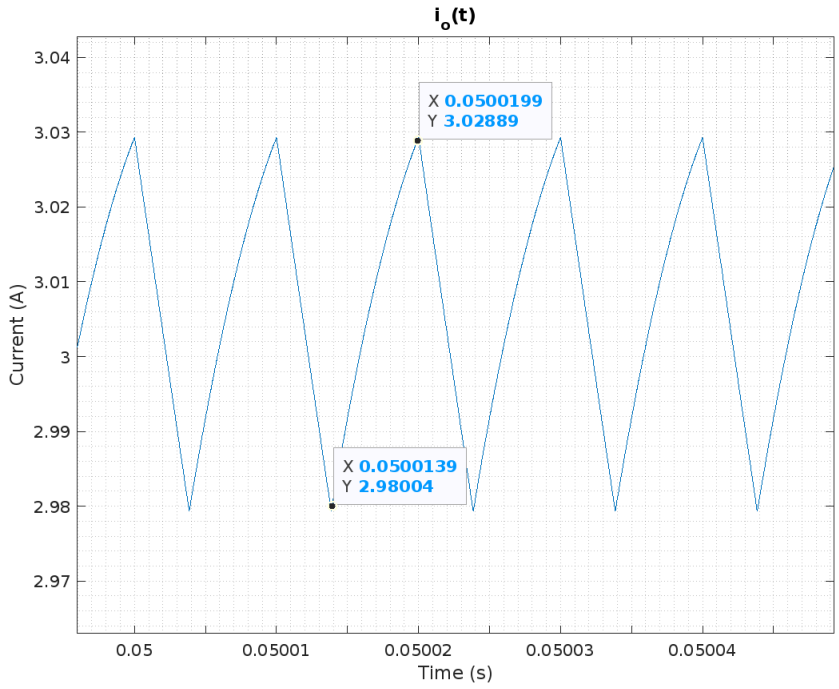


Figure 7. Output current for V_{in} =24V.

The average output current is 3.006A.

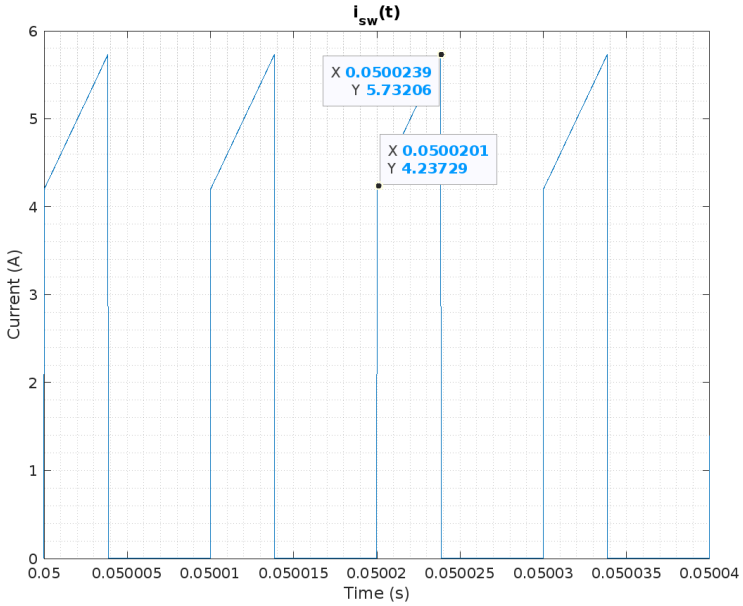


Figure 8. MOSFET current for V_{in} =24V.

The average MOSFET current is 1.915A.

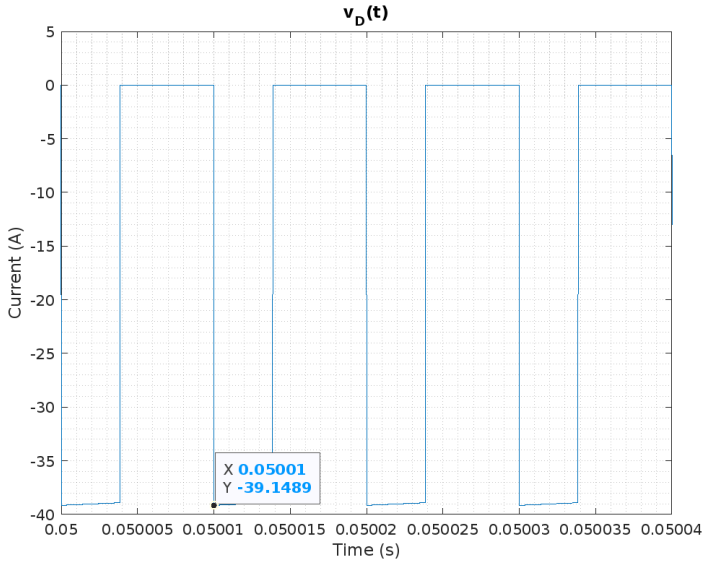


Figure 9. Diode voltage for V_{in} =24V.

The maximum blocked MOSFET voltage is 39.145V.

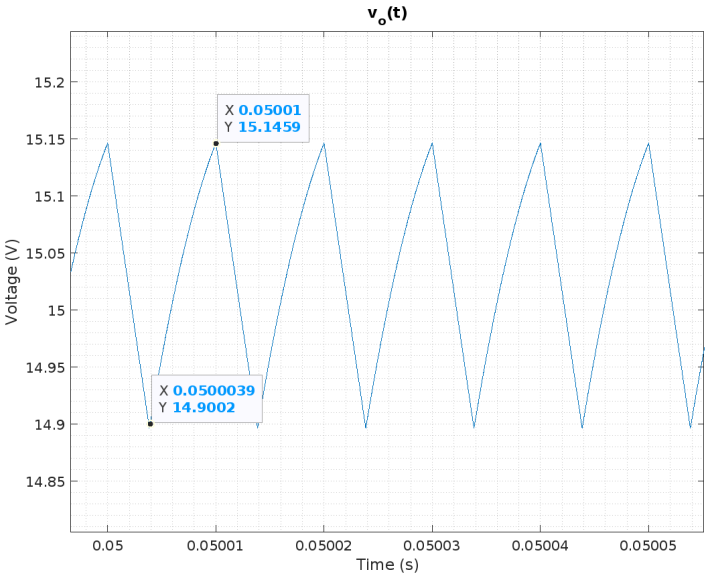


Figure 10. Output voltage for V_{in} =24V.

The average output voltage is 15.03V. With a peak-to-peak ripple of 0.2457V, $\frac{\Delta V_{out}}{V_{out}} = 0.0163 < 0.03$

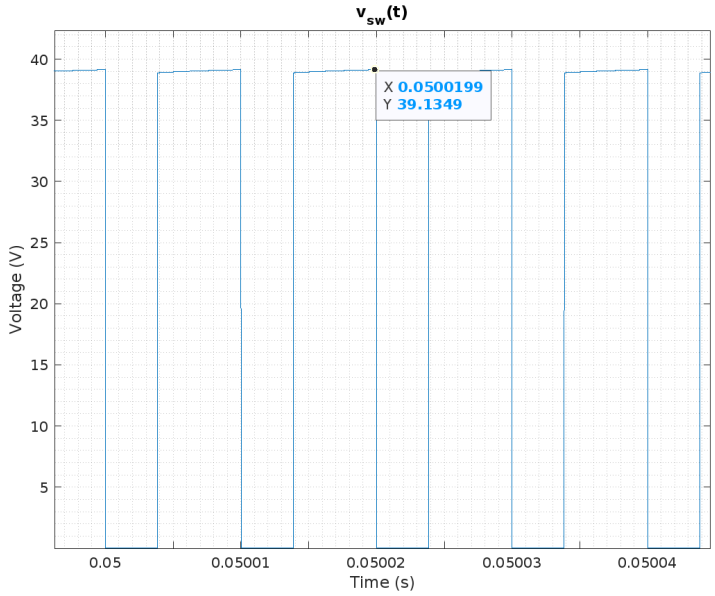


Figure 11. MOSFET voltage for V_{in} =24V.

The maximum blocked MOSFET voltage is 39.135V.

For V_{in} =36V, D = 0.2941:

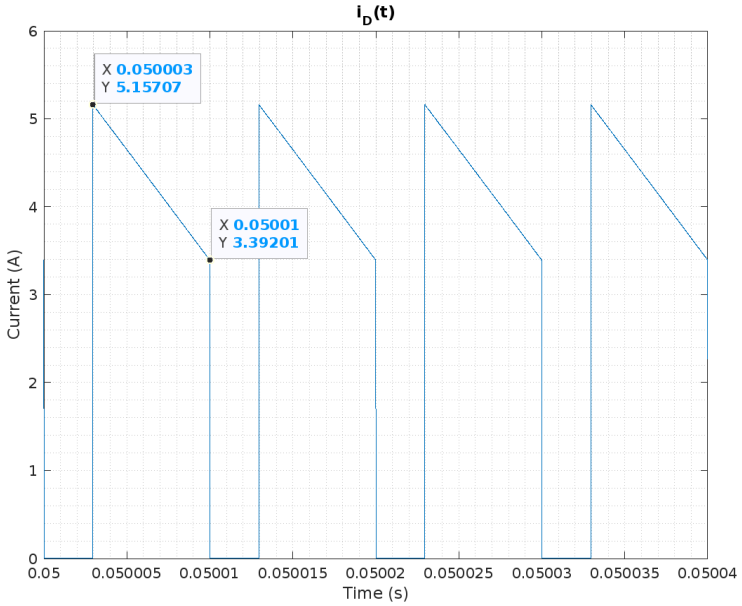


Figure 12. Diode current for V_{in} =36V.

The average output current is 3.016A.

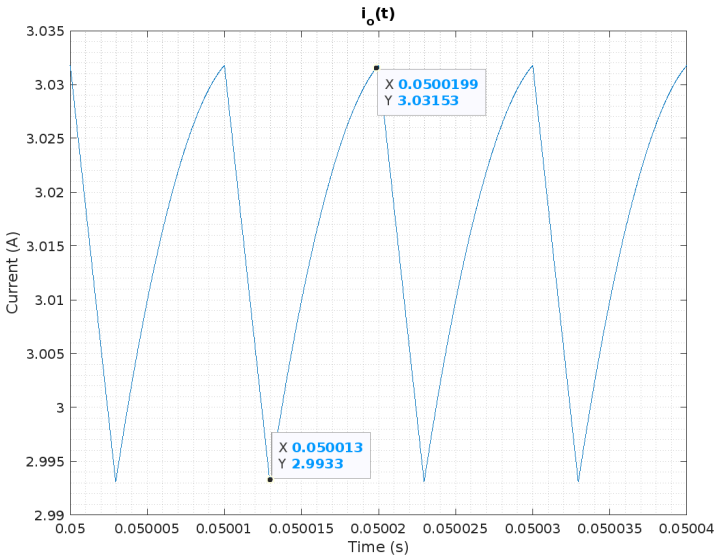


Figure 13. Output current for V_{in} =36V.

The average output current is 3.016A.

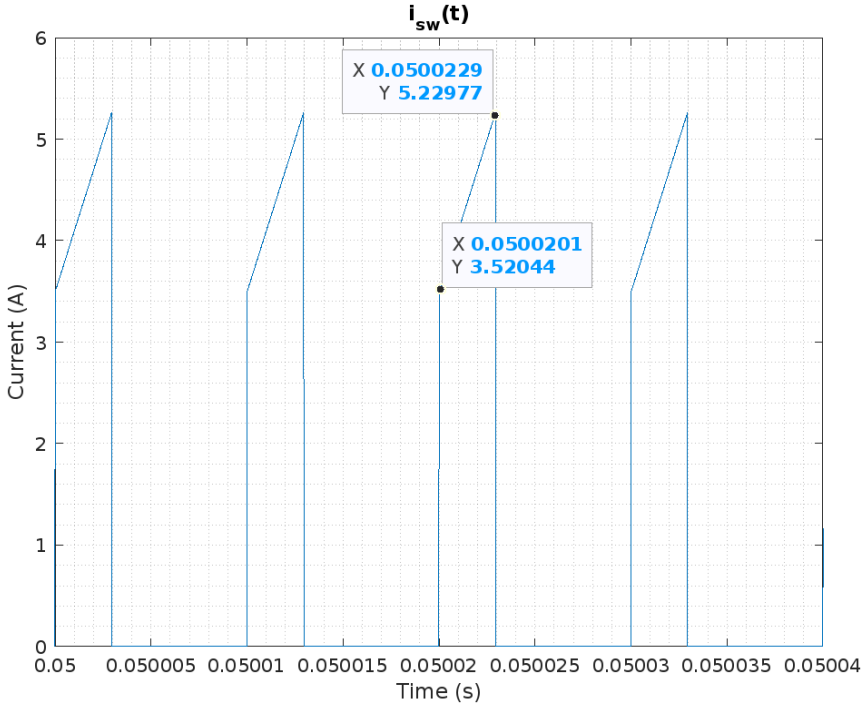


Figure 14. MOSFET current for V_{in} =36V.

The average MOSFET current is 1.292A.

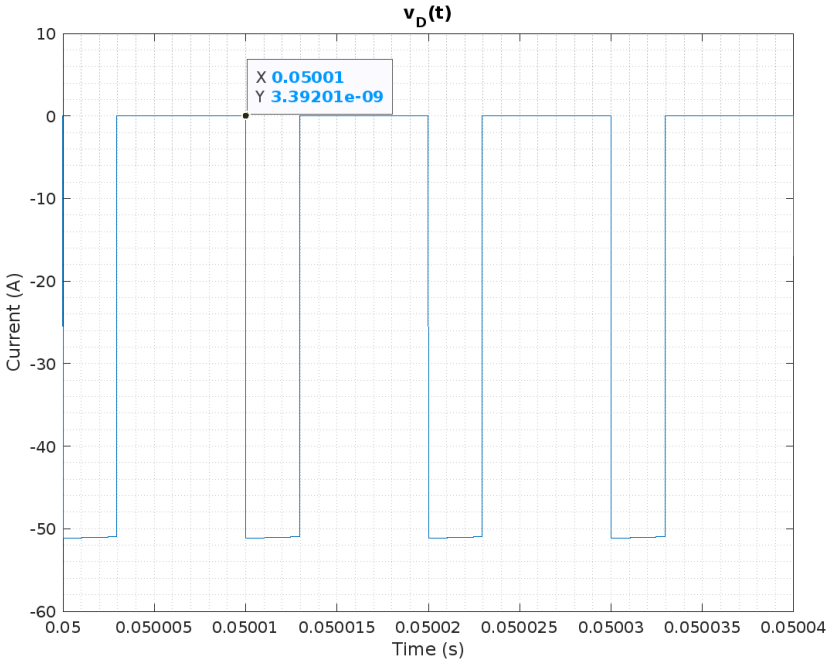


Figure 15. Diode voltage for V_{in} =36V.

The maximum blocked diode voltage is 51.15V.

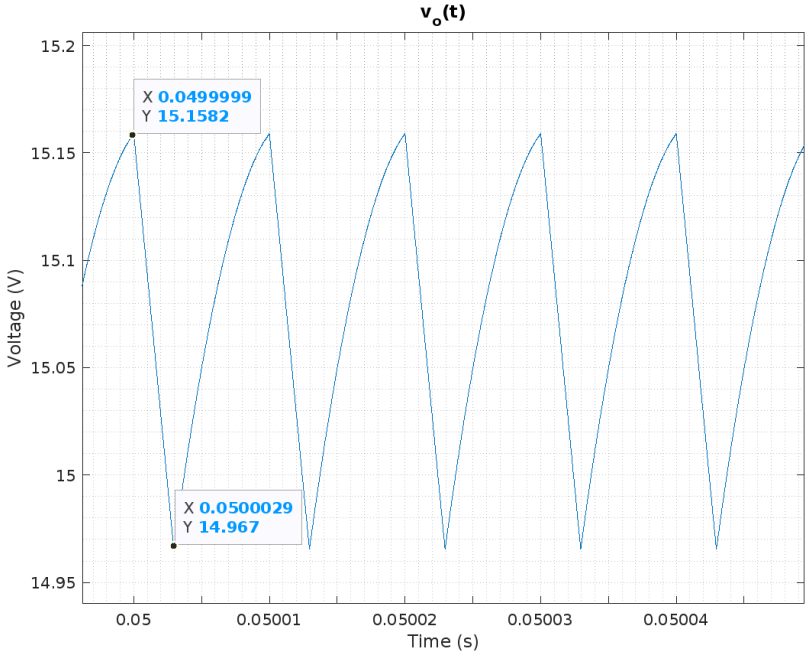


Figure 16. Output voltage for V_{in} =36V.

The average output voltage is 15.08V. With a peak-to-peak ripple of 0.1912V , $\frac{\Delta V_{out}}{V_{out}} = 0.0126 < 0.03$

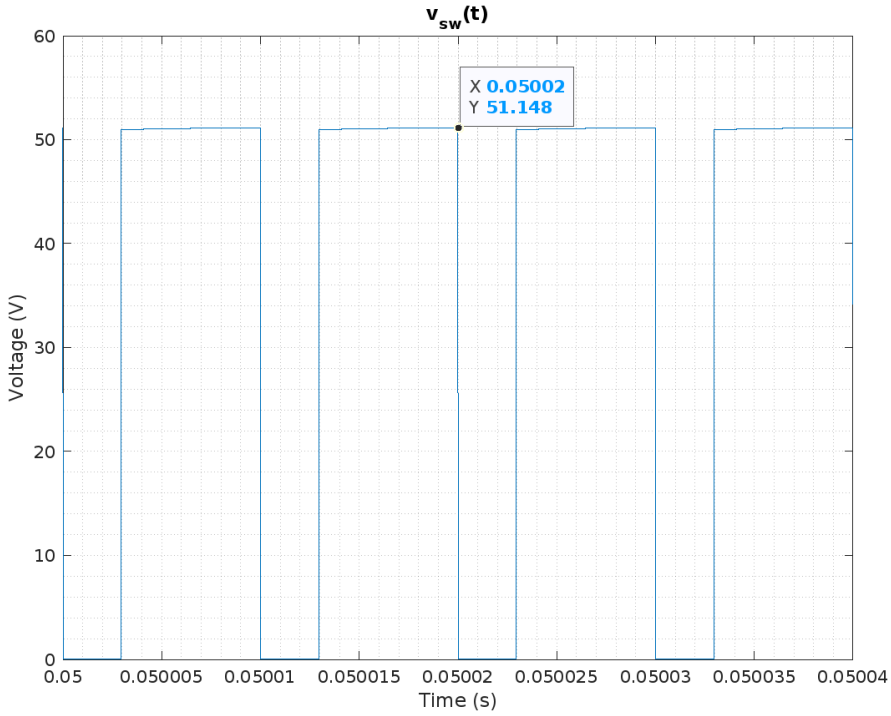


Figure 17. MOSFET voltage for V_{in} =36V.

The maximum blocked MOSFET voltage is 51.15V.

For V_{in} =48V, D=0.2381:

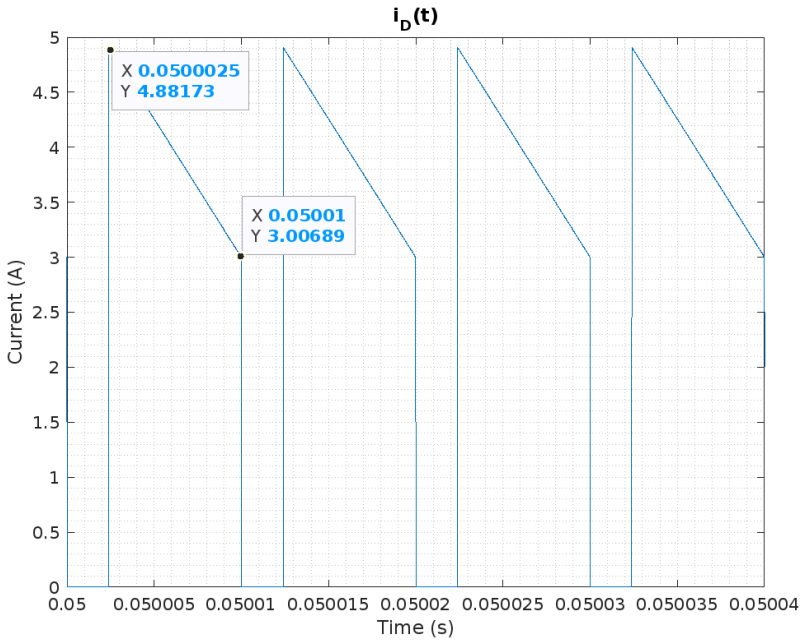


Figure 18. Diode current for V_{in} =48V.

The average diode current is 3.009A.

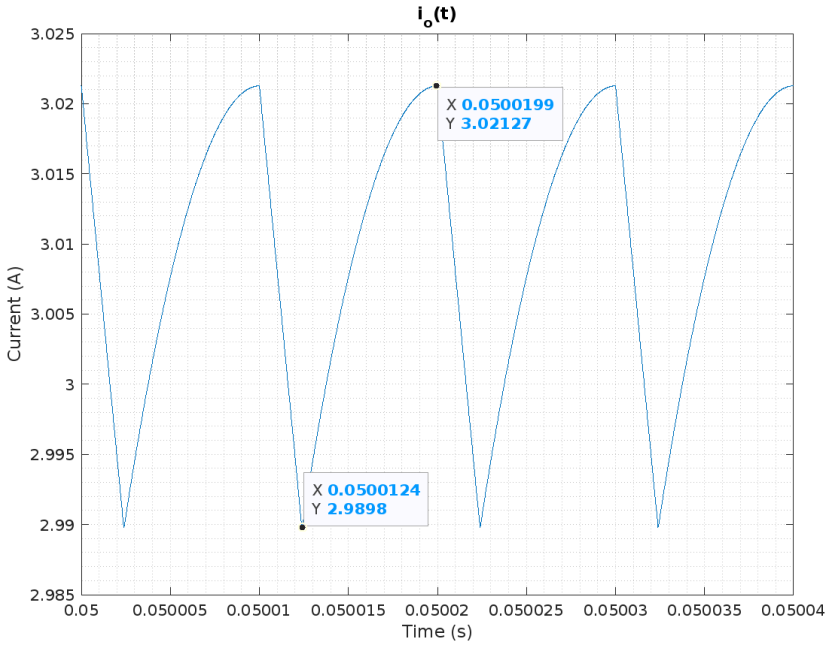


Figure 19. Output current for V_{in} =48V.

The average load current is 3.011A.

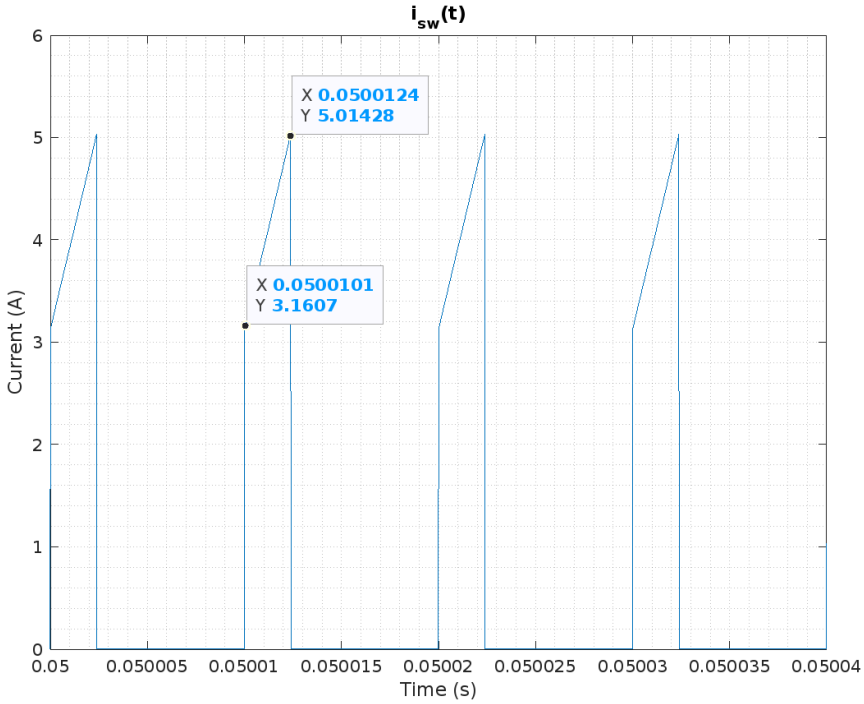


Figure 20. MOSFET current for V_{in} =48V.

The average MOSFET current is 0.975A.

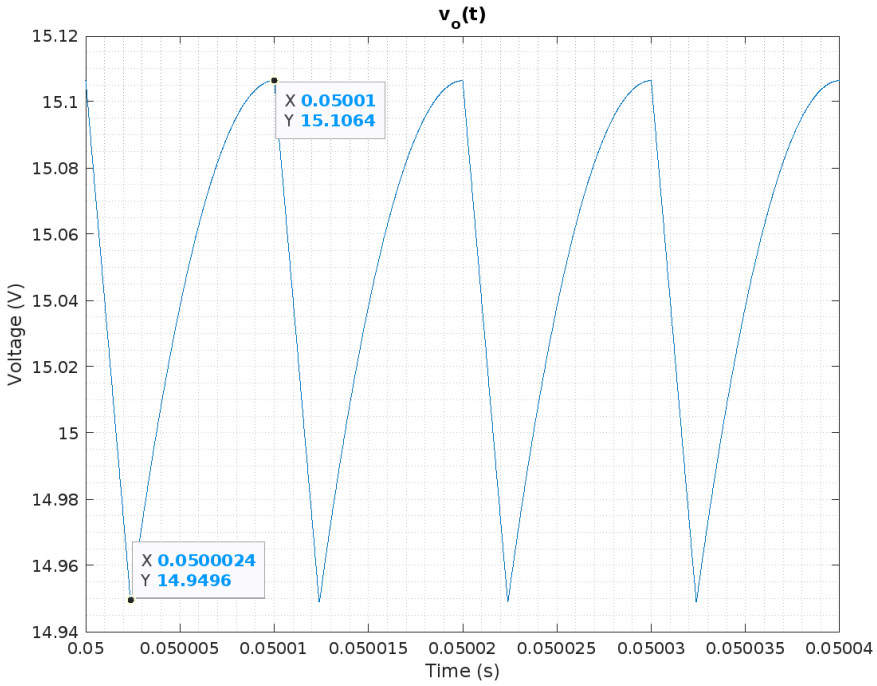


Figure 21. Output voltage for V_{in} =48V.

The average output voltage is 15.05V. The ripple is 0.1574V. Accordingly, $\frac{\Delta V_{out}}{V_{out}} = 0.0105 < 0.03$.

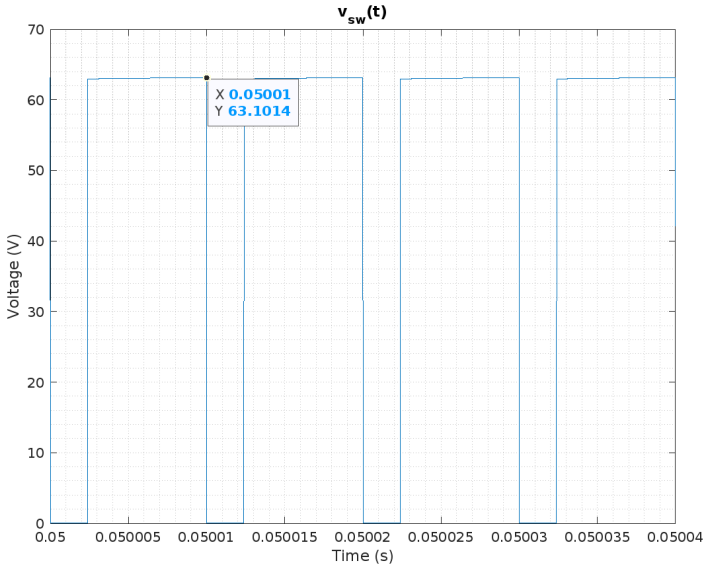


Figure 22. MOSFET voltage for V_{in} =48V.

The maximum blocked MOSFET voltage is 63V.

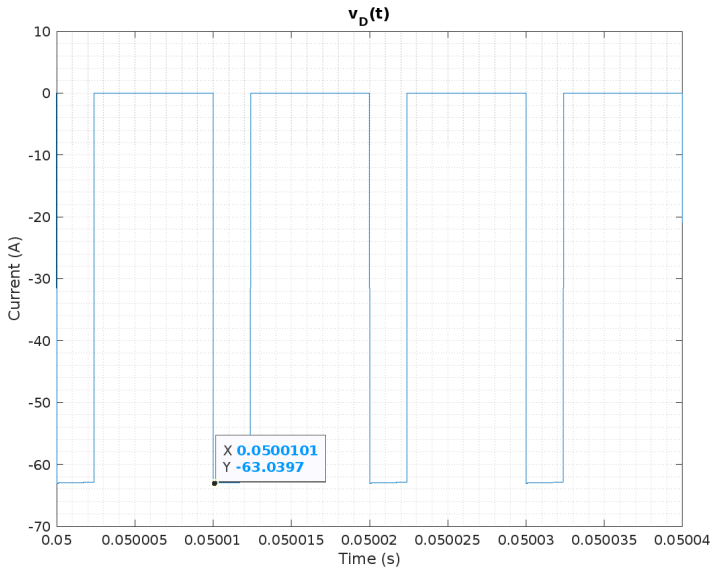


Figure 23. Diode voltage for V_{in} =48V.

The maximum blocked diode voltage is -63V.

As the load resistance and the output voltage is fixed, the diode voltage is also constrained to be fixed at 3A forward current. With a lower duty cycle at V_{in} =48V, the MOSFET and diode blocking voltages increase. A maximum of 63V is blocked.

For the MOSFET, an average current of 1.915A. Naturally, this happens when the duty cycle is at its highest: D = 0.3846. The same voltage is blocked as the diode.

While these values would have been sufficient to choose commercial products from the market, our circuit will not be operating at a fixed operating point. The inclusion of the controller might introduce secondary effects not foreseen nor covered in the scope of these simulations. Even if the practical leakage inductances and copper loss resistances of the windings are included, we do not expect that the results should change significantly.

Closed-Loop Simulation

The closed-loop simulation is based on the example circuit of the controller [1]. The resistances are changed for desired frequency, current limit, and output voltage. Also, magnetic properties are added. A snubber is also introduced as a ringing loss measure for the switch OFF cycle.

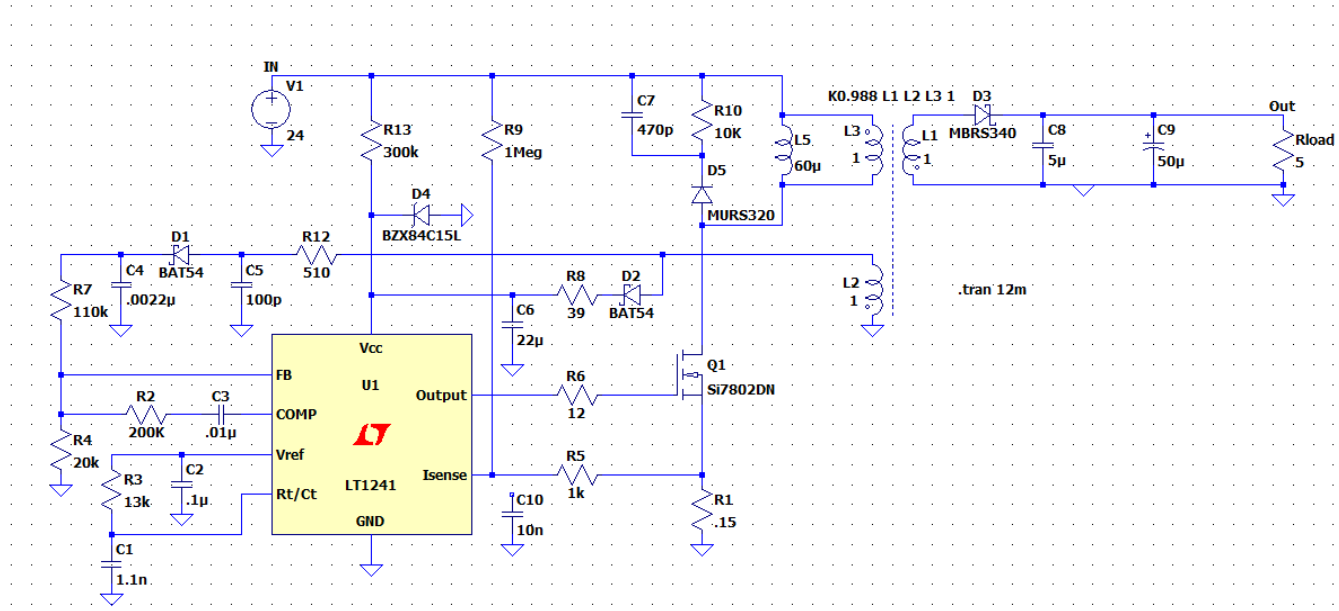


Figure 24. Schematic of the closed-loop design.

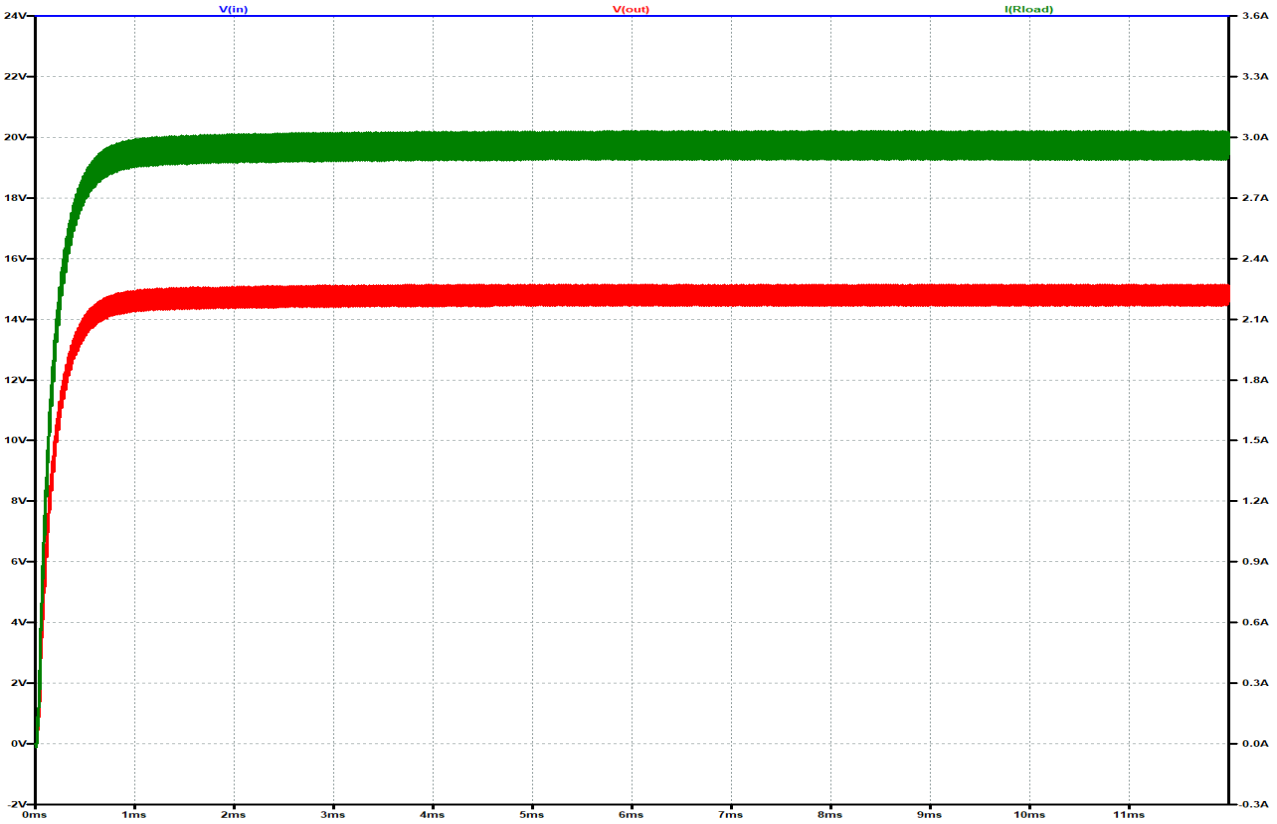


Figure 25. Input and Output Waveforms with 24V input.

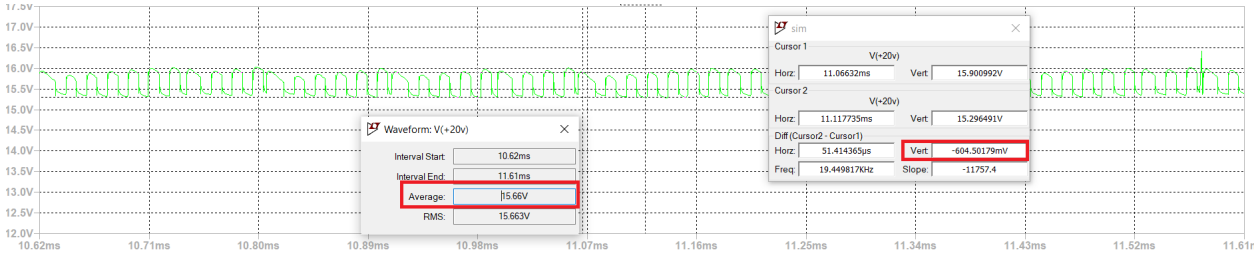


Figure 26. Output voltage ripple with 24V input.

$$\frac{\Delta V_{out}}{V_{out}} = 0.0386 > 0.03$$

The increase in ripple ratio was not something that we expected since the calculated capacitance should cover the output voltage ripple ratio to be less than 0.03. This might have to do with a low solver resolution or an unfiltered sensing at the controller. A similar case will hold for the following input voltage variations at full load.

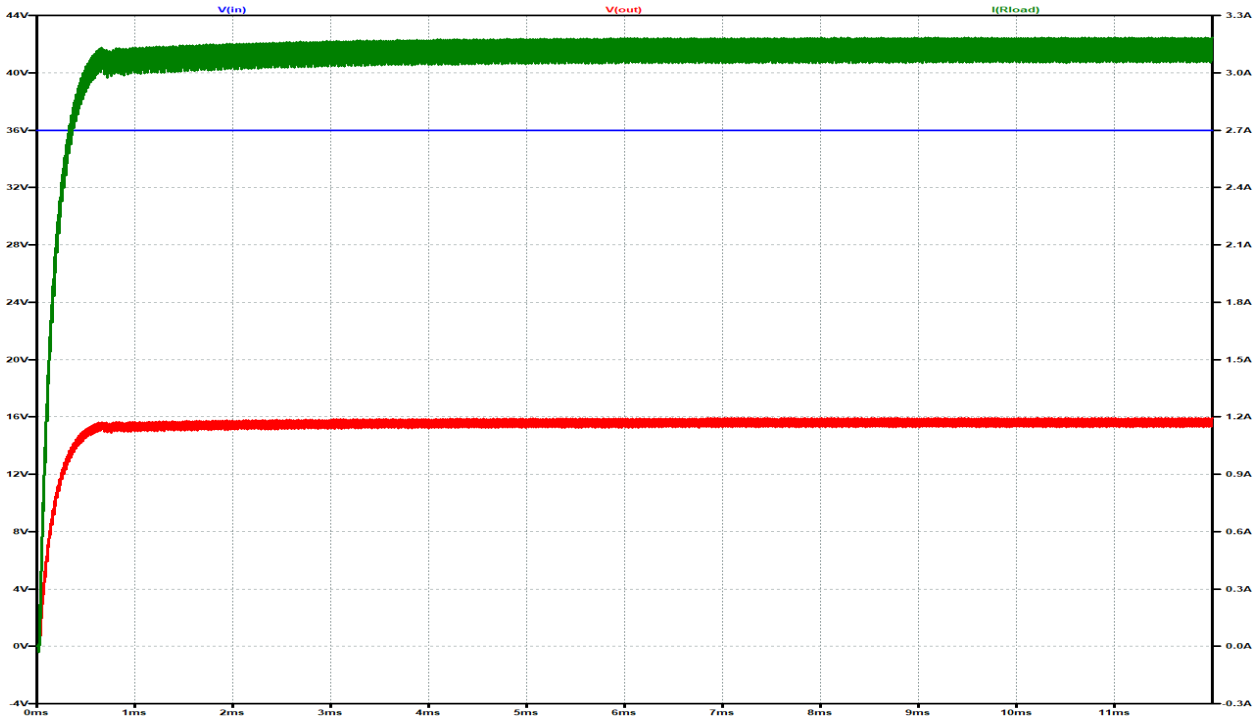


Figure 27. Input and Output Waveforms with 36V input.

Figure 28. Output voltage ripple with 36V input.

$$\frac{\Delta V_{out}}{V_{out}} = 0.0435 > 0.03$$

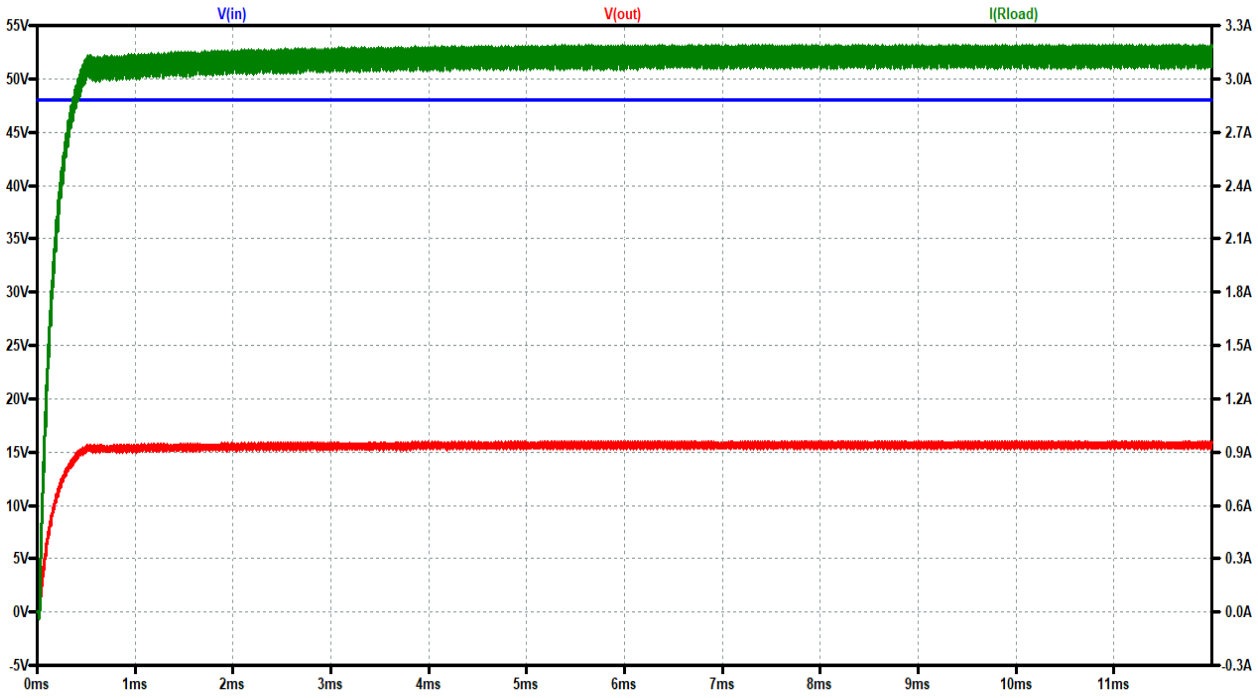


Figure 29. Input and Output Waveforms with 48V input.

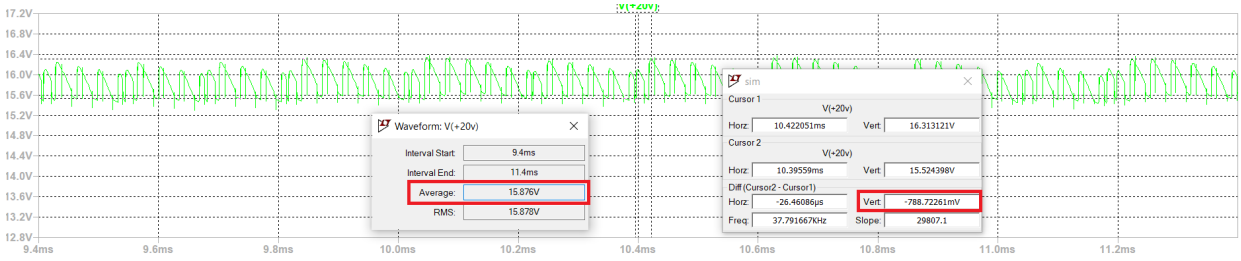


Figure 30. Output voltage ripple with 48V input.

$$\frac{\Delta V_{out}}{V_{out}} = 0.0496 > 0.03$$

Re-checking the semiconductor devices' limits (for the maximum duty case, i.e. lowest input as previously justified):

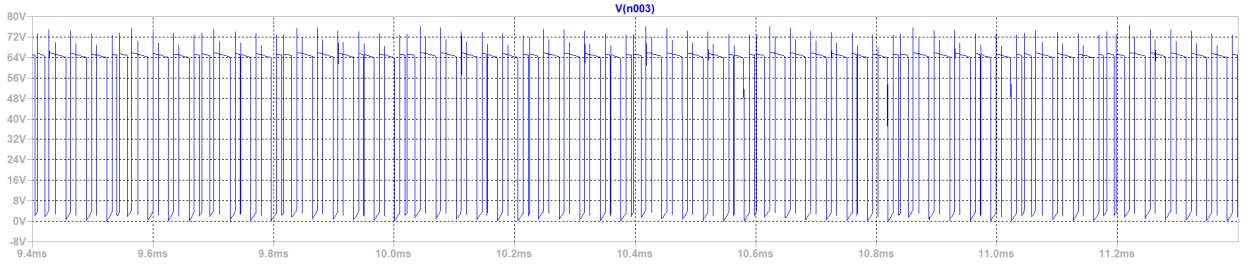


Figure 31. MOSFET voltage with 24V input.

Spikes extend up to 75V instantaneously as opposed to the expected 63V ideally. A similar case holds for the diode:

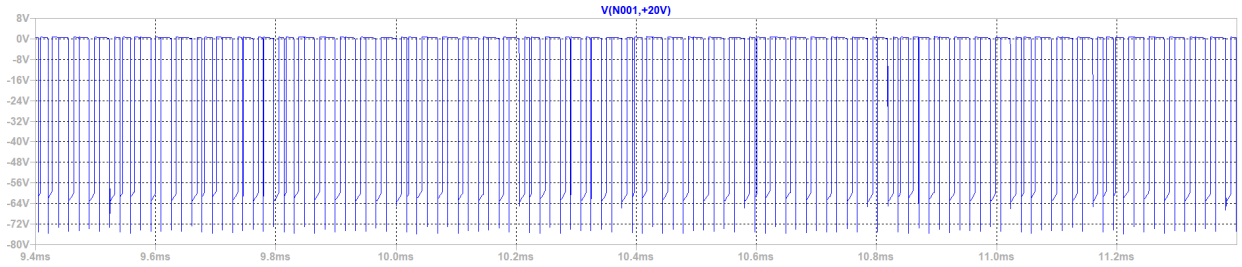


Figure 32. Diode voltage with 24V input.

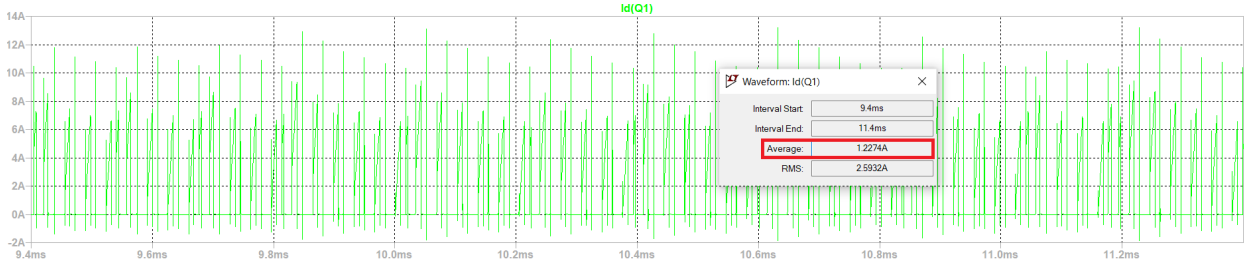


Figure 33. MOSFET current with 24V input.

We observe a decrease from the ideal simulations' 1.915A. The decrease might have to do with an excessive timestep on the simulator's end. Therefore, our MOSFET current limit will not be relaxed.

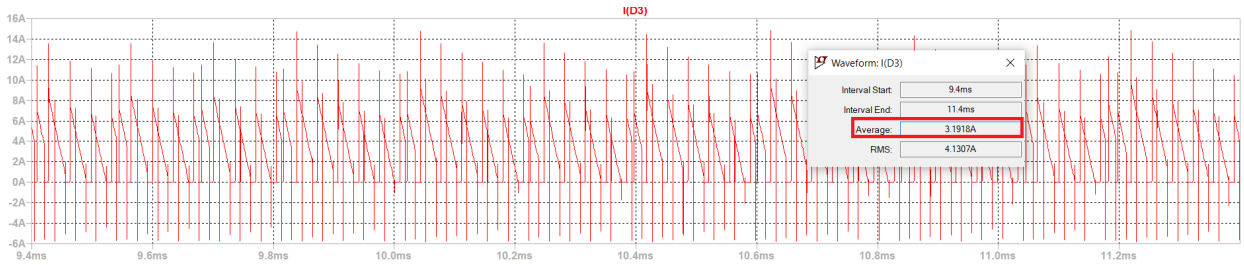


Figure 34. Diode current with 24V input.

For the diode, there seems to be an increase from 3.016A to 3.1918A.

Finally, comparing the efficiencies for the three input scenarios with the given closed loop circuit:

	P_{out}	P_{in}	η
V_{in}=24V	49.425W	61.349W	0.8056
V_{in}=36V	50.487W	59.954W	0.8421
V_{in}=48V	50.632W	58.874W	0.8600

Table 4. Efficiencies with varying inputs.

In all cases, we stand above the limit of 80% efficiency to not be penalized by a negative bonus.

Component Selection

In this part, the switch and diodes selection is explained.

Switch Selection

The maximum drain to source voltage on the MOSFET is measured as about 80V and the maximum current is measured as 8A from the simulations.

While choosing the MOSFET, we looked for these ratings. Also, we checked if it is easily reachable in Turkey. The chosen MOSFET is IRF630.

Type	V_{DSS}	$R_{DS(on)}$	I_D
IRF630	200V	<0.40Ω	9A
IRF630FP	200V	<0.40Ω	9A

Figure 35. Ratings from the datasheet.

Diode Selection

While the maximum reverse voltage on the diode was seen at 75V and the current remained at 3.2A, we can adopt a wide safety factor and select a 100V, 5A diode. An SR5100 diode seems appropriate for this task.

		SYMBOL	SR520	SR530	SR540	SR550	SR560	SR580	SR5100	UNITS
Maximum Recurrent Peak Reverse Voltage		V_{RRM}	20	30	40	50	60	80	100	Volts
Maximum RMS Voltage		V_{RMS}	14	21	28	35	42	56	70	Volts
Maximum DC Blocking Voltage		V_{DC}	20	30	40	50	60	80	100	Volts
Maximum Average Forward Rectified Current .375"(9.5mm) lead length		I_O	5.0							Amps
Peak Forward Surge Current 8.3 ms single half sine-wave superimposed on rated load (JEDEC Method)		I_{FSM}	150							Amps
Maximum Instantaneous Forward Voltage at 5.0A DC		V_F	.55			.70		.85		Volts
Maximum DC Reverse Current at Rated DC Blocking Voltage	$@T_A = 25^{\circ}C$	I_R	2.0							mAmps
	$@T_A = 100^{\circ}C$		50							
Typical Thermal Resistance (Note 1)		$R_{\theta JA}$	18							°C/W
Typical Junction Capacitance (Note 2)		C_J	550			400				pF
Operating Temperature Range		T_J	-65 to +150							°C
Storage Temperature Range		T_{STG}	-65 to +150							°C

NOTES : 1. Thermal Resistance (Junction to Ambient): Vertical PC Board Mounting, 0.5"(12.7mm) Lead Length.
2. Measured at 1 MHz and applied reverse voltage of 4.0 volts.

Figure 36. Ratings from the datasheet.

Conclusion

To conclude, it is seen that flyback topology is found to be appropriate for its advantage of fewer components and no limitations on the duty cycle. lso, it offers a variety of analog controllers. The magnetic design went through several steps not mentioned throughout the report. The most notable would be the transition from a Kool MU toroid to an E core. A Kool MU toroid displayed an immense leakage inductance compared to the magnetizing inductance (at a whopping one third). Some others would be frequency and turn numbers. Moreover, ferrite cores can be used in the magnetic design to both reduce the leakage inductance and arrange the magnetizing inductance properly. Also, loss calculations showed that losses are in the expected range.

The ideal, static and open-loop simulations display that the circuit alone can operate at the desired specifications with the given components. Of course, due to their static nature load regulation or line regulation was not observed. Although the voltage and current stress on the MOSFET are increased due to secondary side effects, there are several available components for these ratings. Finally, appended simulation results more or less approve the claims and calculations. There are some deviations (albeit of minor degree) from the ideal simulations, but these most likely have to do with an insufficient time resolution. If required (upon the

construction of the circuit), some additional filters may be used to send a higher resolution current sensing to the controller and the snubber values may be changed.

References

[1] Analog.com, 2022. [online] Available at: https://www.analog.com/media/en/technical-documentation/data-sheets/lt1241.pdf [Accessed 15 May 2022].