



# **MIDDLE EAST TECHNICAL UNIVERSITY**

## **ELECTRICAL & ELECTRONICS ENGINEERING**

### **EE464 – STATIC POWER CONVERSION II**

#### **TERM PROJECT – DESIGN REPORT**

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## INTRODUCTION

Throughout this paper, an analysis and design of 45 W continuous conduction mode (CCM) flyback converter will be discussed. The specifications of the design are variable input (24 to 48 V) and constant output voltage of 15 V with 3% output voltage ripple. Also, it is required to provide 3% of load and line regulation. From now on, this paper continues with analytic design, magnetic design, snubber design, controller design, simulation results, test results and conclusion parts.

## ANALYTICAL DESIGN

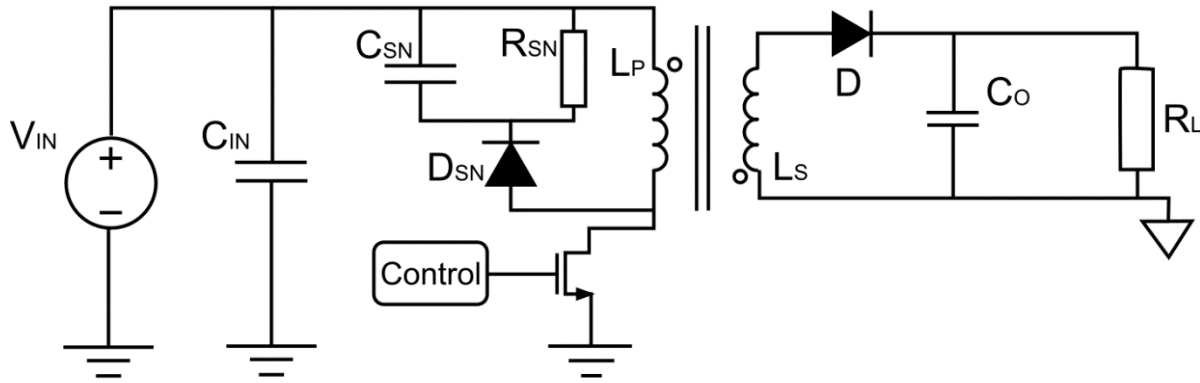


Figure 1. Flyback converter circuit diagram

It is already known that transfer function of flyback converter is as follows:

$$\frac{V_o}{V_{in}} = \frac{N_2}{N_1} \frac{D}{1 - D}$$

Just by inspection from the transfer function, it can be easily seen that 24 V input case is the worst case for this design. So, further designs will be applied referring to this input voltage. For the sake of simplicity, turns ratio is selected as 1:1. Thus,

$$\begin{aligned} \frac{15}{24} &= \frac{D}{1 - D} \rightarrow D = 0.385 \\ \frac{15}{48} &= \frac{D}{1 - D} \rightarrow D = 0.238 \end{aligned}$$

Then, to operate in CCM, it is required to calculate the required magnetizing inductance ( $L_m$ ). Afterwards, maximum and minimum current values should be calculated for the  $L_m$ . According to the TI's application note for CCM flyback converters, it is safe to select  $L_m$  as 1.5 times the calculated minimum inductance [1]. As a result, to calculate the magnetizing inductance value, it

is required to calculate average inductor current. Average inductor current can be calculated as follows.

$$I_m = \frac{N_2}{N_1} I_o \rightarrow I_m = 3 \text{ A}$$

Thus, ripple should be less than the average magnetizing inductor current. To calculate the ripple in the inductor current, voltage waveform of the magnetizing inductance is drawn below.

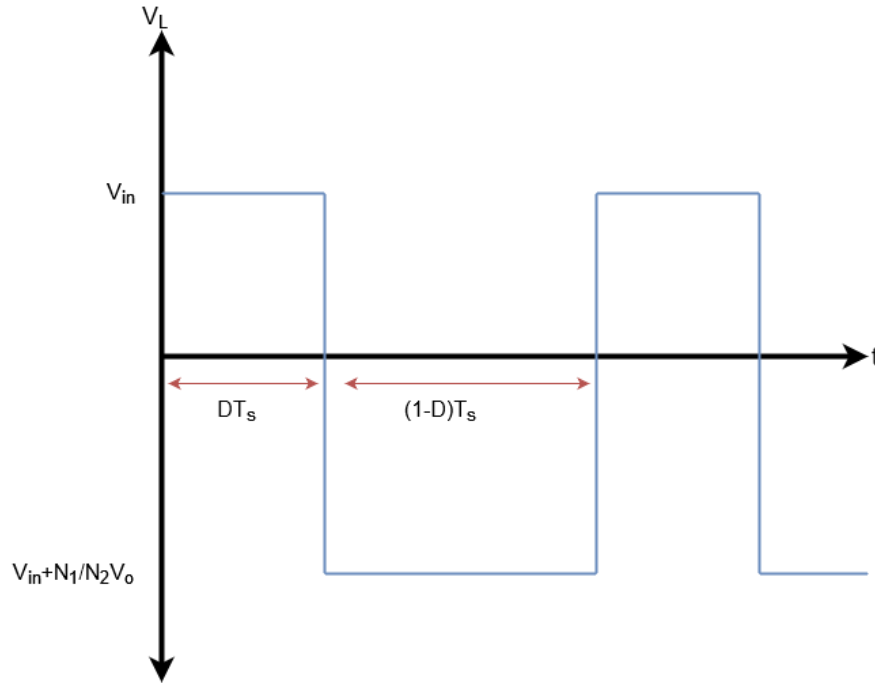


Figure 2. Magnetizing inductor voltage waveform

$$\Delta i_L = \frac{V_{in}DT_s}{2L_m} = \frac{\left(V_{in} + \frac{N_1}{N_2}V_o\right)(1-D)T_s}{2L_m} \leq 3 \text{ A}$$

The worst case for ripple calculation is 48 V input. Hence, minimum magnetizing inductance is calculated as

$$\Delta i_L = \frac{48 \times 0.238 \times 50000^{-1}}{2L_{m,min}} \leq 3 \text{ A} \rightarrow L_{m,min} \geq 38 \mu\text{H}$$

As a result,  $L_m$  is selected as 60  $\mu\text{H}$  for satisfying the requirement. Before moving to the magnetic design part, the peak value of the inductor current should be calculated.

$$\widehat{I}_m = I_m + \frac{V_{in}DT_s}{2L_m} = 6.41 \text{ A}$$

Finally, it comes to output capacitor calculation should be made to meet the ripple requirement and finalize the rough design of the power stage.

$$\Delta V_o = \frac{i_o D T_s}{C} \leq 0.03$$

$$C \geq \frac{i_o D T_s}{0.03 V_o}$$

Table 1. Output capacitor calculations for different cases

Case	C <sub>min</sub> (μF)
V <sub>in</sub> = 24V, I <sub>o</sub> = 3A	25.64
V <sub>in</sub> = 24V, I <sub>o</sub> = 0.3A	2.564
V <sub>in</sub> = 48V, I <sub>o</sub> = 3A	15.87
V <sub>in</sub> = 48V, I <sub>o</sub> = 0.3A	1.587

Note that the values in Table 1 are the minimum required capacitance value. Thus, selecting capacitors with a higher value will provide a safety margin because as the DC bias across the capacitor increases, their actual capacitance decreases.

## MAGNETIC DESIGN

To handle the magnetic design, a MATLAB script is written for ferrite EE cores available in the laboratory. The script basically calculates the required parameters for a flyback transformer for each of the core with a fill factor of 0.3. In this paper, only the selected core will be presented.

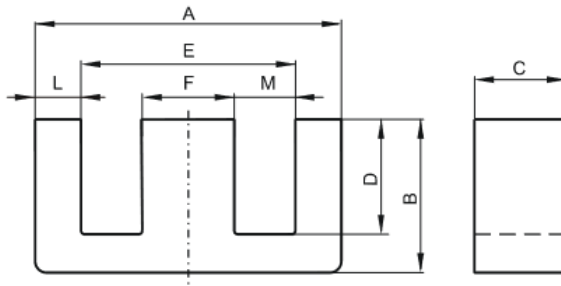


Specification for:

**0P44022EC**

110 Delta Drive  
Pittsburgh, PA 15238  
Phone: 412/696-1333  
Fax: 412/696-0333  
Email: magnetics@spang.com

### DIMENSIONS



(mm)	Nominal:	Tol. min.:	Tol. max.:
<b>A</b>	43.0	-1.7	0.0
<b>B</b>	21.0	-0.2	+ 0.2
<b>C</b>	20.0	-0.8	0.0
<b>D</b>	14.8	0.0	+ 0.6
<b>E</b>	29.5	0.0	+ 1.4
<b>F</b>	12.2	-0.5	0.0
<b>L</b>	6.75 Nom.		
<b>M</b>	8.65 Nom.		
<b>Eff. Parameters</b>			
<b>Ae mm<sup>2</sup></b>	<b>Amin mm<sup>2</sup></b>	<b>le mm</b>	<b>Ve mm<sup>3</sup></b>
233.0	233.0	97.0	22700

### INDUCTANCE

<b>AL value (nH)</b>	<b>Test conditions</b>
Nom: 6013 Min.: 4510	10 kHz, < 0.5 mT, 25 °C

### MARKING

0P44022EC  
PXXXXX

Figure 3. Datasheet of the selected core

The selected core is 0P44022EC ferrite EE core manufactured by Magnetics with P material. The core has an effective area of 233 mm<sup>2</sup>, an effective length of 67 mm, and a relative permeability of 2500. Then, following calculations are made via the MATLAB script.

$$\frac{N_{\text{pri}}^2}{R} = L_m$$

$$\frac{N_{\text{pri}}}{R} = \frac{B_{\text{core}} A_{\text{core}}}{\widehat{I_m}}$$

where  $B_{\text{core}}$  is selected as 0.1 T since P material ferrite has a sharp saturation at approximately 0.47 T. Rearranging the equations above yields

$$N_{\text{pri}} = \frac{L_m \widehat{I_m}}{B_{\text{core}} A_{\text{core}}} = 12$$

Note that turns ratio was selected as 1 for simplicity. Hence,  $N_{\text{sec}}$  is also 12. Then, it comes to airgap calculation.

$$R = \frac{N_{\text{pri}} \widehat{I_m}}{B_{\text{core}} A_{\text{core}}} = \frac{l_e}{\mu_0 \mu_r} + \frac{2g}{\mu_0 A_e}$$

$$g = \mu_0 \frac{N_{\text{pri}} \widehat{I_m}}{2B_{\text{core}}} - \frac{l_e}{2\mu_r} \approx 0.4 \text{ mm}$$

Measuring 0.4 mm is quite hard for the present instruments but it is arranged by using 4 A4 sheets, each has 0.1 mm thickness.

One step is remaining: cable selection. Cable is selected according to the AWG standards. To stay on the safe side, current density is selected in between 3 – 4 A/mm<sup>2</sup>.

22	0.0253	0.64516	0.327	16.14	52.9392	7	0.92	42 kHz	18 lbs
23	0.0226	0.57404	0.259	20.36	66.7808	4.7	0.729	53 kHz	14.5 lbs
24	0.0201	0.51054	0.205	25.67	84.1976	3.5	0.577	68 kHz	11.5 lbs
25	0.0179	0.45466	0.162	32.37	106.1736	2.7	0.457	85 kHz	9 lbs
26	0.0159	0.40386	0.128	40.81	133.8568	2.2	0.361	107 kHz	7.2 lbs

Figure 4. AWG cable standards

Although the AWG23 cable is meeting the requirements, AWG26 was available in the laboratory. Hence, the core is wined with AWG26. The RMS value of the primary and secondary currents are calculated as

$$I_{\text{pri,RMS}} = \sqrt{D} \widehat{I_m} = 3.977 \text{ A}$$

$$I_{\text{sec,RMS}} = \sqrt{1 - D} \widehat{I_m} = 5.031 \text{ A}$$

Number of parallel conductors are calculated as

$$\text{\#of paralel conductors in primary} = \frac{I_{\text{pri,RMS}}}{JA_{\text{cu}}} = 10$$

$$\text{\#of paralel conductors in secondary} = \frac{I_{\text{sec,RMS}}}{JA_{\text{cu}}} = 13$$

After all, using the results above, core and copper losses are calculated as follows.

$$R_{\text{cu}} = \rho \frac{l}{A_{\text{cu}} \times \text{\#of paralel conductors}}$$

where  $\rho$  is the resistivity of the copper which is  $1.68 \times 10^{-8} \Omega \cdot \text{m}$ .

$$R_{\text{cu,pri}} = 9.5 \text{ m}\Omega$$

$$R_{\text{cu,sec}} = 0.79 \text{ m}\Omega$$

$$P_{\text{cu}} = I_{\text{pri,RMS}}^2 R_{\text{cu,pri}} + I_{\text{sec,RMS}}^2 R_{\text{cu,sec}} = 0.172 \text{ W}$$

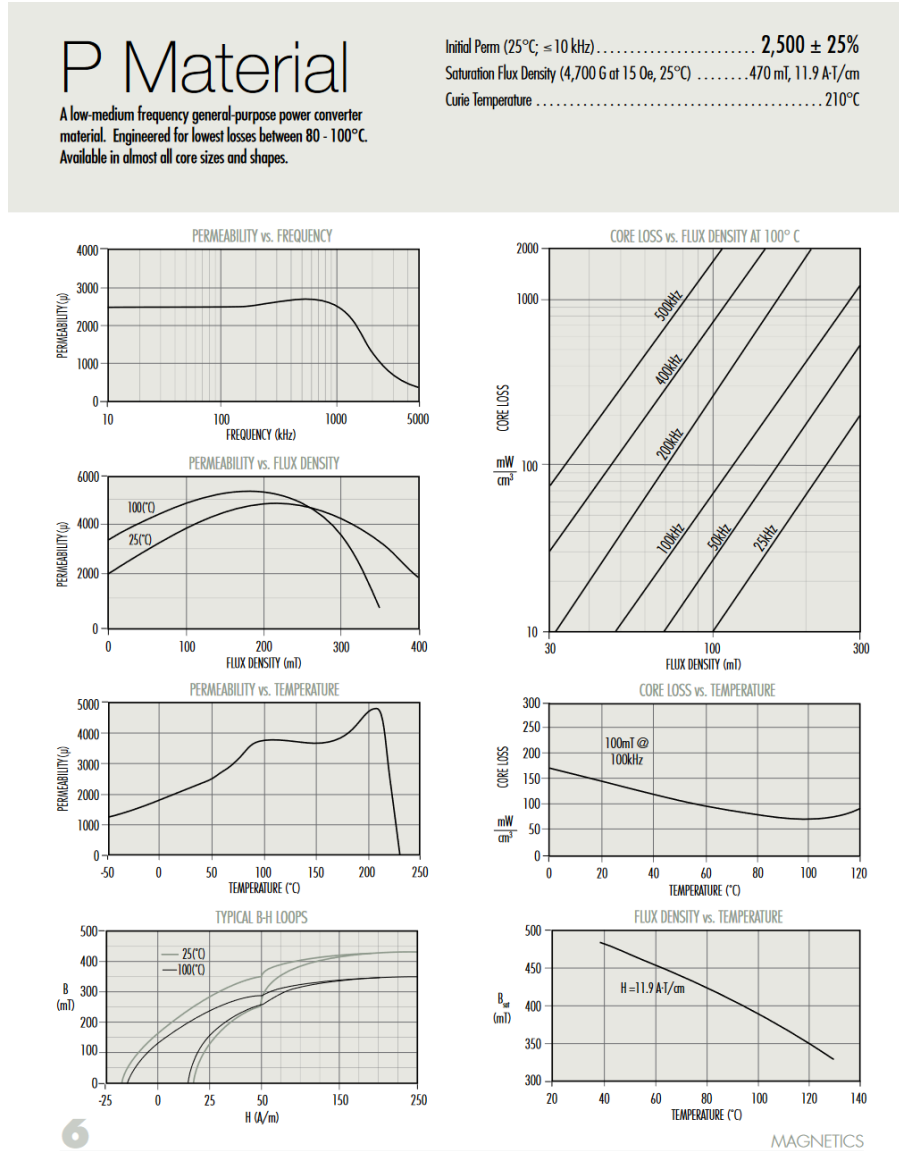


Figure 5. Core material datasheet

$$\Delta B = \frac{N_{pri}}{RA_{core}} (I_{m,max} - I_{m,min}) = 89.2 \text{ mT}$$

$$P_{core} = 11 \times 22.7 = 249.7 \text{ mW}$$

where 11 mW/cm<sup>3</sup> is the core loss density of the core at 50 kHz with a  $\Delta B$  of 90 mT, and 22.7 cm<sup>3</sup> is the volume of the core.



## CLOSED-LOOP SIMULATION

The closed-loop simulation is based on the example circuit of the controller [2].

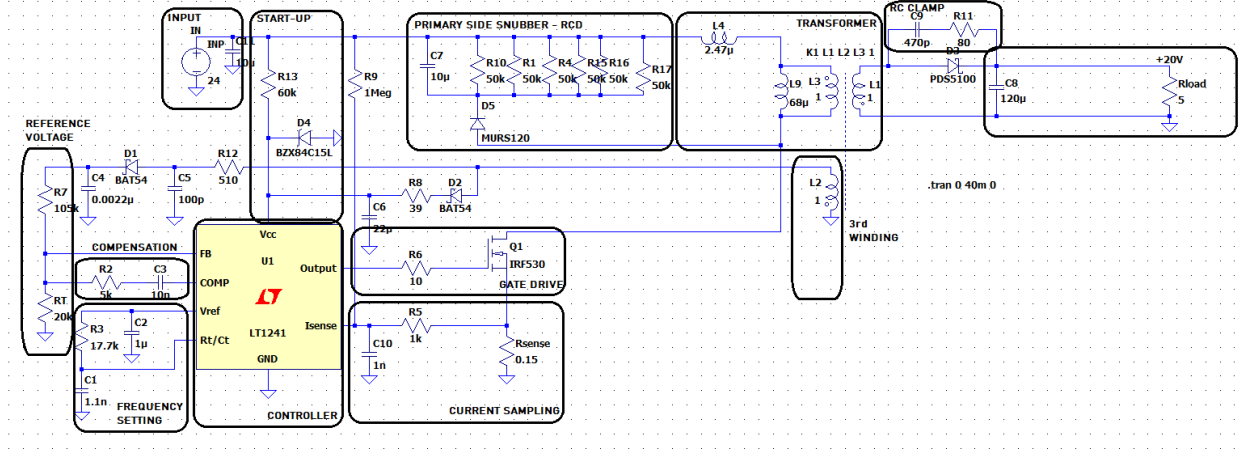


Figure 6. Schematic of the closed-loop design.

The design is comprised a fully closed loop operated by a current mode controller UC3845. For SPICE simulations, an equivalent controller LT1241 was utilized. Our main motivation in employing UC3845 as the controller can be listed as follows:

- a no-opto solution
- CCM operation
- current mode control

Guaranteeing that the circuit operates in CCM facilitates control with the simple voltage transfer function,

$$\frac{V_o}{V_{in}} = \frac{N_2}{N_1} \frac{D}{1-D}$$

Allowing a turns ratio of “1”, the circuit mathematically becomes no different than a buck-boost converter. Moreover, with the output voltage always less than the input, the circuit always operates in the buck mode, implying the duty cycle is not any higher than 0.5.

At the input is a DC link filter to avert inrush current related problems.

A start-up circuit ensures the circuit does not remain in an undesired UVLO. The diode D4, as a Zener diode, clamps the voltage at the ON voltage of the controller (15V) and allows excessive current flow through it. The UVLO pin is also fed by the third winding.

Through the auxiliary third winding, the reference voltage (the node between R7 and RT) is pinned at the aimed output voltage of 15V. Moreover, a compensation branch (acting as a PI controller) also acts as a regulator of the output voltage waveform and its steady state response (errors in the steady state). The  $K_p$  and  $K_i$  coefficients (R2 and C3) were tuned by monitoring the output voltage waveform and their success in keeping the steady state output voltage with an average of 15V and with a ripple less than 3% of the rated average.

The frequency is adjusted through R3 and C1 according to the following relation:

$$f_{sw} = \frac{1.72}{2 * R_3 C_1}$$

Accordingly, the switching frequency is set as 44.170kHz. This result denotes a 10% deviation from the aimed 50kHz but considering the tolerance ranges for the components and our broad safety factor of 1.5 in our magnetic design, this drop in the frequency should be tolerable in keeping the circuit at CCM.

UC3845 boasts an internal gate drive for the external MOSFET Q1. They are connected via a 10 $\Omega$  resistor.

A shunt resistor of 150m $\Omega$  is utilized to sample current via the voltage drop on the resistor. The resultant voltage is input to an RC filter comprised of R5 and C10 with a cutoff frequency,

$$f_c = \frac{1}{2\pi C_{10} R_5} = 159.154\text{kHz}$$

This filter is essential in sending the sampled current signal with a high resolution since the controller deals with the peak of the signal it receives. With a cutoff of thrice the fundamental, the interference of notches is prevented.

The transformer is rendered more realistic with its equivalent parameters, leakage and magnetizing inductances. The values obtained after the winding of the core are put in place. Copper losses of the transformer are not modeled due to the m $\Omega$ -range of individual parallel paths of the transformer windings which will be rendered even more ineffective due to their parallel connection.

Connected to the negative terminal of the primary is the anode of the RCD snubber. The snubber loop will help in minimizing ringing and EMI problems that arise from the switching of the MOSFET leading to impulsive voltage drops on the inductor components of the transformer.

## SNUBBER DESIGN

The snubber design started with the equation below. This equation is calculating the snubber loss.[4]

$$P_{sn} = V_{sn} \frac{i_{peak} \cdot t_s}{2} f_s = \frac{L}{2} i_{peak}^2 \frac{V_{sn}}{V_{sn} - nV_o} f_s$$

Here, the  $I_{peak}$  and  $f_s$  is known.  $f_s$  is decided by us as 44kHz for a proper magnetic design.  $I_{peak}$  is measured as 7A from simulations and calculated as 6A for magnetic design.

From the equation, we can decrease snubber loss by increasing the  $V_{sn}$ . However, this voltage will be blocked by a diode. Hence, we must choose a proper  $V_{sn}$ . We chose 140V because we have a 150V diode already.

Then the calculation is done by these values.

- $V_{sn}=140V$
- $L_{leak}= 2.47\mu H$
- $V_{sec}=16$
- $f_s= 44kHz$

And  $P_{sn}$  is calculated as 3W.

$$R_{sn} = \frac{V_{sn}^2}{\frac{L}{2} i_{peak}^2 \frac{V_{sn}}{V_{sn} - nV_o} f_s}$$

Then, the snubber resistance is calculated from the equation above as 6.6kΩ. The power dissipation was still too much for a resistor. So, we put 6 47kΩ resistor to share power.

$$\Delta V_{sn} = \frac{V_{sn}}{C_{sn} R_{sn} f_s}$$

With this equation, we limit the ringing on the snubber. To make it less  $C_{sn}$  chosen as 10uH. However, we could not find any capacitance to handle this voltage. Hence, we use the design below.

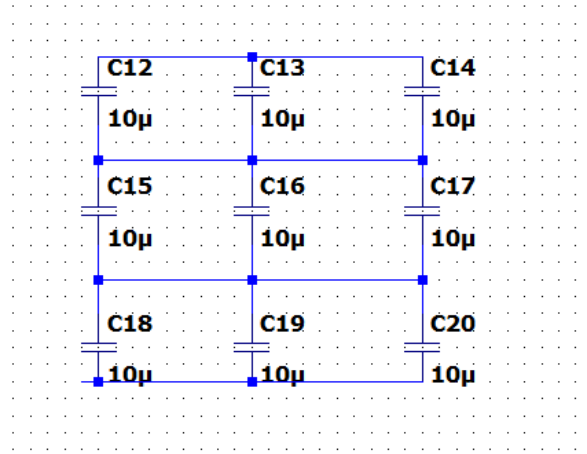


Figure 7. Design for snubber capacitance

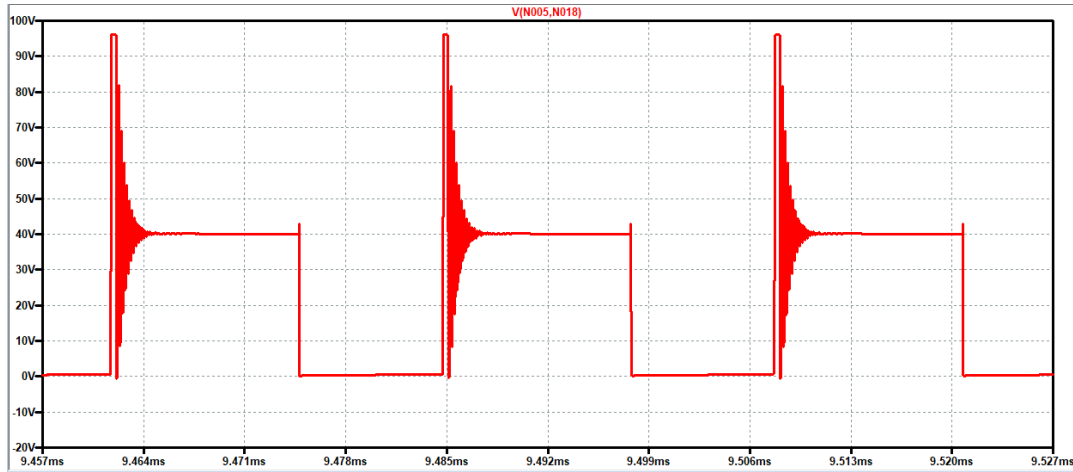


Figure 8. Drain to source voltage

After the design was done, the drain to source voltage graph is measured as above.

At the secondary is another snubber that arises from the switching of the diode. This snubber's design [3] formulates an RC branch using the switching frequency and the measured leakage inductance. We measured  $L_{\text{leakage}}$  to be  $2.84706\mu\text{H}$ .

It is recommended that there be two orders of magnitude between switching frequency and the snubber's ringing frequency assumed for a good design. Our aimed switching frequency was 50kHz, but due to the unavailability of the proper resistance values, it appears 44kHz in practice. Therefore, a ringing frequency of 44MHz will be assumed for a margin of two orders of magnitude. The impedance of the leakage inductance:  $Z = 2\pi f_{\text{ringing}} L_{\text{leakage}} = 78.709\Omega$ . This is taken directly as the snubber resistance.

$C_{\text{snub}}$  used to minimize power dissipation at  $f_{\text{sw}}$  and allow the resistor to be effective at  $f_{\text{ringing}}$ .

$$C_{\text{snub}} = \frac{1}{2\pi f_{\text{ringing}} R_{\text{snub}}} = 459.5\text{pF} \cong 470\text{pF}$$

Power dissipation:  $CV_{\text{diode}}^2 f_{\text{sw}}$ . Here, the article removes the 0.5 factor in the capacitor power equation, stating the capacitor charges and discharges continuously. Accordingly,  $P = 149\text{mW}$ .

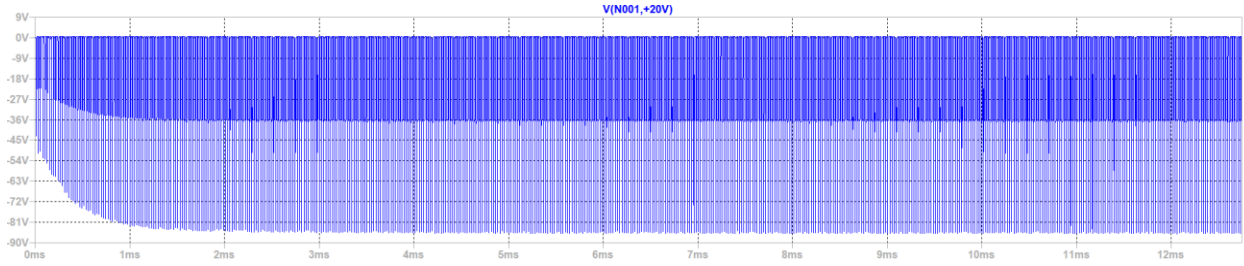


Figure 9. The voltage across the diode without the secondary snubber.

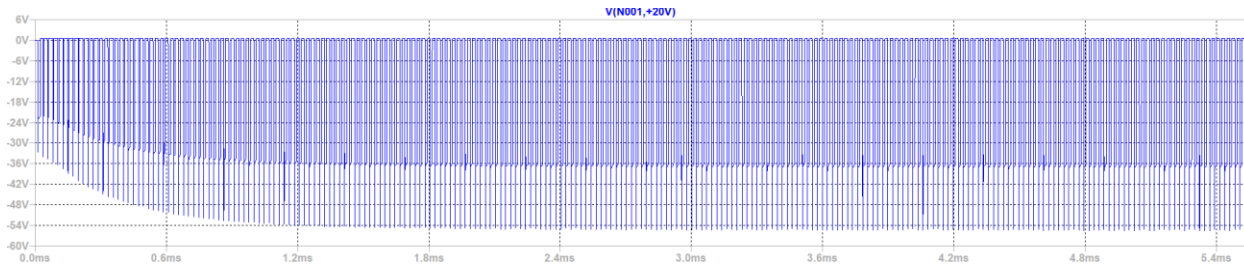


Figure 10. The voltage across the diode without the secondary snubber.

Accordingly, voltage spikes have been suppressed by a 30V difference.

Finally, at the output, is our load and a high filter capacitance in minimizing voltage ripple. Here, an important factor to consider in the composition of the output capacitor is ESR, which exists inherently for electrolytic capacitors and can be significant enough to increase output voltage ripple. Therefore, it is important to place multiple capacitors in parallel to avert this undesired byproduct – decreasing effective ESR.

Comparing the output voltage waveform for different load-line variations,

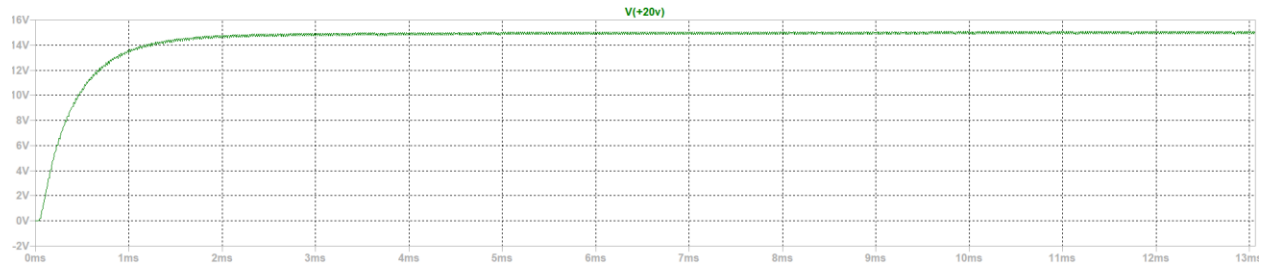


Figure 11. Output Waveform with 24V input and 5Ω load.

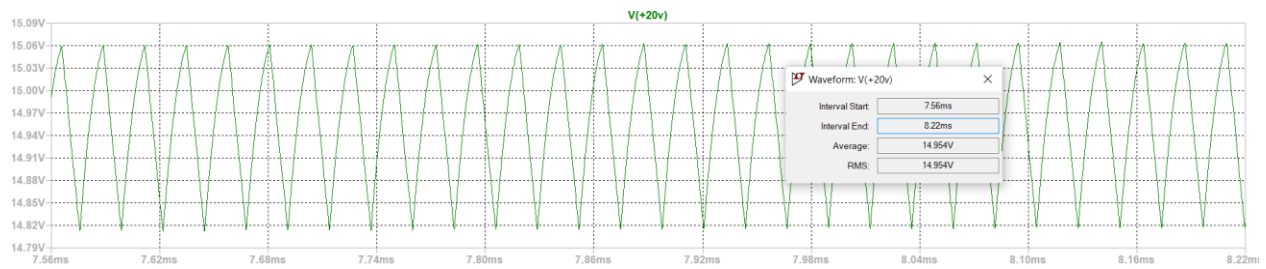


Figure 12. Zoomed voltage waveform.

$$\frac{\Delta V_{\text{out}}}{V_{\text{out}}} = \frac{270\text{mV}}{14.954\text{V}} = 1.806\% < 3\%$$

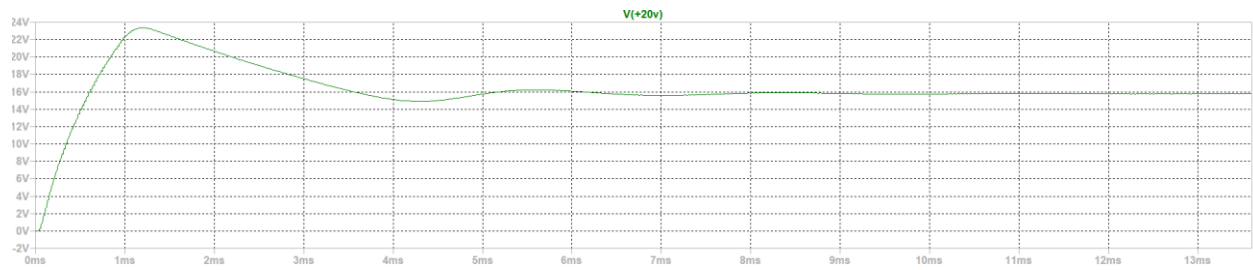


Figure 13. Output Waveform with 24V input and 50Ω load.

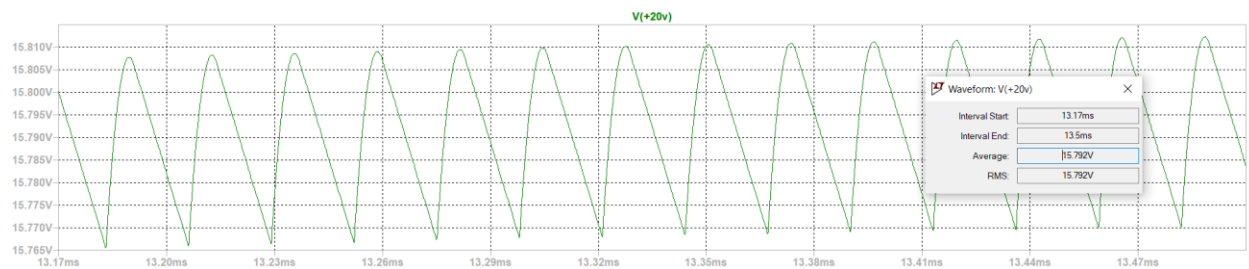


Figure 14. Zoomed voltage waveform.

$$\frac{\Delta V_{\text{out}}}{V_{\text{out}}} = \frac{430\text{mV}}{15.792\text{V}} = 2.723\% < 3\%$$

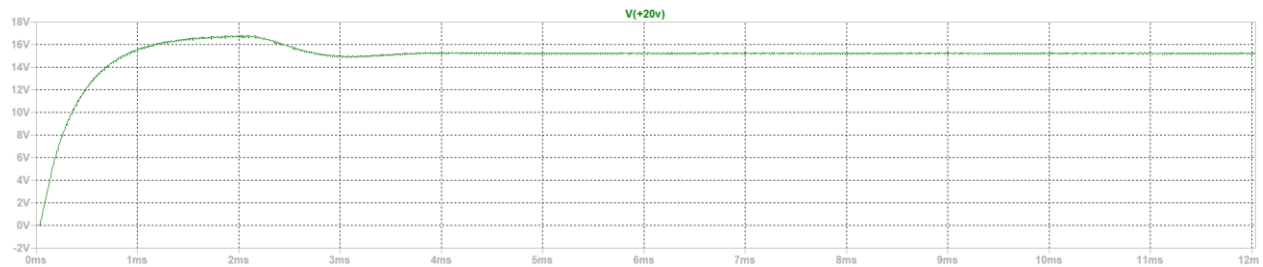


Figure 15. Output voltage ripple with 48V input and 5Ω load.

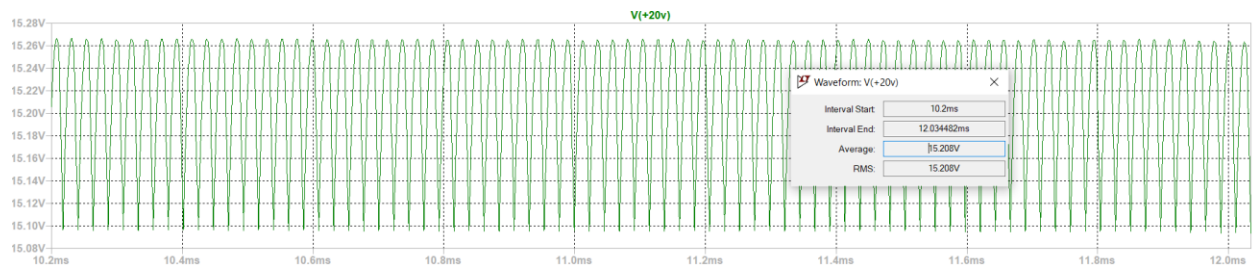


Figure 16. Zoomed voltage waveform.

$$\frac{\Delta V_{\text{out}}}{V_{\text{out}}} = \frac{165\text{mV}}{15.208\text{V}} = 1.804\% < 3\%$$

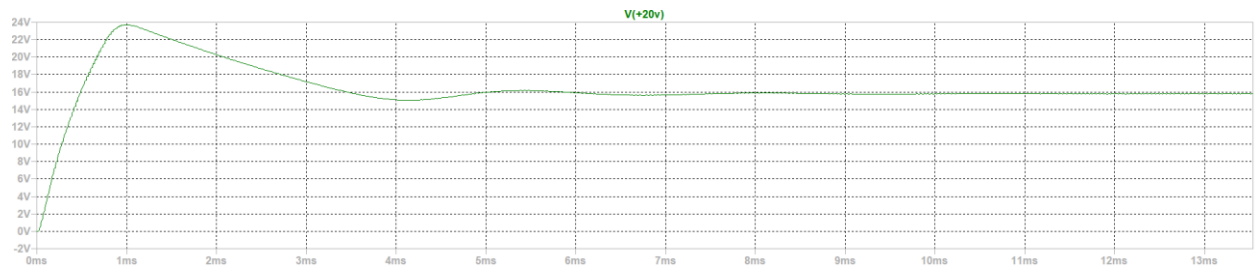


Figure 17. Output voltage ripple with 48V input and 50Ω load.

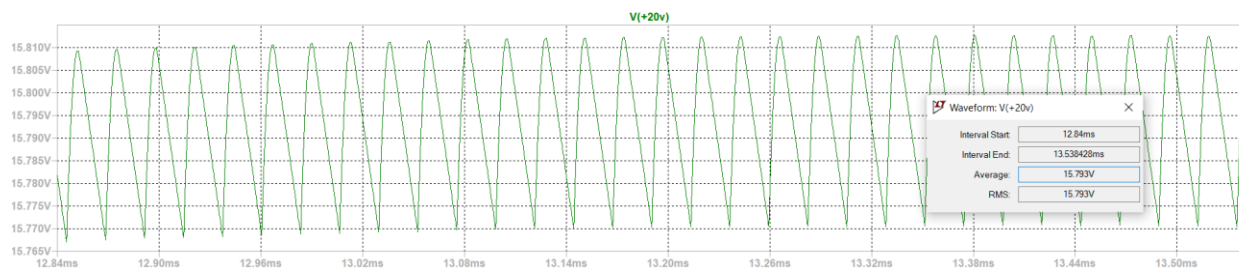


Figure 18. Zoomed voltage waveform.

$$\frac{\Delta V_{\text{out}}}{V_{\text{out}}} = \frac{420\text{mV}}{15.793\text{V}} = 2.659\% < 3\%$$

Input and Load Case	Efficiency	Output Voltage	Voltage Ripple
24V, 5Ω	$\frac{(14.958\text{V})^2}{5\Omega} \times \frac{1}{2.288\text{A} * 24\text{V}} = 0.8149$	14.958V	1.806%
24V, 50Ω	$\frac{(15.792\text{V})^2}{50\Omega} \times \frac{1}{0.241\text{A} * 24\text{V}} = 0.8623$	15.792V	2.723%
48V, 5Ω	$\frac{(15.208\text{V})^2}{5\Omega} \times \frac{1}{2.288\text{A} * 24\text{V}} = 0.8447$	15.208V	1.804%
48V, 50Ω	$\frac{(15.793\text{V})^2}{50\Omega} \times \frac{1}{0.128\text{A} * 48\text{V}} = 0.8117$	15.793V	2.659%

Table 2. Efficiencies and output voltage characteristics for varying load and line cases.

Both the efficiencies and ripple ratios appear below the maximum limits.

Line Regulation (5Ω)	$\frac{15.208\text{V} - 14.958\text{V}}{15\text{V}} = 1.67\%$
Line Regulation (50Ω)	$\frac{15.793\text{V} - 15.792\text{V}}{15\text{V}} \cong 0\%$
Load Regulation (24V)	$\frac{15.792\text{V} - 14.958\text{V}}{15\text{V}} = 5.56\%$
Load Regulation (48V)	$\frac{15.793\text{V} - 15.208\text{V}}{15\text{V}} = 3.9\%$

Table 3. Load and line regulations.

The line regulation is excellent for the low load case and is within the acceptable limits for the rated load case. The load regulation is higher than the limit of 3.9% for both loads.



## COMPONENT SELECTION

### Switches

#### 1. MOSFET

After designing the snubber circuit, the voltage stress on the MOSFET (drain to source) is calculated around 100V and simulation also showed it same. Also, the current flow through it is 2.5A in average. However, there are some notches at the switching moments to 7A. Hence, with a safety margin, we looked for 150V, 9A MOSFET. Because of the chip crises, we found IRF630 which is 200V,9A n-channel MOSFET.

#### 2. Snubber Diode

To design the snubber circuit, we decided a diode, which is durable for 7A and 100V. The decision is done at snubber circuit design part. With a safety margin, we choose MUR10150 which is 10A,150V Schottky Diode.

#### 3. Output Diode

At output, the rated current is 3A and the rated voltage is 15V. With a safety margin, SR5100 is chosen which is 5A,100V Schottky diode. The voltage rating is much than we needed, but the access of this diode was easier. Hence, we saved our time.

#### 4. Third Winding Diodes

At third winding there is two Schottky diode to prevent reverse current flow through the winding. Because if it flows, there will be no power stacking in Lm. Then we could not transfer the power to output. These diodes are carrying much less current than others. Because the current flow through third winding is less. Hence, MBR560 is chosen for them.

#### 5. IC VCC Diode

There is need for a 16V Zener because we want to use single supply and the input is varying. We used a Zener diode to clamp VCC voltage of the IC which is BZX84C15LT1.

### Capacitors and Resistors

To make easy to solder we used 1206 package capacitors and resistors and the voltage ratings were decided from the simulation and some safety margin.

## DEMO RESULTS

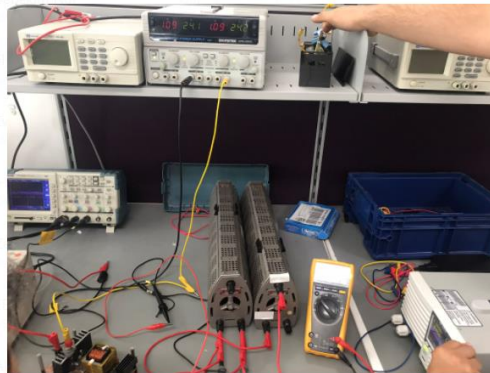
Input Voltage	Input Current	Input Power	Output Voltage	Output Current	Output Power	Efficiency	Ripple
48	1,09	52,32	13,94	2,788	38,86472	74,28272171	0,4
24	2,15	51,6	13,5	2,7	36,45	70,63953488	0,36
48		0	14,65	0,586	8,5849	#DIV/0!	
24		0	14,65	0,586	8,5849	#DIV/0!	

Table 4. Demo Results

There is a missing info. The input current was not taken at demo. Hence, we cannot calculate the efficiency at low load.

From the table,

- Line regulation is calculated as 3%.
- Load regulation is calculated as 4.7% at 48V input.
- Again, load regulation is calculated as 7.5% at 24V input.
- Max ripple is measured as 2.6%.



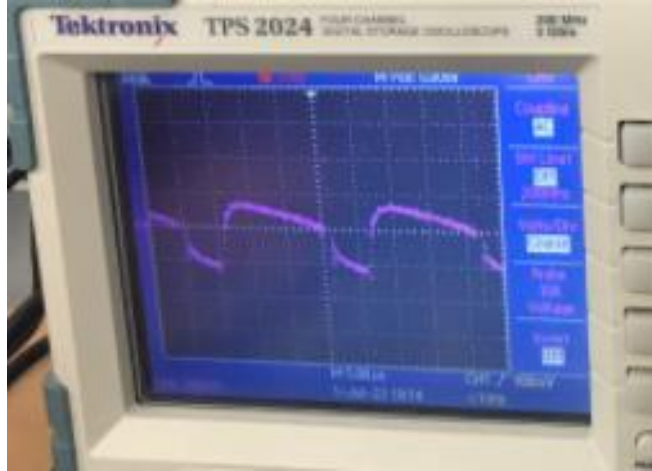


Figure 19. Some Demo Results photos

## CONCLUSION

Throughout this hardware project, closed loop isolated DC/DC converter, specifically flyback topology, is analyzed by means of analog controller. The regulation is made via the 3<sup>rd</sup> winding, i.e., the output voltage feedback is taken via an auxiliary winding which is reversely coupled with the primary winding like secondary winding. It is seen that calculated and simulated results do not correlate with the actual results. This is due to the parasitic effects coming from the leakage inductance, line inductance and switching components, which are affecting the feedback voltage and sense current. With the help of the RC filters, these phenomena are tried to be reduced as much as possible. Moreover, in an SMPS like this paper discussed, the magnetic design is quite important for the overall system performance because it affects the control loop characteristics as well as the output characteristics. Specifically, filter design in the control loop is strongly dependent on the transformer design. Also, it might be difficult to design flyback transformer because the airgap is utilized for energy storing during the on period. In other words, the flyback transformer acts like coupled inductor which filters the primary side current. Hence, adjusting airgap is the core of the magnetic design in a flyback DC/DC converter since it strongly affects the mode of operation. Furthermore, peak current mode control method helps to supply a good load regulation with a high line regulation which are the most important characteristics for a power supply. To conclude with, it should be considered that design of a flyback converter with auxiliary winding sensing is quite comprehensive and hard to implement in terms of ensuring the safe load and line regulations.

## APPENDIX A: BILL OF MATERIALS

Component	Description	Designator	Footprint	LibRef	Quantity	Price (per unit)
1NF	CAP,1UF(16V,10%,CER,X7R,SMD-1206)	C1, C3	1206N	10023689-135	2	\$0.060
1UF	CAP,1UF(16V,10%,CER,X7R,SMD-1206)	C2, C20	1206N	10023689-135	2	\$0.060
2.2NF	CAP,1UF(16V,10%,CER,X7R,SMD-1206)	C4	1206N	10023689-135	1	\$0.026
100PF	CAP,1UF(16V,10%,CER,X7R,SMD-1206)	C5,C10	1206N	10023689-135	1	\$0.029
22UF	CAP,1UF(16V,10%,CER,X7R,SMD-1206)	C6	1206N	10023689-135	1	\$0.109
10UF	CAP,1UF(16V,10%,CER,X7R,SMD-1206)	C7, C7_1, C7_2, C7_3, C	1206N	10023689-135	15	\$1.481
22UF	CAP,22UF(25VDC,20%,CER,X5R,SMD-0805)	C8, C9, C11, C12, C13, C	0805L	30000061	6	\$0.654
470PF	CAP,1UF(16V,10%,CER,X7R,SMD-1206)	C16	1206N	10023689-135	1	\$0.109
100NF	CAP,1UF(16V,10%,CER,X7R,SMD-1206)	CG	1206N	10023689-135	1	\$0.109
MBR560	Schottky Rectifier	D1	TO-220AC	Diode 10TQ035	1	\$0.304
SR5100	3 Amp General Purpose Rectifier	D2	DO-201AD	Diode 1N5401	1	\$0.164
MBR10100	Schottky Rectifier	D3	TO-220AC	Diode 10TQ035	1	\$0.854
BZX84C15LT1	DIODE(ZNR,15V,SOT-23)	D4	SOT23_190P290X240X1	5961-1315-0002	1	\$0.029
MBR10150	Schottky Rectifier	D5	TO-220AC	Diode 10TQ035	1	\$0.723
NMOS-2	N-Channel Power MOSFET	Q1	TO-220AB	NMOS-2	1	\$2.573
470M OHM	RES,3M(THFL,2W,1%,SMD-2512)	R1_1, R1_2, R1_3	2512N	30007383	3	\$0.015
0 OHM	RES,0R(THFL,0.250W,0%,SMD-1206)	R2_1, R3_2, R7_1	1206L	10023672-5	3	\$0
10K OHM	POT,10KR(CRMT_LIN,0.25W,10%,MULT,SMD)	R2_2	pot_3224j	5905-9993-1034	1	\$0.005
15K OHM	RES,0R(THFL,0.250W,0%,SMD-1206)	R3_1	1206L	10023672-5	1	\$0.005
2.7K OHM	RES,0R(THFL,0.250W,0%,SMD-1206)	R3_3, R7_2, R7_3	1206L	10023672-5	3	\$0.015
10K OHM	RES,0R(THFL,0.250W,0%,SMD-1206)	R4_1, R4_2	1206L	10023672-5	2	\$0.010
1K OHM	RES,0R(THFL,0.250W,0%,SMD-1206)	R5	1206L	10023672-5	1	\$0.005
10R OHM	RES,0R(THFL,0.250W,0%,SMD-1206)	R6	1206L	10023672-5	1	\$0.005
100K OHM	RES,0R(THFL,0.250W,0%,SMD-1206)	R7_4, R13_1, R13_2, R1	1206L	10023672-5	4	\$0.020
39R OHM	RES,0R(THFL,0.250W,0%,SMD-1206)	R8	1206L	10023672-5	1	\$0.005
1MEG OHM	RES,0R(THFL,0.250W,0%,SMD-1206)	R9, R14_1, R14_2, R14	1206L	10023672-5	4	\$0.020
47K OHM	RES,0R(THFL,0.250W,0%,SMD-1206)	R10_1, R10_2, R10_3, R	1206L	10023672-5	6	\$0.030
80 OHM	RES,0R(THFL,0.250W,0%,SMD-1206)	R11	1206L	10023672-5	1	\$0.005
120R OHM	RES,0R(THFL,0.250W,0%,SMD-1206)	R12_1	1206L	10023672-5	1	\$0.005
390R OHM	RES,0R(THFL,0.250W,0%,SMD-1206)	R12_2	1206L	10023672-5	1	\$0.005
UC3845D8	No Description Available	U1	D8	UC3845D8	1	\$0.090
AWG26 cable	No Description Available	(-)	(-)	(-)	8m	\$1.595
0P44022EC ferrite core	No Description Available	(-)	(-)	(-)	1	contact distributor
Circuit Board	No Description Available	(-)	(-)	(-)	1	\$4.83
TOTAL:						\$13.949 + core

Table 3. Bill of materials.

The magnetic core 0P44022EC from Magnetics, Inc. requires specific contact with the recognized distributors in pricing. Excluding the core, the circuit costs \$13.95 per unit.

## APPENDIX B: PCB DESIGN

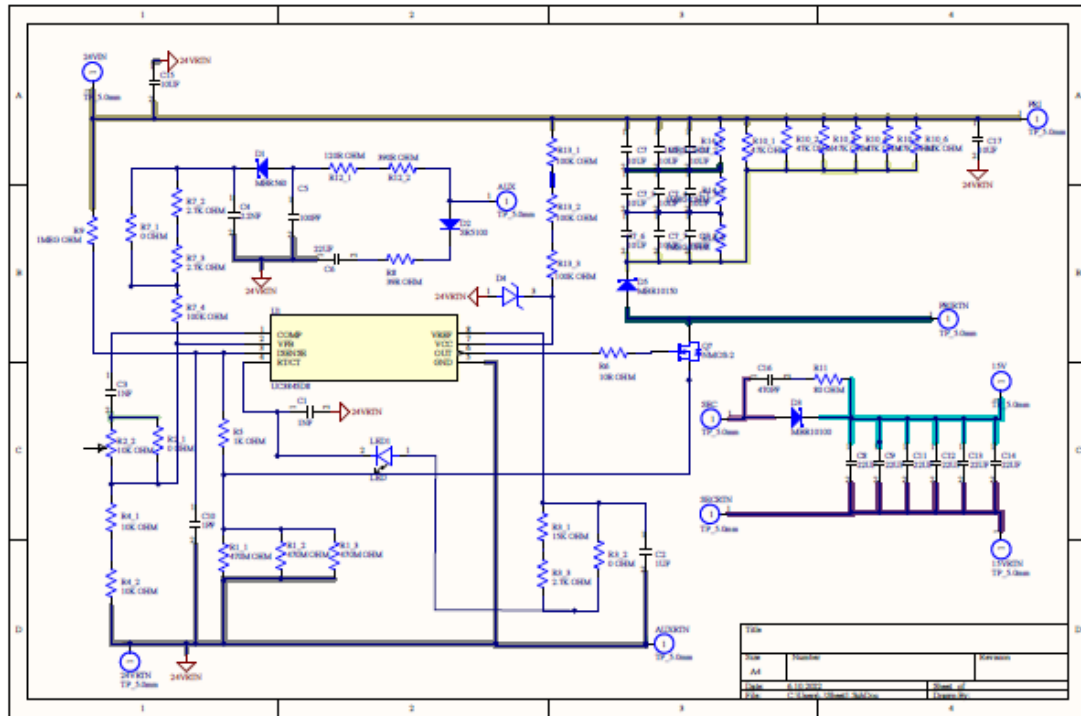


Figure 20. Schematic of the circuit

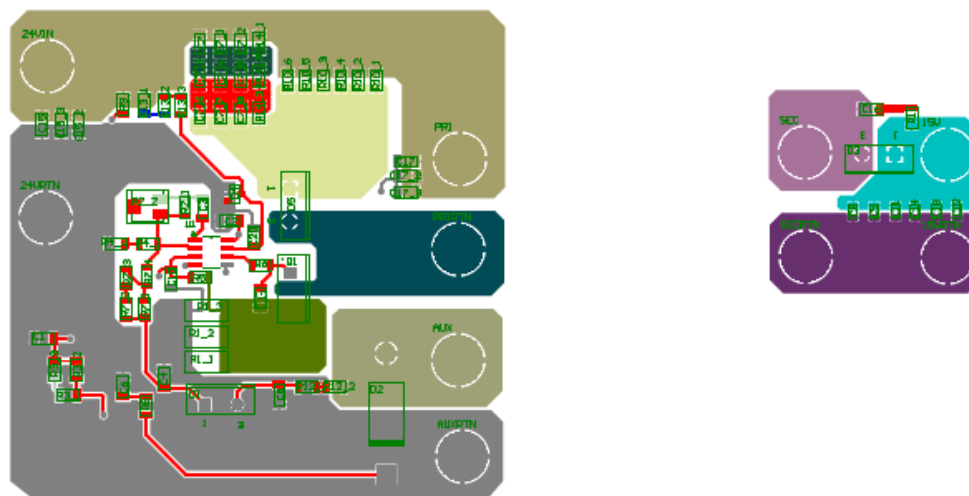
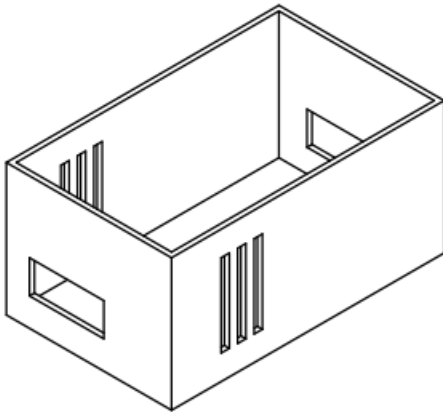
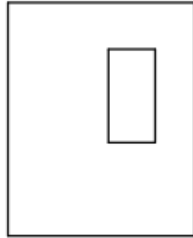


Figure 21. Layout of the circuit

## APPENDIX C: INDUSTRIAL DESIGN



## REFERENCES

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