# SEQUENTIAL LOGIC CIRCUITS


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## PRELIMINARY WORK

1.In combinational logic circuits output depends only on the input but in the sequential logic circuits output depends on the current inputs and past states.

2. The reason is not using set = reset =0, Q and the $\bar{Q}$ (output and opposite value of the output) both are getting 1. It can't be happened. In latch Q and the $\bar{Q}$ should not be equal ($Q \neq \bar{Q}$ ). Here this basic requirement violates.

3. NOR and NAND gates have different logics even though they use for getting S-R latch

Table01: Characteristic table for NOR gate S-R latch

| S | R | Q | $\bar{Q}$ |
|---|---|---|---|
| 0 | 0 | Memory | |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | Undefined | |

Table02: Characteristic table for NAND gate S-R latch

| S | R | Q | $\bar{Q}$ |
|---|---|---|---|
| 0 | 0 | Invalid | |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | Memory | |

According to the above two tables we can see that the output for same input in NOR gate S-R latch is opposite for the output in NAND gate S-R latch. Therefore, if we replace NOR gate S-R latch for NAND gate S-R latch it won't work properly.

4. In S-R flipflop when S=1 and R=1 output becomes unpredictable but in the case of JK flip flop the output will toggle to the opposite state. It is the major advantage.

5.

Table 03: function table of JK flipflop

| CLK | J | K | Q |
|---|---|---|---|
| ⎍ | 0 | 0 | Q |
| ⎍ | 0 | 1 | 0 |
| ⎍ | 1 | 0 | 1 |
| ⎍ | 1 | 1 | $\bar{Q}$ |

6.

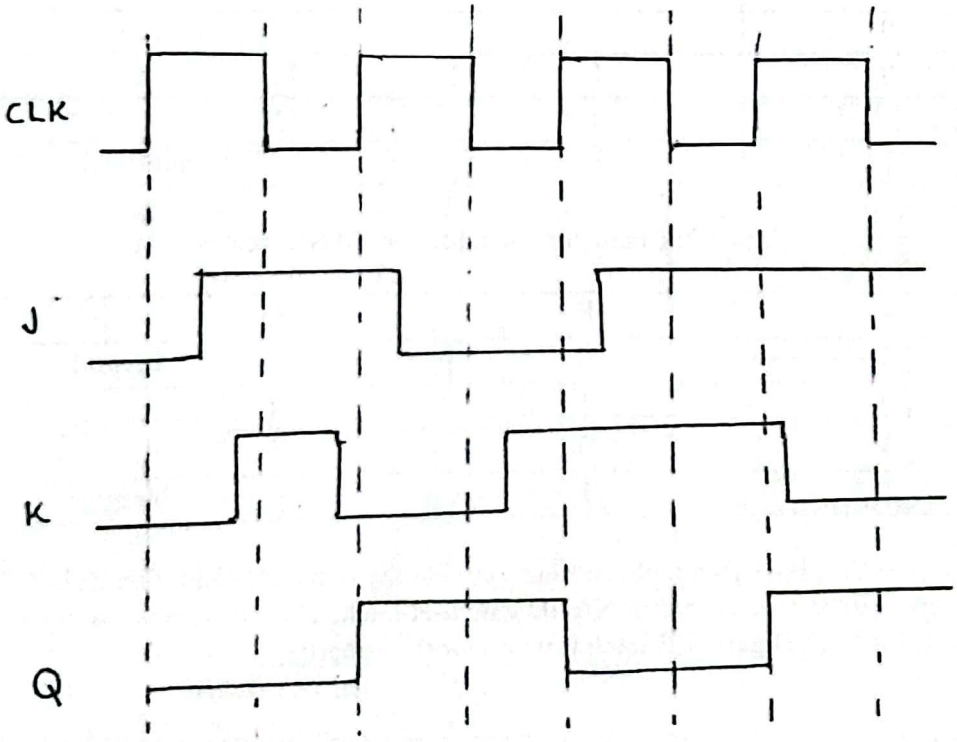


Figure 01: Output wave form for a JK flip flop

7. Operating time is fast
   Accuracy is high

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8.

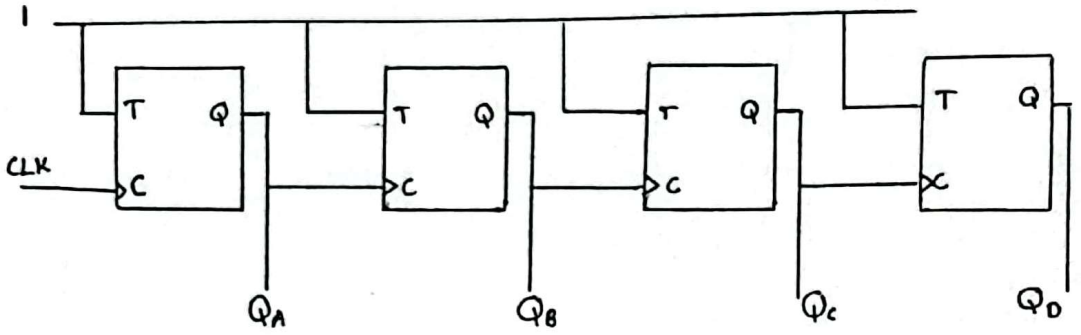


Figure 02: Circuit diagram for 4-bit asynchronous counter

9.

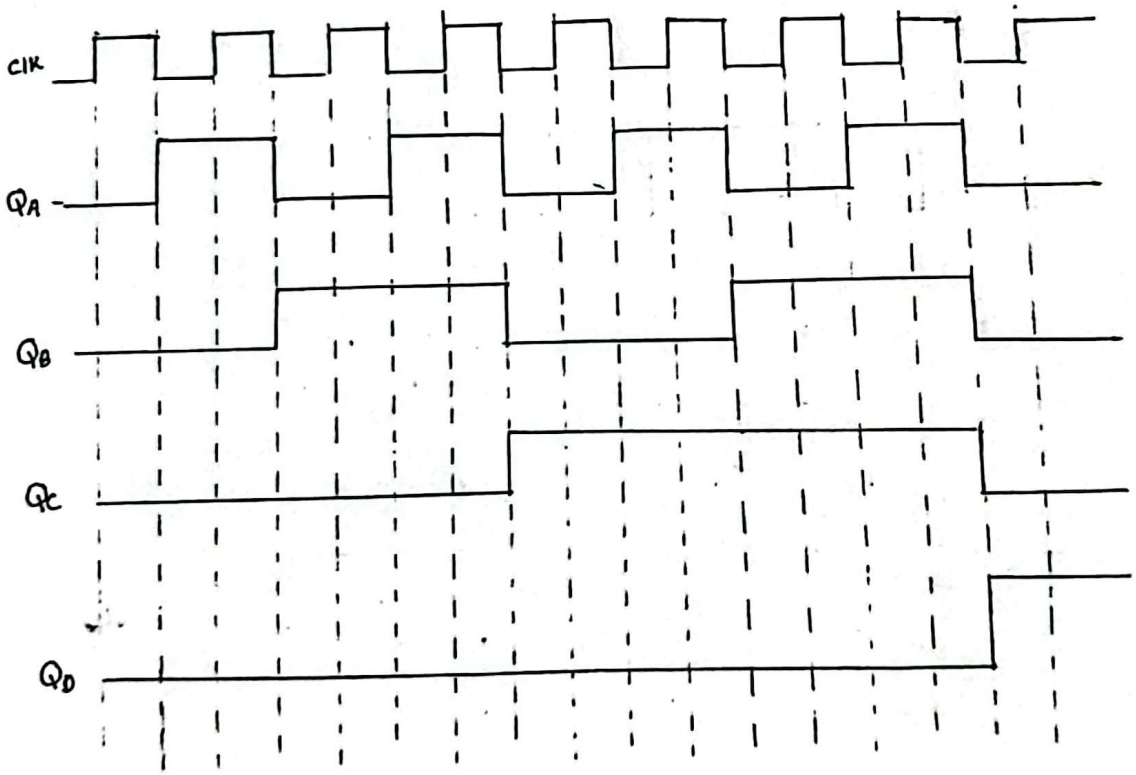


Figure 03: Timing diagram for each bit of the 4-bit asynchronous counter

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PRACTICAL WORK

**A. Basic transparent (D-type) Latches**

1.

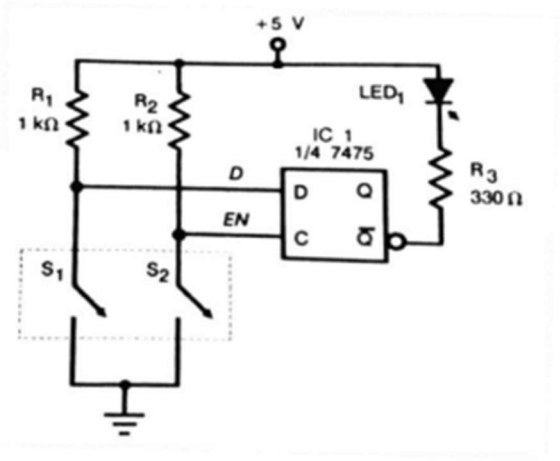


*Figure 3: Circuit of a basic transparent, D-type latch*

a) I. When ENABLE = 1 and D = 0 , Q = 0

II. When ENABLE =1 and D = 1 , Q =1

b) No

c)

Table 04: Function table of D type latch

| Input | | Output |
|---|---|---|
| Enable | D | $Q_{n+1}$ |
| 0 | X | $Q_n$ |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

## B. Introduction to J-K flip flop

1.

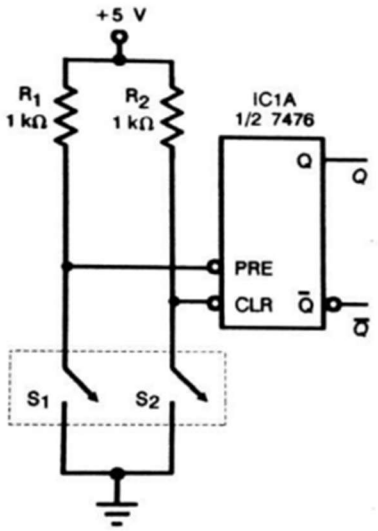


*Figure 4: Demonstrating the operation of the PRE and CLR inputs on a 7476 dual JK filp-flop.*

a)

Table 05: Data Table of PRE and CLR inputs operations

| $\overline{PRE}$ | $\overline{CLR}$ | Q | $\bar{Q}$ | Mode (SET /RESET /NO change) |
|---|---|---|---|---|
| 1 | 0 | 0 | 1 | RESET |
| 1 | 1 | 0 | 1 | NO change |
| 0 | 1 | 1 | 0 | SET |
| 1 | 1 | 1 | 0 | NO change |

2.

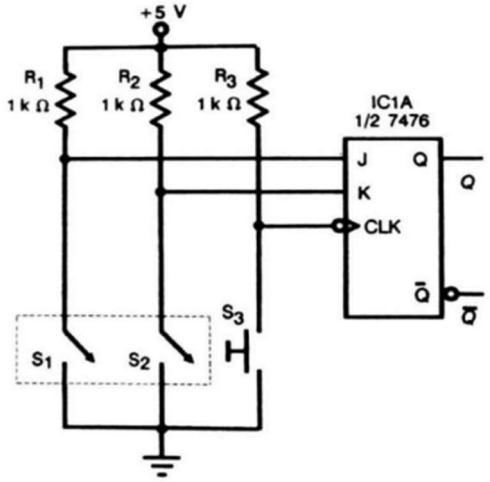


*Figure 5: Circuit diagram of the J and K inputs operation on a 7476 dual JK flip-flop.*

a)

Table 06 : Data table of J and K inputs operations

| J | K | CLK | Q | $\bar{Q}$ | Mode (SET /RESET /NO change) |
|---|---|---|---|---|---|
| 1 | 0 | ⎍ | 1 | 0 | SET |
| 1 | 1 | ⎍ | 1 | 0 | NO change |
| 0 | 1 | ⎍ | 0 | 1 | RESET |
| 1 | 1 | ⎍ | 0 | 1 | NO change |

## C. Ripple Counters

1.

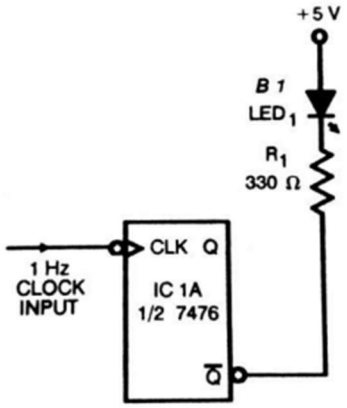


*Figure 6: Circuit of a 1-bit binary counter*

a)

Tabel 07: Data table of a one-bit binary counter

| Count (Decimal) | LED1(ON/OFF) | Q Output IC 1A(0,1) |
|---|---|---|
| 0 | OFF | 0 |
| 1 | ON | 1 |

b)

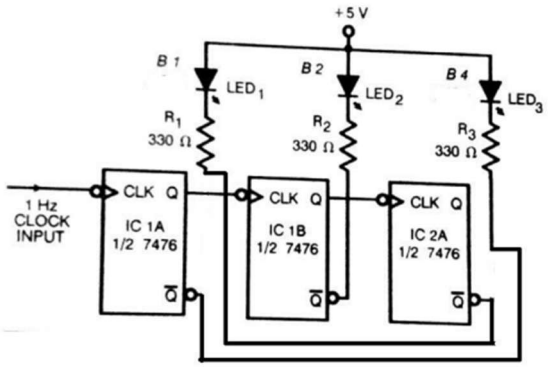


*Figure 7: Circuit of a 3-bit binary counter*

Table 08: Data table of a 3-bit binary counter

| COUNT(Decimal) | LED status (ON/OFF) | | | Q outputs (0/1) | | |
|---|---|---|---|---|---|---|
| | LED3 | LED2 | LED1 | IC 1A | IC 1B | IC 2A |
| 0 | OFF | OFF | OFF | 0 | 0 | 0 |
| 1 | ON | OFF | OFF | 0 | 0 | 1 |
| 2 | OFF | ON | OFF | 0 | 1 | 0 |
| 3 | ON | ON | OFF | 0 | 1 | 1 |
| 4 | OFF | OFF | ON | 1 | 0 | 0 |
| 5 | ON | OFF | ON | 1 | 0 | 1 |
| 6 | OFF | ON | ON | 1 | 1 | 0 |
| 7 | ON | ON | ON | 1 | 1 | 1 |

**D. Synchronous Binary Counter**

1.
a)

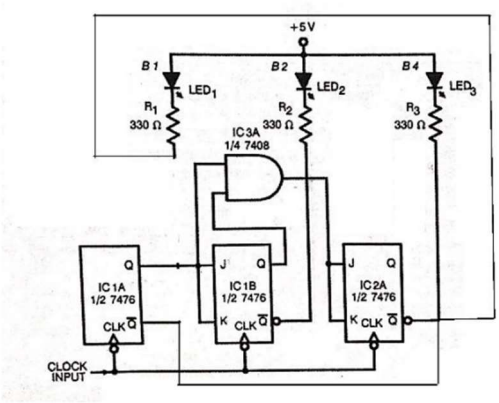


*Figure 8: 3-bit binary synchronous counter*

Table 09: Data table of a 3-bit binary synchronous counter

| COUNT(Decimal) | LED status (ON/OFF) | | | Q outputs (0/1) | | |
|---|---|---|---|---|---|---|
| | LED3 | LED2 | LED1 | IC 1A | IC 1B | IC 2A |
| 0 | OFF | OFF | OFF | 0 | 0 | 0 |
| 1 | ON | OFF | OFF | 1 | 0 | 0 |
| 2 | OFF | ON | OFF | 0 | 1 | 0 |
| 3 | ON | ON | OFF | 1 | 1 | 0 |
| 4 | OFF | OFF | ON | 0 | 0 | 1 |
| 5 | ON | OFF | ON | 1 | 0 | 1 |
| 6 | OFF | ON | ON | 0 | 1 | 1 |
| 7 | ON | ON | ON | 1 | 1 | 1 |