LOGIC FAMILIES

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PRELIMINARY WORK

01. CMOS has less power consumption and less power dissipation over TTL
CMOS has higher noise margin compared to TTL. The higher noise margin higher the accuracy of the output.

02. Fan out is the number of devices or inputs that one output can connect to and control without any performance distortion. Knowing the fan out helps ensure that the output is strong enough to work properly with all the devices it's connected without causing errors or weakening the signal.

03. I_{HIGH}= 7mA
I_{LOW}= 2mA
Supply voltage-5V

Average current (I_{AVG}) $= \frac{I_{HIGH}+I_{LOW}}{2}$

$= \frac{7mA+2mA}{2}$

$= 4.5$ mA

Average power drawn by IC = V× I_{AVG}

= 5V × 4.5mA

= 22.5 mW

04. Noise immunity is the ability of a circuit to operate correctly in the presence of electrical noise or interference. High noise immunity ensures reliable operation in real-world environments, reducing the risk of errors caused by external disturbances.

05.

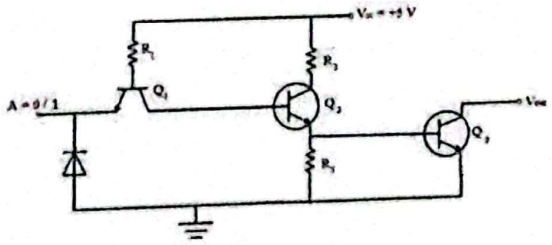

Figure 1: Open collector TTL NOT gate

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a.) When A= 0 means that in the transistor Q_1 , V_{BE} is in forward bias and V_{BC} in reversed biased. Q_2 and Q_3 also OFF that means they are in the cutoff mode. It is acts as a open circuit. Without a conducting path through the pull-up resistor R_3 can be used to bias the voltage. Therefore, when A=0, $v_{out} = 1$.

b.) When A=1 means that in the transistor Q_1, V_{BE} is in reversed bias. Therefore, the current flows through the Collector to base. That means Q_2 and Q_3 are switched ON. It is acts as an open circuit. Therefore v_{out} approximately equal to the v_{CC} at saturated mode. Therefore, when A=0, $v_{out} = 0$.

c.)

Table 01: Truth table of TTL NOT gate

A	Q_1(ON/OFF)	Q_2(ON/OFF)	Q_3(ON/OFF)	Output
0	ON	OFF	OFF	1
1	OFF	ON	ON	0

06. resolution is smallest change in analog input that can be detected by the ADC

07.

a.) Resolution (K) = $\frac{\text{full scale output}}{2^n - 1}$

$= \frac{5V}{2^8 - 1}$

= 0.01961 V

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b.)

Table 02: digital output for analog inputs

Input voltage(V)	ADC Value	Digital output
5	$\frac{5}{0.0196} = 255.10$	11111111
4.28	$\frac{4.28}{0.0196} = 218.37$	11011010
3.62	$\frac{3.26}{0.0196} = 166.33$	10111001
2.54	$\frac{2.54}{0.0196} = 129.59$	10000010
1.37	$\frac{1.37}{0.0196} = 69.90$	01000110
0.43	$\frac{0.43}{0.0196} = 21.94$	00010110
0	$\frac{0}{0.0196} = 0$	00000000

08.

a.) $n=2^m$

$4= 2^m$

$m = 2$

number of outputs = 2

b.)

Table 03: truth table for the priority encoder

Input				Output		
I_4	I_3	I_2	I_1	A	B	V
0	0	0	0	X	X	0
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1
1	X	X	X	1	1	1

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c.) Output A

I_4I_3 \ I_2I_1	00	01	11	10
00	X	0	0	0
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

$A = I_3 + I_4$

Output B

I_4I_3 \ I_2I_1	00	01	11	10
00	X	0	1	1
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

$B = I_4 + \overline{I_3} I_2$

V

I_4I_3 \ I_2I_1	00	01	11	10
00	0	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

$V = I_4 + I_3 + I_2 + I_1$

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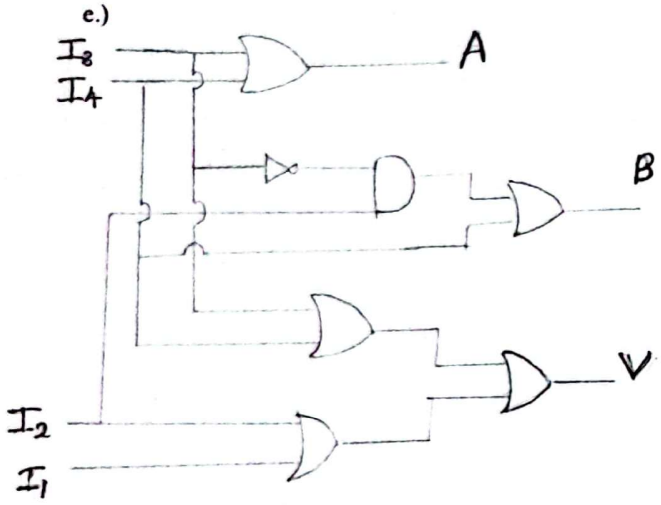
d.) A= $I_3 + I_4$

B= $I_4 + \overline{I_3} I_2$

V= $I_4 + I_3 + I_2 + I_1$

e.)



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PRACTICAL WORK

A. Open-collector TTL Outputs

1.

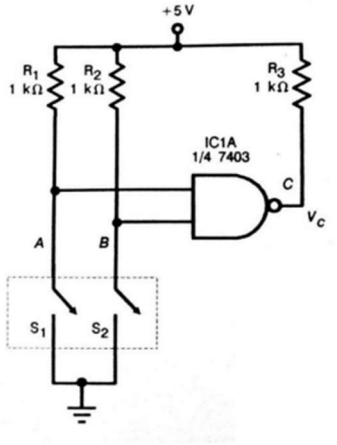

Figure 2 : Circuit diagram of a 2-input NAND gate with open-collector outputs.

b.

Table 04: Data table of a 2-input NAND gate with open -collector outputs

A	B	V_C(V)	I_C(mA)
0	0	4.354	0.646
0	1	4.352	0.648
1	0	4.359	0.641
1	1	0.3	4.7

c.

$$I_C \frac{V_{CC}-V_C}{R_3} = \frac{5V-V_C}{1k\Omega}$$

$$I_{C(max)} = \frac{5V-0.3V}{470\Omega} = 10mA$$

2.

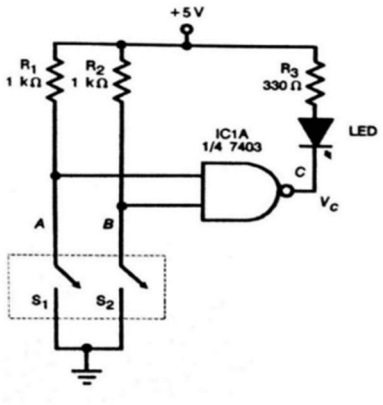

Figure 3 : Circuit diagram of a 2-input NAND gate with an open-collector output driving an LED

a. Table 05: Data table of a 2 input NAND gate with an open -collector output driving an LED

A	B	LED(ON/OFF)	V_C(V)	I_C(mA)
0	0	OFF	3.112	0
0	1	OFF	3.14	-84.848μA
1	0	OFF	3.103	27.272 μA
1	1	ON	0.353	8.360mA

b. V_{LED}=1.888V

c. $I_C = \frac{V_{CC}-V_{LED}-V_C}{R_3} = \frac{5V-1.888-V_C}{330\Omega}$

d. P = $I^2R = (8.36 \times 10^{-3})^2 \times 330$

= 0.0230W

3.

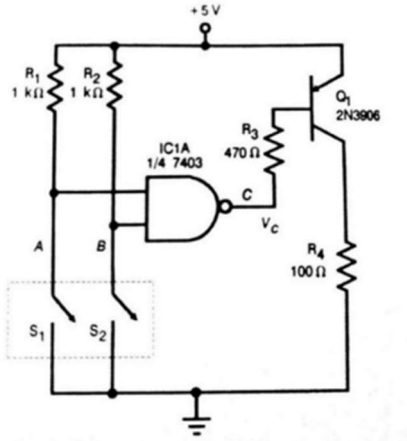

Figure 4 : Circuit diagram of a 2-input NAND gate with an open collector output driving a BJT current Amplifier.

Table 06: Data table of a 2 input NAND gate with an open collector output driving a BJT current amplifier

A	B	V_C(V)	V_{R4}(V)
0	0	3.829	0.0001
0	1	3.833	0.0001
1	0	3.825	0.0001
1	1	0.363	4.239

B. Using the CMOS ADC 0804 A/D Converter IC

1.

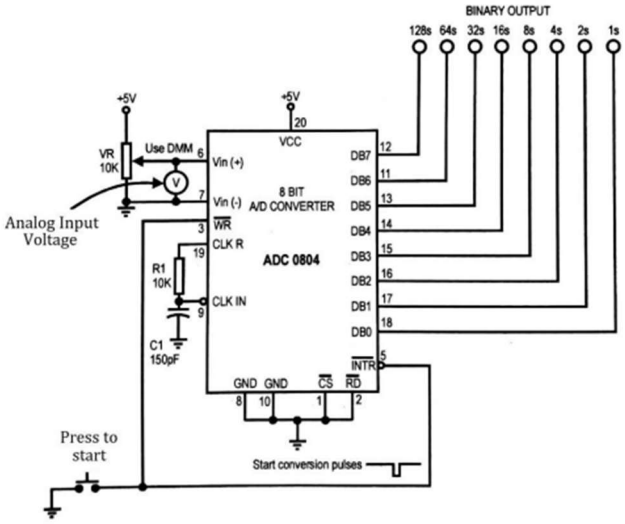

Figure 5: Analog to digital converter circuit.

a. Analogue input value =5V
   Binary output = 1111 1111

b. Analogue input value =0.02V
   Binary output = 0000 0001

c. The resolution of the converter is equal to the analog voltage corresponding to the LSB.

d. 0.02V resolution

e. 1. The ADC 0804 is an 8-bit A/D converter with binary outputs.
   2. The INTR output of the ADC 0804 IC emits a negative pulse at the end of each A/D conversion.
   3. Above pulse is feedback to the WR input to start the next analogue to digital conversion.

C. Decimal-to-binary Encoders and Binary-to-decimal Decoders

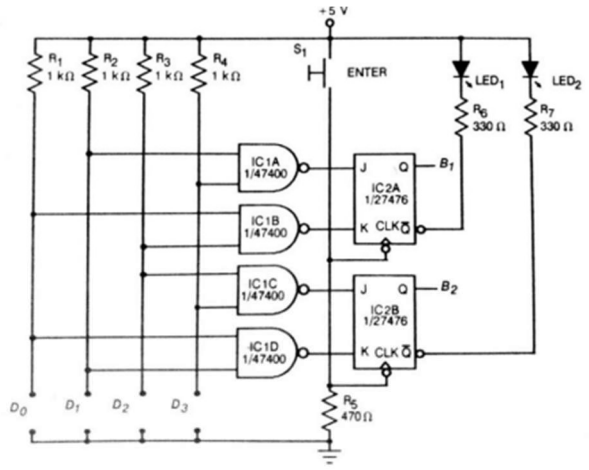

Figure 6: A 4-line decimal to binary encoder with latching output.

a. $J_1 = \overline{D_1 . D_3}$

$K_1 = \overline{D_0 . D_2}$

$J_2 = \overline{D_2 . D_3}$

$K_2 = \overline{D_0 . D_1}$

b. Table 07: Data table of a 4-line decimal to binary encoder with latching outputs

INPUTS					OUTPUTS					
D_3	D_2	D_1	D_0	ENTER	J_1	K_1	J_2	K_2	B_2	B_1
1	1	1	0	⎍	0	1	0	1	0	0
1	1	0	1	⎍	1	0	0	1	0	1
1	0	1	1	⎍	0	1	1	0	1	0
0	1	1	1	⎍	1	0	1	0	1	1
1	1	1	1	⎍	0	0	0	0	1	1

2.

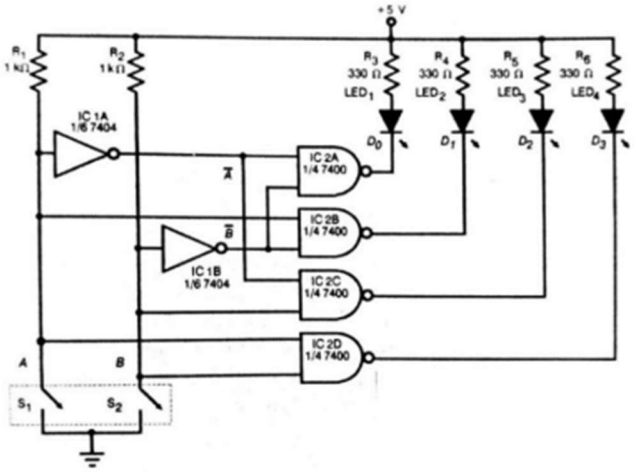

Figure 7: Decoder demonstration circuit

a. IC 2A = $\overline{\bar{A} \cdot \bar{B}}$
= A+ B

IC 2B = $\overline{A \cdot \bar{B}}$

IC 2C = $\overline{\bar{A} \cdot B}$

IC 2D = $\overline{A \cdot B}$

b. Table 08: truth table for decoder demonstration

B	A	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

c. Yes

d. A 2-to-4-line decoder operates by taking two input signals and using them to turn on one of its four outputs. The other three outputs stayed off. This behavior makes it a decoder and differentiates it from other types of digital circuits.