COMBINATIONAL LOGIC CIRCUITS

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PRELIMINARY WORK

① Table 1: Truth table of an exclusive-OR/exclusive-NOR gate

Input		Output	
		C	
A	B	XOR	XNOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

- XOR - even parity generator
  XNOR - odd parity generator

② i. Odd parity generator

This adds a special bit (called a parity bit) to the data to make sure the total number of 1s in the data is odd. it helps to detect errors when sending data

ii. Even parity generator

This adds a parity bit to the data to make sure the total number of 1s even. It also helps in catching errors during data transmission.

iii. Odd parity checker

This checks if the number of 1s in the received data is odd. If it is not odd, it means there might be an error in the data.

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iv. Even parity checker.

This checks if the number of 1s in the received data is even. If it is not even, it means there might be a mistake in the data.

③ i. Table 2: Truth table for parity generator with 3 bit inputs.

Input				A ⊕ B	C ⊕ S	Output
A	B	C	SEL			
0	0	0	0	0	0	0
0	0	0	1	0	1	1
0	0	1	0	0	1	1
0	0	1	1	0	0	0
0	1	0	0	1	0	1
0	1	0	1	1	1	0
0	1	1	0	1	1	0
0	1	1	1	1	0	1
1	0	0	0	1	0	1
1	0	0	1	1	1	0
1	0	1	0	1	1	0
1	0	1	1	1	0	1
1	1	0	0	0	0	0
1	1	0	1	0	1	1
1	1	1	0	0	1	1
1	1	1	1	0	0	0

ii. When SEL = 1 (ON) it works as an even parity generator

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④ i. Sending data over the internet. (Data transmission)
Memory Systems (RAM)

ii. Table 3: Truth table for a 4-bit even parity checker

A	B	C	P	Even parity check 1-Yes / 0-No
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

iii.

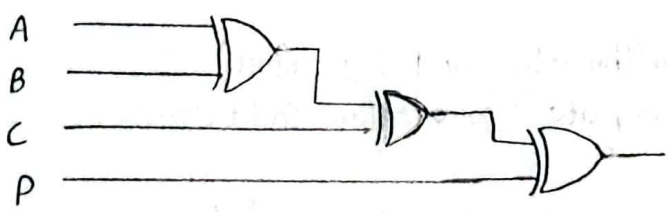

Figure 01: 4-bit even parity checker using 3XNOR gates

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⑤ Table 4: Truth table of a half adder

Input		Output	
A_0	B_0	S_0	C_0
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 5: Truth table of full adder

Input			Output	
A_0	B_0	C_{in}	S_0	C_0
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

(i) carry propagation delay

(ii) In ALU (arithmetic and logic unit)
To compute calculations (addition)

In audio processing, Digital Signal Processors use adders to combine signals in noise cancelling headphones. for cancelout external sounds, improving the quality of the audio output

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PRACTICAL WORK

A.Parity Circuits

1.

Table 06: Data table of the odd/even parity generator circuit

Input				Output
SEL	C	B	A	P
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

c) even parity generator

2. a) I. A ⊕ B

II.C⊕ GND

III. A⊕ B ⊕ C⊕ GND

IV.A⊕ B ⊕ C⊕ GND ⊕P

b)

Table 07: Data table on the odd/parity checker

Input				Output
P	C	B	A	CHK
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

B. Half Adders and Full Adders

1.a)

Table 08: Tuth table of half adder

Input		Output	
A_0	B_0	S_0	C_0
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

2.

Table 09: Truth table for full adder

Input			Output	
A_0	B_0	C_{in}	S_0	C_0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

a) $S_0=\overline{A_0}\ .\ \overline{B_0}\ .\ C_{in} + \overline{A_0}\ .B_0\ .\ \overline{C_{in}} + A_0.\ \overline{B_0}\ .\ \overline{C_{in}} + A_0\ .\ B_0\ .\ C_{in}$

$= \overline{A_0}\ (\overline{B_0}\ .\ C_{in} + B_0\ .\ \overline{C_{in}})\ + A_0(\ \overline{B_0}\ .\ \overline{C_{in}}\ + B_0\ .\ C_{in})$

$= \overline{A_0}\ (\ B_0 \oplus C_{in}\ ) + A_0\ (\ \overline{B_0 \oplus C_{in}})$

$= A_0 \oplus B_0 \oplus C_{in}$

b) $C_0= \overline{A_0}\ .\ B_0\ .\ C_{in} + A_0.\ \overline{B_0}\ .\ C_{in} + A_0\ .\ B_0.\ \overline{C_{in}} + A_0\ .\ B_0\ .\ C_{in}$

$= B_0\ .\ C_{in} + A_0.(\ B_0 \oplus C_{in})$

3.

Table 09: Truth table of a 2-bit adder

Input				Output		
A_1	A_0	B_1	B_0	C_1	S_1	S_0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	0	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0