

ECE 429 Introduction to VLSI

FALL 2020

FINAL PROJECT

Case Study for 32-bit Pipelined CPU Design with New ALU Architecture

By

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Objective:

The aim of the project is to design a pipelined CPU structure with various adders such as Carry Ripple Adder (CRA), Carry Lookahead Adder (CLA), Carry Skip Adder (CSA), and Carry Select Adder (CSeA). In addition, to design a 32-bit pipelined CPU with new ALU architecture using the comparator.

Introduction:

In this project a 32-bit pipelined CPU is explained along with the analysis of timing, area, number of cells and power for the four adder implementations mentioned above. As it is a pipelined processor, the execution of more than one instruction can be done at the same time parallelly. The components of CPU i.e. ALU, memory, are synchronized by the external clock. These components are positive edge triggered devices. The minimum operating period is decided by the critical path delay of the circuit. Therefore, we design a 32-bit pipelined circuit of CPU and synchronize the signals with critical path delay. The 32-bit CPU is designed by using adders, and a comparator. The performance and the path delays are analyzed. In Case Study 1, we are provided with Verilog files of Carry Ripple Adder, Carry Lookahead Adder, Carry Skip Adder and Carry Select Adder along with the source Verilog code and the test bench for the CPU design. This gives us the liberty to check the RTL SIMULATION, Logic Synthesis and Physical Synthesis. In Case Study 2, we add a 32-bit comparator block into the ALU design.

Theory:

The given figure gives an overview of the CPU block diagram. The primary building blocks are the memory files and ALU. The execution of the instruction takes place in 2 cycles. In the first cycle, the data is fetched from the memory using address A and address B. However, in the second cycle, ALU performs certain operation on the fetched data based on operation select signal such as addition, subtraction, multiplication, logical operations like AND, NOR, XNOR, XOR etc. The result is obtained by enabling the output tri-state buffer and the output is written back to memory at the word specified by Address B.

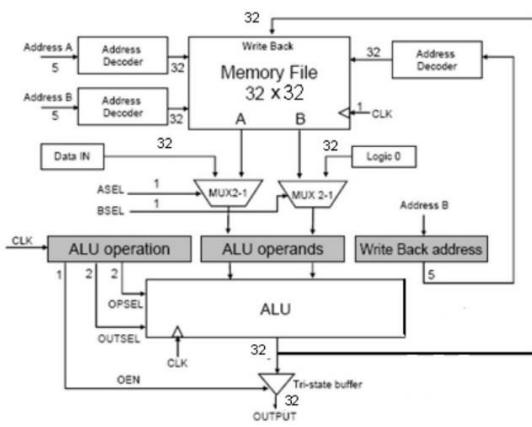


Fig 1: Circuit Overview.

Memory File:

The memory file of this design stores 32 32-bit words. There are two read ports and a write port in the memory file. The words to be read in each clock cycle are specified by the external 5-bit words address A and address B. A D-register is the primary storage element within the memory file. The output of each D-register is connected via tri-state buffers to the two output ports of the memory file.

ALU (Arithmetic Logic Unit):

The ALU of the circuit has two operands A and B and implements the following eight functions:

1. A+B – Addition
2. A-B – Subtraction
3. B-A – Subtraction
4. A*B – Multiplication
5. A OR B – Logic OR function
6. A AND B – Logic AND function
7. A XOR B – Logic XOR function
8. A XNOR B – Logic XNOR function

The below figure explains the architecture of the ALU. It has three activity blocks. They are Adder, Multiplier and the logic function block. The multiplier can be implemented as 32-by-32 array-based multiplier. Hence, to store the multiplication result back to memory file we need two clock cycles.

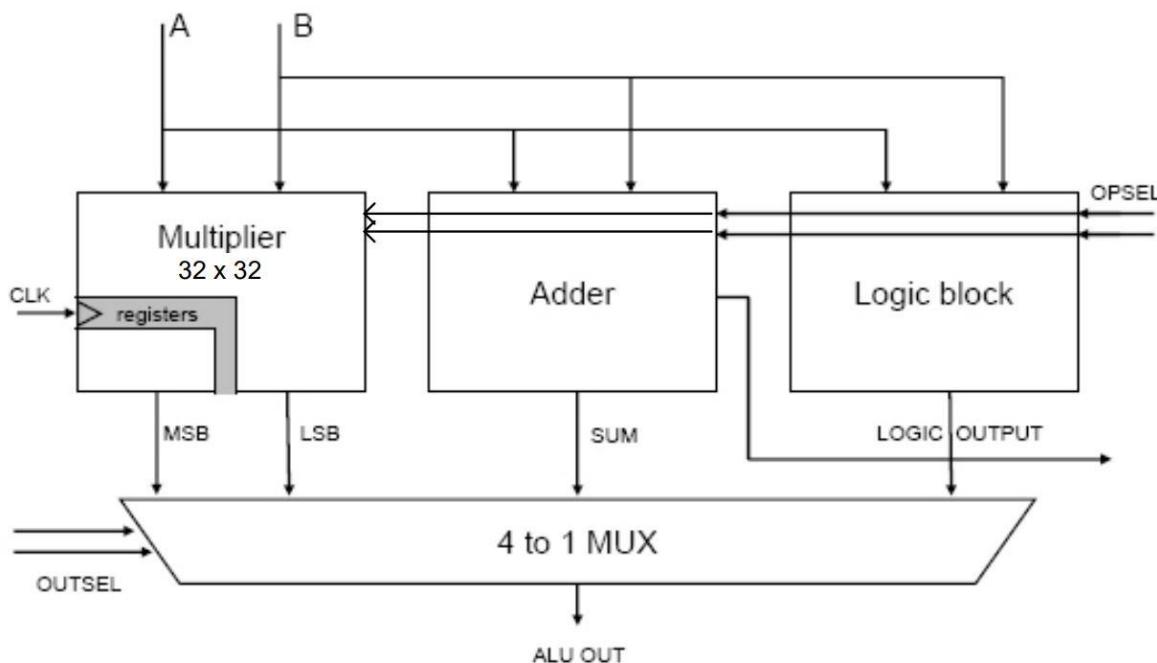


Fig 2: ALU Block Diagram.

Synchronization:

Let us consider an instruction word to understand better. After the clock turns high, the instruction is fetched to the signals that control the CPU operation. Since each instruction is executed in two steps. And few of these control signals must be stored at the internal registers of the CPU. Initially, the signals will specify the contents of the memory file which will be read from the read ports A and B. the control signals will determine the operation to be executed in the second cycle. The result of the ALU will be available if the OEN signal is set and is written back in the memory file. The address in memory where the ALU result is written is specified by the address B value. The information is composed that at the following positive edge of the clock signal.

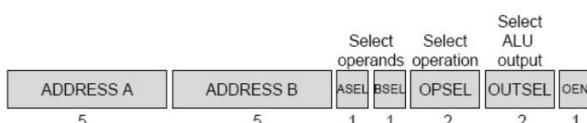


Fig 3: Instruction Word Contents.

Implementation:

The basic steps for the implementation of all adders and comparator from RTL to Post Synthesis Wave Generation are:

1. Verilog Code and Testbench:

A 32-bit CPU is designed for different adders by initially writing a Verilog code as cpu_xxx.v and also a testbench code tb_cpu.v to verify the functionality. In addition, a testbench tb_cpu.v is created according to the requirements. We perform the I/O operations so that the output is visible in the waveforms.

2. Logic Synthesis:

The RTL is converted into the gate level netlist cpu.vh. the compile_dc.tcl file has the necessary corrections.

3. P & R and Post Synthesis:

We use the encounter.tcl which has the gate level netlist and we use the cpu.vh file which has the interconnection and routing information which can be obtained from encounter.conf which has the circuit information.

4. Equivalence Checking:

In this, equivalence checking is performed between final.v and cpu.v. we have to perform this to resolve tool or manual errors.

1. Case Study 1:

In Case Study 1, different adders are implemented. RTL simulation, Post Synthesis Simulation, Post P&R Simulation and Equivalence Checking are done for all the cases and comparison of the results is done. The four kinds of adders used are Carry Ripple Adder, Carry Look Ahead Adder, Carry Skip Adder and Carry Select Adder. The testbench program and source Verilog programs are provided.

a. Carry Ripple Adder:

The following figures go through the implementation steps explained above.

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xterm

```

fa8 cra2(.sum(sum[23:16]), .c_out(c23), .a(a[23:16]), .b(b[23:16]), .c_in(c15));
      |
xmelab: *W,CUWNSP (./cpu_CRA.v,55917): 1 output port was not connected:
xmelab: (./cpu_CRA.v,524): over

      Top level design units:
          stimulus
      Building instance overlay tables: ..... Done
      Generating native compiled code:
          worklib.muliv <0x293149fe>
              streams: 32, words: 6720
          worklib,as32bitv <0xb2d02010>
              streams: 2, words: 420
          worklib,logic_fnv <0x5af3e3b5>
              streams: 1, words: 1113
          worklib,aluiv <0x612a0b00>
              streams: 1, words: 1246
          worklib,tristate_32iv <0x71d5a1b7>
              streams: 0, words: 0
          worklib,mux2to1iv <0x3f654099>
              streams: 0, words: 0
          worklib,mux2to1_32v <0x0d0009ec>
              streams: 0, words: 0
          worklib,memorystackv <0x9ba1896>
              streams: 1, words: 208
          worklib,dregiv <0x60a2e9c9>
              streams: 2, words: 264
      Building instance specific data structures.
      Loading native compiled code: ..... Done
      Design hierarchy summary:
      Instances Unique
      Modules: 6569 30
      Primitives: 7381 6
      Registers: 2166 14
      Scalar wires: 5536 -
      Expanded wires: 1198 41
      Vectorized wires: 6 -
      Always blocks: 2156 4
      Initial blocks: 3 3
      Cont. assignments: 1 6
      Pseudo assignments: 43 43
      Writing initial simulation snapshot: worklib.stimulus:v
      Loading snapshot worklib,stimulus:v ..... Done
xcelium> source /apps/cadence/XCELUMI803/tools/xsim/xcelium/files/xmsimrc
xcelium> run
xmsim: *W,SHMPOPT: Some objects excluded from $shm_probe due to optimizations,
      File: ./tb_cpu.v, line = 28, pos = 11
      Scope: stimulus
      Time: 0 FS + 0

Simulation complete via $finish(1) at time 501 NS + 0
./tb_cpu.v:30 #1 $finish;
xcelium> exit
stripura@uranus.ece.iit.edu:~% █ [Gmail - ece 429 - Mozilla Firefox]

```

Thunar (6) [Gmail - ece ...] [Blackboard L... xterm 22:12

Fig 4: RTL Simulation

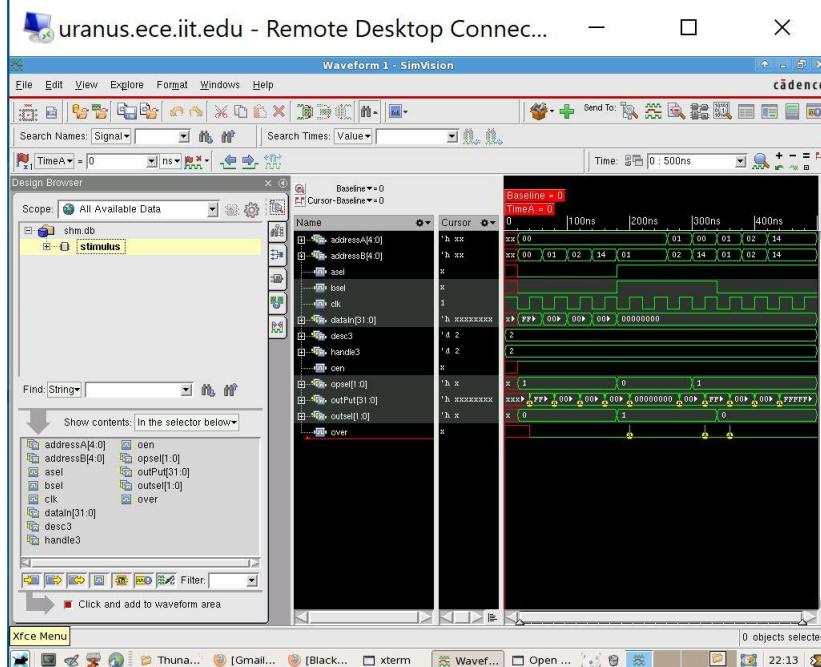


Fig 5: Waveforms in Simvision of RTL Simulation.

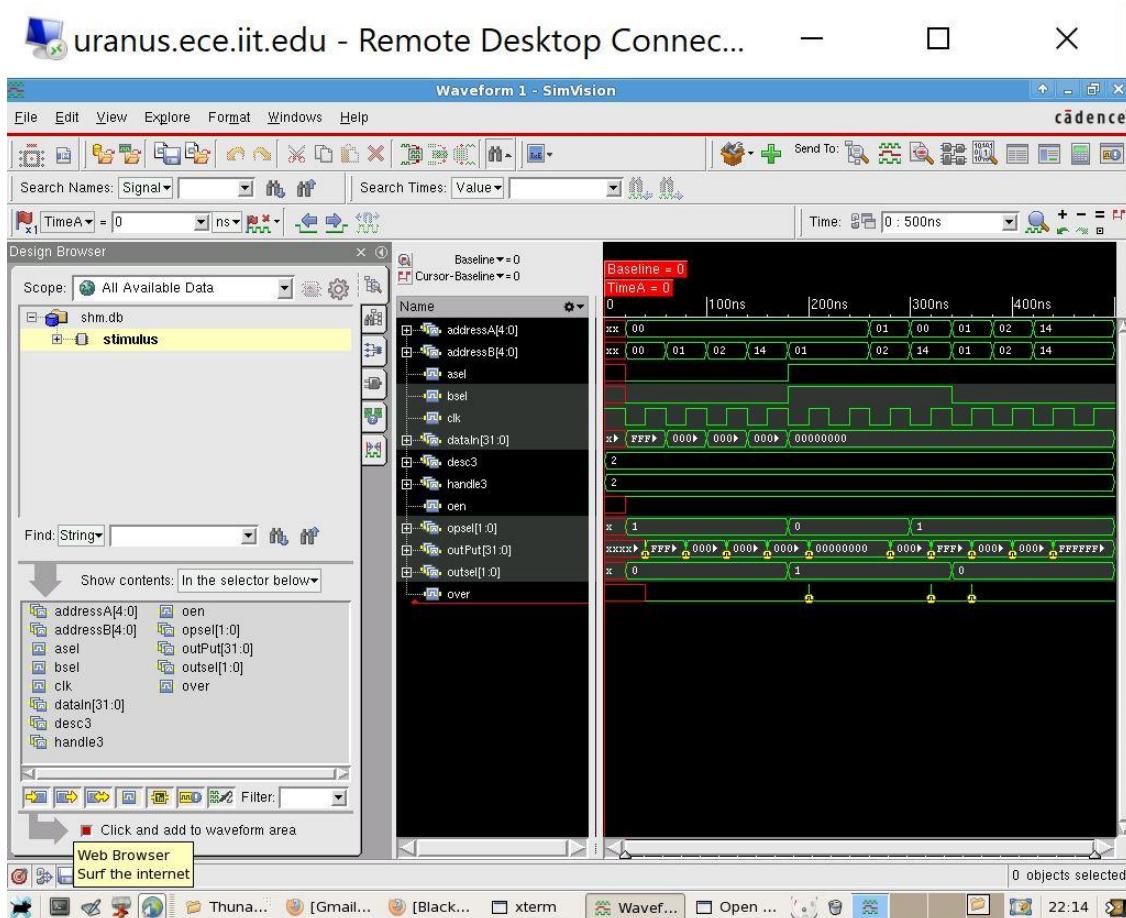


Fig 6: Complete Waveforms in Simvision of RTL Simulation.

```

Beginning Incremental Implementation Selection
-----
Beginning Delay Optimization Phase
-----
ELAPSED          WORST NEG TOTAL NEG DESIGN
TIME            AREA   SLACK    SLACK RULE COST
-----          -----
0:00:01        48597.4    0.00     0.0      2.9
0:00:02        48597.4    0.00     0.0      2.9
0:00:02        48597.4    0.00     0.0      2.9

Beginning Design Rule Fixing (max_capacitance)
-----
ELAPSED          WORST NEG TOTAL NEG DESIGN
TIME            AREA   SLACK    SLACK RULE COST
-----          -----
0:00:02        48597.4    0.00     0.0      2.9
Loading db file '/apps/FreePIK45/osu_soc/lib/files/gsc145nm.db'

Optimization Complete
-----
Warning: Design 'cpu' contains 1 high-fanout nets. A fanout number of 1000 will be used for delay calculations involving these nets. (TIN-134)
  Net 'clk': 1624 load(s), 1 driver(s)
1
check_design
1
#report_constraint -all_violators
set filename [format "%s%s" $my_toplevel ".vh"]
cpu.vh
write_f verilog -output $filename
Writing verilog file '/home/striplura/Desktop/ecd429/accu/cpu.vh'.
1
set filename [format "%s%s" $my_toplevel ".sdc"]
cpu.sdc
write_sdc $filename
1
#set filename [format "%s%s" $my_toplevel ".db"]
#write_f db -hier -output $filename -xg_force_db
redirect timing,rep { report_timing }
redirect cell,rep { report_cell }
redirect power,rep { report_power }
quit

```

Fig 7: Logic Synthesis using Design Compiler.

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timing.rep (~/Desktop/ece429/accu) - gedit

```

File Edit View Search Tools Documents Help
cell.rep x
a/l3/f256/U2/Y (XOR2X1) 0.00 3.84 r
a/l3/f265/U5/Y (XNOR2X1) 0.07 5.91 r
a/l3/f265/U2/Y (XOR2X1) 0.06 5.97 r
a/l3/f274/U5/Y (XNOR2X1) 0.07 6.04 r
a/l3/f274/U2/Y (XOR2X1) 0.06 6.11 r
a/l3/f274/U2/Y (XOR2X1) 0.07 6.18 r
a/l3/f283/U5/Y (XNOR2X1) 0.06 6.24 r
a/l3/f283/U2/Y (XOR2X1) 0.07 6.31 r
a/l3/f292/U5/Y (XNOR2X1) 0.06 6.37 r
a/l3/f292/U2/Y (XOR2X1) 0.07 6.44 r
a/l3/h301/U2/Y (XOR2X1) 0.04 6.48 f
a/u26/Y (A0I22X1) 0.03 6.52 r
U222/Y (BUFX2) 0.04 6.56 r
U65/Y (AND2X1) 0.06 6.61 r
U1787/Y (INVX1) 0.21 6.83 f
mb/ram/mer0/m0/m31/U3/Y (A0I22X1) 0.10 6.93 r
U3318/Y (INVX1) 0.02 6.95 f
mb/ram/mer0/ll/me31/qout_reg/D (DFFPOSX1) 0.00 6.95 f
data arrival time 6.95

clock clk (rise edge) 16.00 16.00
clock network delay (ideal) 0.00 16.00
mb/ram/mer0/ll/me31/qout_reg/CLK (DFFPOSX1) 0.00 16.00 r
library setup time -0.06 15.94
data required time 15.94
-----
data required time 15.94
data arrival time -6.95
-----
slack (MET) 8.99

1

```

Ln 16, Col 1 INS

Fig 8: timing.rep from synthesis of CRA.

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cell.rep (~/Desktop/ece429/accu) - gedit

```

File Edit View Search Tools Documents Help
cell.rep x
o/tr/t7/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t8/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t9/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t10/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t11/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t12/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t13/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t14/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t15/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t16/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t17/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t18/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t19/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t20/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t21/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t22/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t23/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t24/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t25/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t26/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t27/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t28/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t29/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t30/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t31/b1 TBUFX2 gscl45nm 3.754400 n
wb/bd/me0/qout_reg DFFPOSX1 gscl45nm 7.978100 n
wb/bd/me1/qout_reg DFFPOSX1 gscl45nm 7.978100 n
wb/bd/me2/qout_reg DFFPOSX1 gscl45nm 7.978100 n
wb/bd/me3/qout_reg DFFPOSX1 gscl45nm 7.978100 n
wb/bd/me4/qout_reg DFFPOSX1 gscl45nm 7.978100 n

Total 14381 cells 48597.421985
1

```

xterm Ln 1, Col 1 INS

Fig 9: cell.rep from synthesis of CRA.

```

uranus.ece.iit.edu - Remote Desktop Connec... - power.rep (~/Desktop/ece429/accu) - gedit
File Edit View Search Tools Documents Help
power.rep x
gscl45nm (File: /apps/FreePDK45/osu_soc/lib/files/gscl45nm.db)

Operating Conditions: typical Library: gscl45nm
Wire Load Model Mode: top

Global Operating Voltage = 1.1
Power-specific unit information :
  Voltage Units = 1V
  Capacitance Units = 1.000000pf
  Time Units = 1ns
  Dynamic Power Units = 1mW      (derived from V,C,T units)
  Leakage Power Units = 1nW

Cell Internal Power = 1.7076 mW (85%)
Net Switching Power = 302.0056 uW (15%)
Total Dynamic Power = 2.0096 mW (100%)
Cell Leakage Power = 260.9149 uW



| Power Group   | Internal Power | Switching Power | Leakage Power | Total Power | ( % )     | Attrs |
|---------------|----------------|-----------------|---------------|-------------|-----------|-------|
| io_pad        | 0.0000         | 0.0000          | 0.0000        | 0.0000      | ( 0.00%)  |       |
| memory        | 0.0000         | 0.0000          | 0.0000        | 0.0000      | ( 0.00%)  |       |
| black_box     | 0.0000         | 0.0000          | 0.0000        | 0.0000      | ( 0.00%)  |       |
| clock_network | 0.0000         | 0.0000          | 0.0000        | 0.0000      | ( 0.00%)  |       |
| register      | 1.4685         | 4.2972e-02      | 8.9282e+04    | 1.6007      | ( 70.50%) |       |
| sequential    | 0.0000         | 0.0000          | 0.0000        | 0.0000      | ( 0.00%)  |       |


Ln 1, Col 1 INS
[ec429 - File... [accu - File... xterm accu - File... power.re... xterm 15:56

```

Fig 10: power.rep from synthesis of CRA.

```

uranus.ece.iit.edu - Remote Desktop Connec... - xterm
file: cpu.vh
  module worklib.cpu;vh
    errors: 0, warnings: 0
    Caching library 'worklib' ..... Done
  Elaborating design hierarchy:
  Top level design units:
    A0I21X1
    BUFX4
    CLKBUF1
    CLKBUF2
    CLKBUF3
    DFFNEGEX1
    DFFSR
    FFX1
    HNX1
    INVX2
    INVX4
    INVX8
    LATCH
    MUX2X1
    MUX3X1
    NAND3X1
    NOR2X1
    OR12X1
    OR2X2
    TBUFX1
    stimulus
  Building instance overlay tables: ..... Done
  Generating native compiled code:
    worklib.cpu;vh (0x62175753)
      streams: 0, words: 0
  Building instance specific data structures.
  Loading native compiled code: ..... Done
  Design hierarchy summary:
    Instances Unique
    Modules: 14402 34
    UDPs: 1628 4
    Primitives: 29324 6
    Timing outputs: 14402 19
    Registerset: 1628 18
    Scalar wires: 16260 -
    Expanded wires: 46 5
    Always blocks: 1 1
    Initial blocks: 3 3
    Pseudo assignments: 9 9
    Timing checks: 9769 1625
    Simulation timescale: 10ps
  Writing initial simulation snapshot: worklib.A0I21X1:v
  Loading snapshot worklib.A0I21X1:v ..... Done
  xcclium> source /apps/cadence/XCELUM1803/tools/xcclium/files/xmsimrc
  xcclium> run
  Simulation complete via $finish(1) at time 501 NS + 0
  ./tb_cpu.v30 #1 $finish;
  xcclium> exit
  stipura@uranus.ece.iit.edu:"% "

```

Fig 11: Post Synthesis Simulation of CRA.

```

2020-Dec-03 16:02:20 (2020-Dec-03 22:02:20 GMT): 10%
2020-Dec-03 16:02:20 (2020-Dec-03 22:02:20 GMT): 15%
2020-Dec-03 16:02:20 (2020-Dec-03 22:02:20 GMT): 20%
2020-Dec-03 16:02:20 (2020-Dec-03 22:02:20 GMT): 25%
2020-Dec-03 16:02:20 (2020-Dec-03 22:02:20 GMT): 30%
2020-Dec-03 16:02:20 (2020-Dec-03 22:02:20 GMT): 35%
2020-Dec-03 16:02:20 (2020-Dec-03 22:02:20 GMT): 40%
2020-Dec-03 16:02:20 (2020-Dec-03 22:02:20 GMT): 45%
... Calculating internal and leakage power
2020-Dec-03 16:02:20 (2020-Dec-03 22:02:20 GMT): 50%
2020-Dec-03 16:02:21 (2020-Dec-03 22:02:21 GMT): 55%
2020-Dec-03 16:02:21 (2020-Dec-03 22:02:21 GMT): 60%
2020-Dec-03 16:02:21 (2020-Dec-03 22:02:21 GMT): 65%
2020-Dec-03 16:02:21 (2020-Dec-03 22:02:21 GMT): 70%
2020-Dec-03 16:02:21 (2020-Dec-03 22:02:21 GMT): 75%
2020-Dec-03 16:02:21 (2020-Dec-03 22:02:21 GMT): 80%
2020-Dec-03 16:02:21 (2020-Dec-03 22:02:21 GMT): 85%
2020-Dec-03 16:02:21 (2020-Dec-03 22:02:21 GMT): 90%
2020-Dec-03 16:02:22 (2020-Dec-03 22:02:22 GMT): 95%
Finished Calculating power
2020-Dec-03 16:02:22 (2020-Dec-03 22:02:22 GMT):
*

Total Power
-----
Total Internal Power: 5,342 55,682
Total Switching Power: 3,989 41,58%
Total Leakage Power: 0,2628 2,733%
Total Power: 9,593
-----
report_power consumed time (real time) 00:00:03 : peak memory (571M)
Output file is power.final
*****
* Encounter script finished *
* Results: *
* -----
* Layout: final.gds2 *
* Netlist: final.v *
* Timing: timing.rep.5.final *
* Area: area.final *
* Power: power.final *
* -----
* Type 'win' to get the Main Window *
* or type 'exit' to quit *
* -----
encounter 1> reportGateCount -limit 0
Gate area 2.81588 um2
[0] cpu Gates=15743 Cells=14456 Area=44330.5 um2
encounter 2> [accu - File Manager]

```

Fig 12: Area Report.

```

Total Power
-----
Total Internal Power: 5,342 55,682
Total Switching Power: 3,989 41,58%
Total Leakage Power: 0,2628 2,733%
Total Power: 9,593
-----
Group Internal Power Switching Power Leakage Power Total Power Percentage
-----
Sequential 2,495 0,2169 0,08928 2,801 29,19
Macro 0 0 0 0 0 0
IO 0 0 0 0 0 0
Combinational 2,733 2,548 0,1716 5,455 56,84
Clock (Combinational) 0,1142 1,223 0,001849 1,34 13,96
Clock (Sequential) 0 0 0 0 0 0
Total 5,342 3,989 0,2628 9,593 100
-----
Rail Voltage Internal Power Switching Power Leakage Power Total Power Percentage
-----
vdd 1.1 5,342 3,989 0,2628 9,593 100
-----
Clock Internal Power Switching Power Leakage Power Total Power Percentage
-----
clk 0,1142 1,223 0,001849 1,34 13,96
Total 0,1142 1,223 0,001849 1,34 13,96
-----
* Power Distribution Summary:
* Highest Average Power: clk_L4_15 (INV8): 0,01967
* Highest Leakage Power: mb/ram/mer2/11/we31/qout_reg (DFFPOSX1): 5,498e-05
* Total Caps: 1,8088e-10 F
* Total instances in design: 14456
* Total instances in design with no power: 0
* Total instances in design with no activity: 0
* Total Fillers and Decap: 0
-----
report_power consumed time (real time) 00:00:00 : peak memory (571M)
1
encounter 3> [ece429 - File Manager]

```

Fig 13: Power Report.

```

xrun: 18.03-s001: (c) Copyright 1995-2018 Cadence Design Systems, Inc.
File: final.v
  module worklib.cpuv;
    parameter integer warnings=0;
    Caching library 'worklib' ..... Done
  Elaborating the design hierarchy:
  Top level design units:
    A0I21X1
      BUFX4
      CLKBUF1
      CLKBUF2
      CLKBUF3
      INV4
      INV2
      INV4X
      LATCH
      NOR2X1
      NOR3X1
      NOR2X2
      NOR3X2
      OR12X1
      OR2X2
      TBUF4
      stimulus
    Building instance overlay tables: ..... Done
    Generating native compiled code:
      worklib.cpuv <0x01302ea7>
        streams: 0, words: 0
    Building instance specific data structures.
    Loading native compiled code: ..... Done
  Design hierarchy summary:
    Instances Unique
    Modules: 14476 34
    UDPs: 1628 4
    Primitives: 25358 6
    Timing outputs: 14476 19
    Registers: 1638 18
    Scalar wires: 16334 -
    Expanded wires: 46 5
    Always blocks: 1 1
    Init blocks: 3 3
    Pseudo assignments: 9 9
    Timing checks: 9769 1625
    Simulation timescale: 10ps
  Writing initial simulation snapshot: worklib.A0I21X1.v
Loading snapshot worklib.A0I21X1.v ..... Done
xcelium> source /apps/cadence/XCELUM1803/tools/xcelium/files/xsimrc
xcelium run
Simulation complete via $finish(1) at time 501 NS + 0
./tb_cpu.v30 # $finish;
xcelium> exit
stripura@uranus.ece.iit.edu:~% 

```

Fig 14: Post P&R Simulation.

Arrival	Required	Pin	Edge	Net	Cell	Delay
Time	Time					
0.340	1.952	m0pd/bb/me1/qout_reg/CLK	^	clk_L4_N12		
m0pd/bb/me1/qout_reg/0			v	R[1]	DFFPOSX1	0.252

Fig 15: timing.rep.5.final

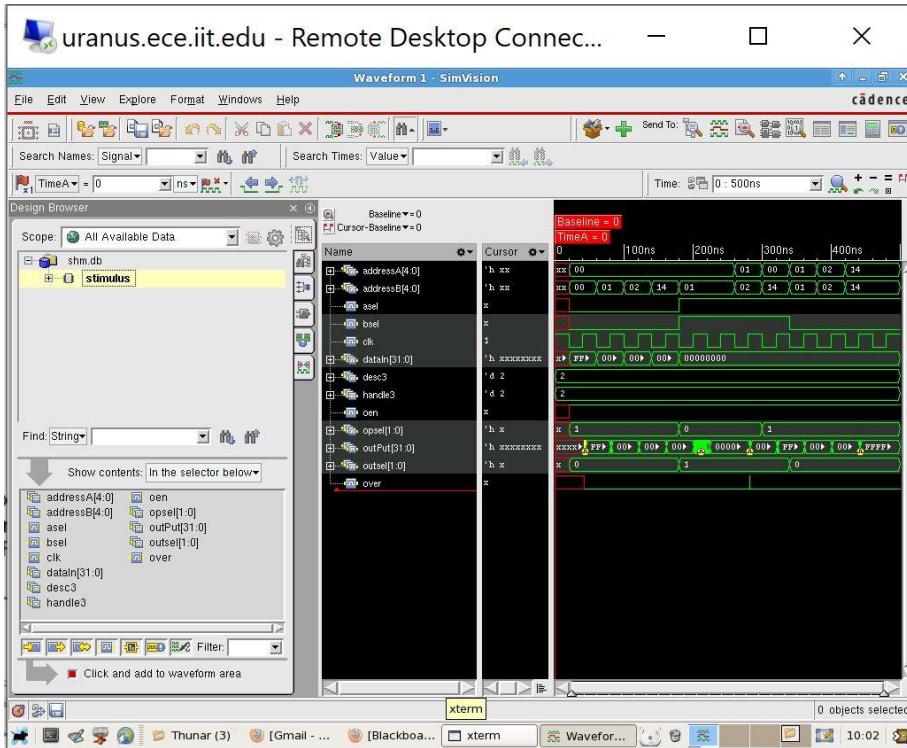


Fig 16: Waveforms of CRA Post P&R Simulation.

Encounter is mainly used to place the standard cells and route to the interconnects. The Verilog model output from encounter is used for post P&R simulation. Furthermore, from the output file timing.rep, required time (8.99) is obtained. Therefore, maximum clock frequency should be 11.123MHz.

b. Carry Lookahead Adder:

The following figures go through the implementation steps explained above.

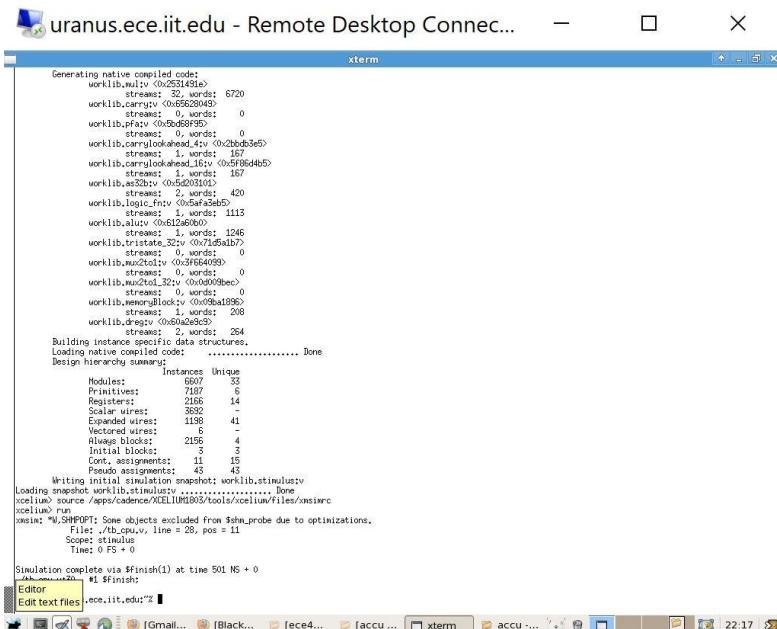


Fig 17: RTL simulation of CLA.

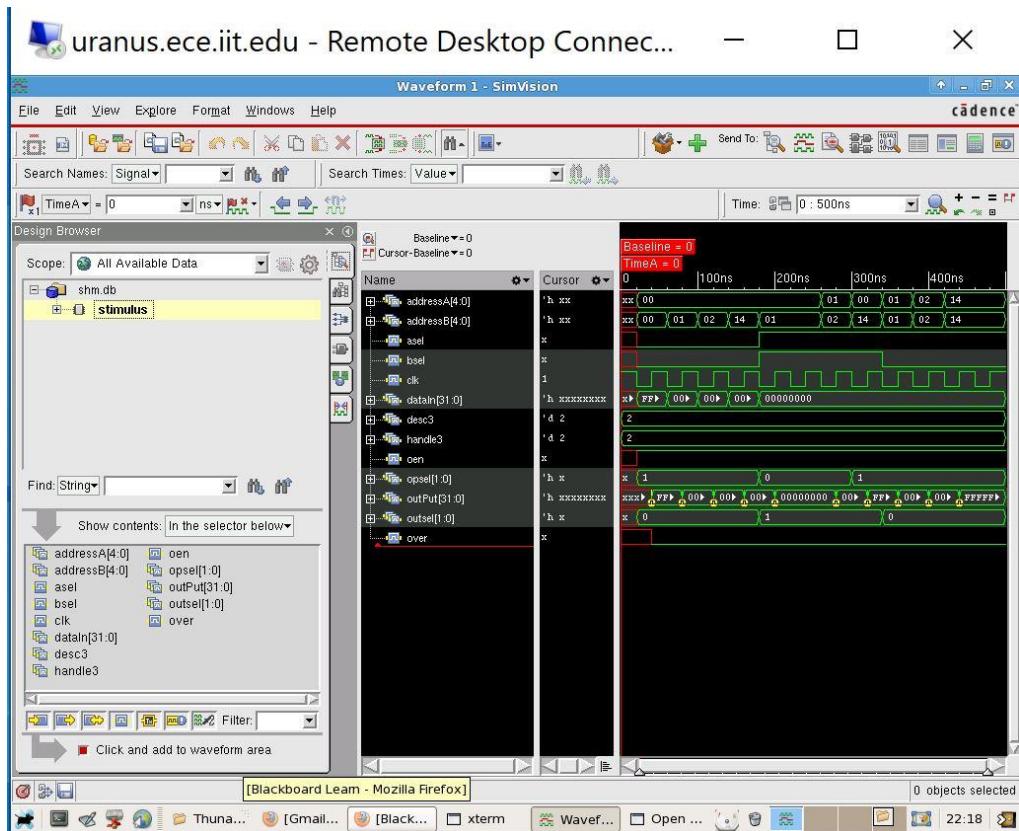


Fig 18: Waveforms of RTL Simulation of CLA.

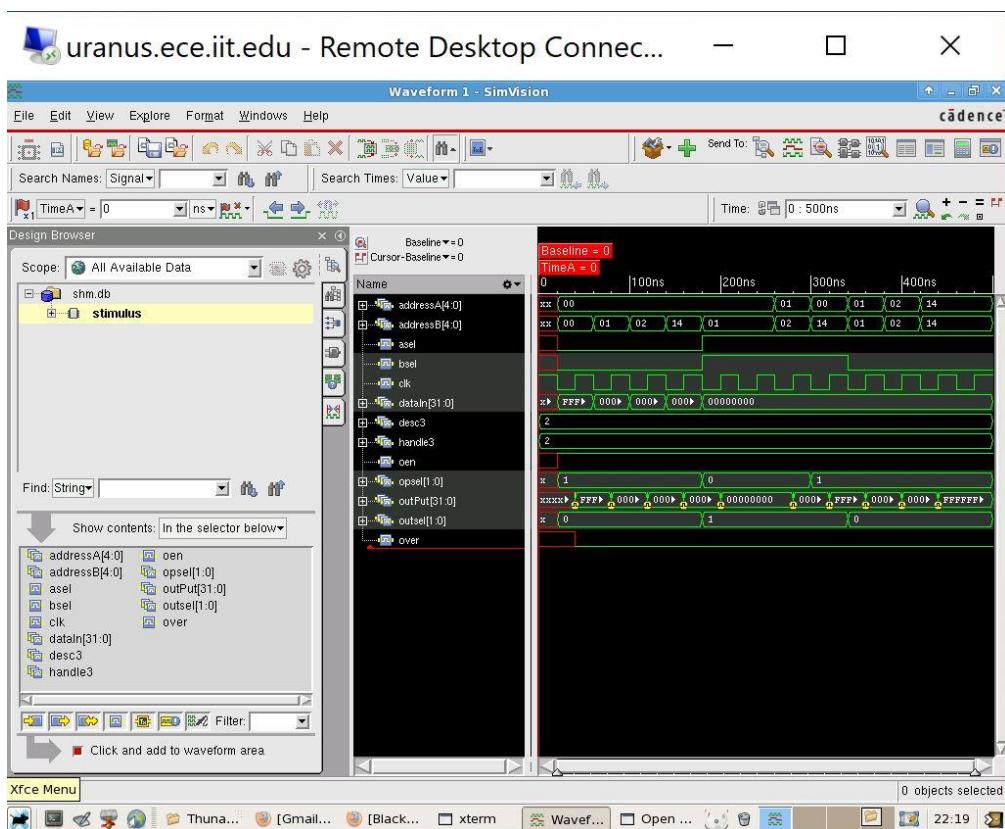


Fig 19: Complete Waveforms of RTL Simulation of CLA.

```

Beginning Mapping Optimizations (Medium effort) (Incremental)
-----
Beginning Incremental Implementation Selection
-----
Beginning Delay Optimization Phase
-----
ELAPSED      WORST NEG TOTAL NEG DESIGN
TIME        AREA SLACK SLACK RULE COST   ENDPOINT
-----|-----|-----|-----|-----|-----|
0:00:02    48572.1 0.00   0.0   3.0
0:00:03    48572.1 0.00   0.0   3.0
0:00:03    48572.1 0.00   0.0   3.0
-----
Beginning Design Rule Fixing (max_capacitance)
-----
ELAPSED      WORST NEG TOTAL NEG DESIGN
TIME        AREA SLACK SLACK RULE COST   ENDPOINT
-----|-----|-----|-----|-----|-----|
0:00:03    48572.1 0.00   0.0   3.0
Loading db file '/apps/FreePDK45/osu_soc/lib/files/gscl45nm.db'
Optimization Complete
Warning: Design 'cpu' contains 1 high-fanout nets. A fanout number of 1000 will be used for delay calculations involving these nets. (TIM-134)
Net 'clk'; 1624 load(s), 1 driver(s)
1
check_design
1
#report_constraint -all_violators
set filename [format "%xs%s" $my_toplevel ".vh"]
cpu.vh
write -f verilog -output $filename
Writing verilog file '/home/stripura/Desktop/ece429/accu/cpu.vh'.
1
set filename [format "%xs%s" $my_toplevel ".sdc"]
cpu.sdc
write_sdc $filename
1
#set filename [format "%xs%s" $my_toplevel ".db"]
#write_db -hier -output $filename -xg_force_db
redirect timing.rep { report_timing }
redirect cell.rep { report_cell }
redirect power.rep { report_power }
quit
Thank you...
Elapsed Time = 2:28.70, CPU Time = 146.441
stripura@uranus.ece.iit.edu:~$ 

```

Fig 20: Logic Synthesis using Design Compiler.

a/l3/f3027/U3/Y (INVX1)	0.04	0.02	f
U3457/Y (INVX1)	0.04	6.06	r
a/l3/f3028/U3/Y (0AI21X1)	0.04	6.10	r
U3459/Y (INVX1)	0.04	6.14	f
a/l3/f3029/U3/Y (0AI21X1)	0.04	6.18	r
U3767/Y (INVX1)	0.04	6.21	f
a/l3/f3030/U3/Y (0AI21X1)	0.04	6.26	r
U3768/Y (INVX1)	0.04	6.29	f
a/l3/f3031/U3/Y (0AI21X1)	0.04	6.33	r
U3461/Y (INVX1)	0.04	6.37	f
a/l3/f3032/U2/Y (XOR2X1)	0.03	6.40	f
a/U29/Y (A0I22X1)	0.05	6.45	r
U224/Y (BUFX2)	0.04	6.48	r
U67/Y (AND2X1)	0.06	6.54	r
U1237/Y (INVX1)	0.21	6.76	f
mb/ram/mer0/m0/m30/U3/Y (AOI22X1)	0.10	6.85	r
U3298/Y (INVX1)	0.02	6.88	f
mb/ram/mer0/ll/me30/qout_reg/D (DFFPOSX1)	0.00	6.88	f
data arrival time		6.88	

clock clk (rise edge)	15.00	15.00	
clock network delay (ideal)	0.00	15.00	
mb/ram/mer0/ll/me30/qout_reg/CLK (DFFPOSX1)	0.00	15.00	r
library setup time	-0.06	14.94	
data required time		14.94	

data required time		14.94	
data arrival time		-6.88	

slack (MET)		8.07	

1			

Fig 21: timing.rep from synthesis of CLA.

```

uranus.ece.iit.edu - Remote Desktop Connec...
File Edit View Search Tools Documents Help
cell.rep (~/Desktop/ece429/accu) - gedit
cell.rep x
o/tr/t7/c7/v1    TBUF2      gscl45nm   3.754400 n
o/tr/t8/b1        TBUFX2     gscl45nm   3.754400 n
o/tr/t9/b1        TBUFX2     gscl45nm   3.754400 n
o/tr/t10/b1       TBUFX2     gscl45nm   3.754400 n
o/tr/t11/b1       TBUFX2     gscl45nm   3.754400 n
o/tr/t12/b1       TBUFX2     gscl45nm   3.754400 n
o/tr/t13/b1       TBUFX2     gscl45nm   3.754400 n
o/tr/t14/b1       TBUFX2     gscl45nm   3.754400 n
o/tr/t15/b1       TBUFX2     gscl45nm   3.754400 n
o/tr/t16/b1       TBUFX2     gscl45nm   3.754400 n
o/tr/t17/b1       TBUFX2     gscl45nm   3.754400 n
o/tr/t18/b1       TBUFX2     gscl45nm   3.754400 n
o/tr/t19/b1       TBUFX2     gscl45nm   3.754400 n
o/tr/t20/b1       TBUFX2     gscl45nm   3.754400 n
o/tr/t21/b1       TBUFX2     gscl45nm   3.754400 n
o/tr/t22/b1       TBUFX2     gscl45nm   3.754400 n
o/tr/t23/b1       TBUFX2     gscl45nm   3.754400 n
o/tr/t24/b1       TBUFX2     gscl45nm   3.754400 n
o/tr/t25/b1       TBUFX2     gscl45nm   3.754400 n
o/tr/t26/b1       TBUFX2     gscl45nm   3.754400 n
o/tr/t27/b1       TBUFX2     gscl45nm   3.754400 n
o/tr/t28/b1       TBUFX2     gscl45nm   3.754400 n
o/tr/t29/b1       TBUFX2     gscl45nm   3.754400 n
o/tr/t30/b1       TBUFX2     gscl45nm   3.754400 n
o/tr/t31/b1       TBUFX2     gscl45nm   3.754400 n
wb/bd/me0/qout_reg DFFPOSX1 gscl45nm   7.978100 n
wb/bd/me1/qout_reg DFFPOSX1 gscl45nm   7.978100 n
wb/bd/me2/qout_reg DFFPOSX1 gscl45nm   7.978100 n
wb/bd/me3/qout_reg DFFPOSX1 gscl45nm   7.978100 n
wb/bd/me4/qout_reg DFFPOSX1 gscl45nm   7.978100 n
-----
Total 14363 cells          48572.079785
1

Xfce Menu
Ln 1, Col 1 INS
[Icons] [ece429 ...] [accu - Fil... xterm accu - Fil... cell.rep ... 16:54
```

Fig 22: cell.rep from synthesis of CLA.

```

power.rep (~/Desktop/ece429/accu) - gedit
File Edit View Search Tools Documents Help
power.rep x
wire Load Model Mode: top

Global Operating Voltage = 1.1
Power-specific unit information :
  Voltage Units = 1V
  Capacitance Units = 1.000000pf
  Time Units = 1ns
  Dynamic Power Units = 1mW   (derived from V,C,T units)
  Leakage Power Units = 1nW

Cell Internal Power = 1.8212 mW (85%)
Net Switching Power = 322.2322 uW (15%)
-----
Total Dynamic Power = 2.1435 mW (100%)
Cell Leakage Power = 261.3371 uW

          Internal      Switching      Leakage      Total
Power Group    Power        Power        Power      Power  ( % ) Attrs
-----+-----+-----+-----+-----+-----+-----+
io_pad        0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory        0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
clock_network 0.0000    0.0000    0.0000    0.0000 ( 0.00%)
register      1.5664    4.5838e-02  8.9282e+04  1.7015 ( 70.75%)
sequential     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
combinational 0.2549    0.2764    1.7204e+05  0.7033 ( 29.25%)
-----
Total         1.8212 mW    0.3222 mW   2.6133e+05 nW   2.4048 mW
1

Xfce Menu
Ln 1, Col 1 INS
[Icons] [ece429 ...] [accu - Fil... xterm accu - Fil... power.re... 16:55
```

Fig 23: power.rep from synthesis of CLA.

```

module worklib.cprvvh
  errors: 0, warnings: 0
  Caching library 'worklib' ..... Done
Elaborating the design hierarchy:
Top level design units:
  BUFX4
  CLKBUF1
  CLKBUF2
  CLKBUF3
  DFFBUF
  DFFNEGEX1
  DFFSR
  FDX1
  HAX1
  INVX2
  INVX4
  INVX8
  LATCH
  MUX2X1
  NMOS2X1
  NOES2X1
  OR2X2
  TBUFX1
  stimulus
Building instance overlay tables: ..... Done
Generating native compiled code:
  worklib.cprvvh <0x1fc78e4>
    streams: 0, words: 0
  worklib.stimulusiv <0x416cb96f>
    streams: 13, words: 17664
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
  Instances Unique
  Modules: 14383 34
  UDPs: 1628 4
  Primitives: 25230 6
  Timing outputs: 14383 19
  Registers: 1638 18
  Scalar wires: 16241 -
  Enabled blocks: 46 5
  Always blocks: 1 1
  Initial blocks: 3 3
  Pseudo assignments: 9 9
  Timing checks: 9769 1625
  Simulation timescale: 10ps
Writing initial simulation snapshot: worklib.BUFX4.v
Loading snapshot worklib.BUFX4.v..... Done
xcelium> source /apps/cadence/XCELUM1803/tools/xcelium/files/xmsimrc
xcelium> run
Simulation complete via $finish(1) at time 501 NS + 0
./tb_cprv.v:30  #! $finish;
xcelium> exit
strip@uranus.ece.iit.edu:~% 

```

Fig 24: Post Synthesis Simulation.

```

2020-Dec-03 17:00:00 (2020-Dec-03 23:00:00 GMT): 10%
2020-Dec-03 17:00:00 (2020-Dec-03 23:00:00 GMT): 15%
2020-Dec-03 17:00:00 (2020-Dec-03 23:00:00 GMT): 20%
2020-Dec-03 17:00:00 (2020-Dec-03 23:00:00 GMT): 25%
2020-Dec-03 17:00:00 (2020-Dec-03 23:00:00 GMT): 30%
2020-Dec-03 17:00:00 (2020-Dec-03 23:00:00 GMT): 35%
2020-Dec-03 17:00:00 (2020-Dec-03 23:00:00 GMT): 40%
2020-Dec-03 17:00:00 (2020-Dec-03 23:00:00 GMT): 45%
... Calculating internal and leakage power
2020-Dec-03 17:00:01 (2020-Dec-03 23:00:01 GMT): 50%
2020-Dec-03 17:00:01 (2020-Dec-03 23:00:01 GMT): 55%
2020-Dec-03 17:00:01 (2020-Dec-03 23:00:01 GMT): 60%
2020-Dec-03 17:00:01 (2020-Dec-03 23:00:01 GMT): 65%
2020-Dec-03 17:00:01 (2020-Dec-03 23:00:01 GMT): 70%
2020-Dec-03 17:00:01 (2020-Dec-03 23:00:01 GMT): 75%
2020-Dec-03 17:00:01 (2020-Dec-03 23:00:01 GMT): 80%
2020-Dec-03 17:00:02 (2020-Dec-03 23:00:02 GMT): 85%
2020-Dec-03 17:00:02 (2020-Dec-03 23:00:02 GMT): 90%
2020-Dec-03 17:00:02 (2020-Dec-03 23:00:02 GMT): 95%
Finished Calculating power
2020-Dec-03 17:00:02 (2020-Dec-03 23:00:02 GMT)
*

Total Power
-----
Total Internal Power: 5,607 55,49%
Total Switching Power: 4,235 41,91%
Total Leakage Power: 0,2634 2,6072
Total Power: 10,11
-----
report_power consumed time (real time) 00:00:03 : peak memory (570M)
Output file is power.final
*****
* Encounter script finished *
* Results: *
* -----
* Layout: final.gds2 *
* Netlist: final.v *
* Timing: timing.rep.5.final *
* Area: area.final *
* Power: power.final *
* -----
* Type 'win' to get the Main Window *
* or type 'exit' to quit *
* -----
encounter 1> reportGateCount -limit 0
Gate area 2,8198 um^2
[0] cpu Gates=15745 Cells=14448 Area=44336,6 um^2
encounter 2> 

```

Fig 25: Area Report.

uranus.ece.iit.edu - Remote Desktop Connec... — □ X

xterm

```
Total Power
-----
Total Internal Power: 5,607 55.49%
Total Switching Power: 4,235 41.91%
Total Leakage Power: 0,2634 2,6072
Total Power: 10,11

Group           Internal   Switching   Leakage   Total   Percentage
                  Power      Power      Power     Power (%) 
-----
Sequential        2,606     0,233    0,08928    2,929    28,98
Macro            0         0         0          0         0
IO               0         0         0          0         0
Combinational    2,899     2,69     0,1721     5,761    57,01
Clock (Combinational) 0,1017   1,312    0,002084   1,416    14,01
Clock (Sequential)   0         0         0          0         0
Total             5,607     4,235    0,2634    10,11    100

Rail            Voltage   Internal   Switching   Leakage   Total   Percentage
                  Power      Power      Power     Power (%) 
-----
vdd              1,1       5,607     4,235    0,2634    10,11    100

Clock           Internal   Switching   Leakage   Total   Percentage
                  Power      Power      Power     Power (%) 
clk              0,1017   1,312    0,002084   1,416    14,01
Total             0,1017   1,312    0,002084   1,416    14,01

* Power Distribution Summary:
* Highest Average Power: clk_L4_140 (INVX8); 0.02077
* Highest Leakage Power: tb/rax/mer2/11/we31/out_reg (DFFPUSX1); 5.498e-05
* Total Fills: 70956<-10 P
* Total Instances in design: 14448
* Total Instances in design with no power: 0
* Total Instances in design with no activity: 0
* Total Fillers and Decap: 0

report_power_consumed_time (real time) 00:00:00 : peak memory (570M)
```

1 Web Browser
encounter Surf the internet

[ece429 - File... [accu - File M... xterm accu - File Ma... 17:01 |

Fig 26: Power Report.

uranus.ece.iit.edu - Remote Desktop Connec... — □ X

xterm

```
striprupa@uranus.ece.iit.edu:~% gedit timing.rep.5.final
striprupa@uranus.ece.iit.edu:~% xrun gsc14sw_v_tb_cpu.v final.v +access+r
xrun: 18.03-s001: (c) Copyright 1995-2018 Cadence Design Systems, Inc.
file: final.v
module worklib.cpu;
  errors: 0, warnings: 0
  Caching library 'worklib' ..... Done
  Elaborating the design hierarchy;
  Top level design units:
    BUFX4
    CLKBUFL
    CLKBUFL2
    CLKBUFL3
    DFFNEXGXL
    DFFSR
    PRX1
    HXL1
    INV2
    LATCH
    MUX2X1
    NAN03X1
    NOR3X1
    OR122X1
    OR22
    TBUF24
    stimulus
  Building instance overlay tables: ..... Done
  Generating native compiled code;
  worklib.cpu:v (<0xe56d6c0>)
    streams: 0, words: 0
  Building instance specific data structures.
  Loading native compiled code: ..... Done
  Design hierarchy summary:
    Instances Unique
  Modules: 14466 34
  UDPs: 1628 4
  Primitives: 25313 6
  Timing outputs: 14466 19
  Registers: 1638 18
  Scalar wires: 16324 -
  Expanded wires: 46 5
  Alias wires: 1
  Initial blocks: 3 3
  Pseudo assignments: 9 9
  Timing checks: 9769 1625
  Simulation timescale: 10ps
  Writing initial simulation snapshot: worklib.BUFX4.v
Loading snapshot worklib.BUFX4.v ..... Done
xcelium> source /apps/cadence/XCELLUM1803/tools/xcelium/files/xmsimrc
xcelium> run
Simulation complete via $finish(1) at time 501 NS + 0
/tb.cpu.v:30  #1 $finish;
xcelium> exit
striprupa@uranus.ece.iit.edu:~%
```

[ece429 - File... [accu - File M... xterm accu - File Ma... 17:03 |

Fig 27: Post P&R Simulation.

```

uranus.ece.iit.edu - Remote Desktop Connec... - X
timing.rep.5.final (~/Desktop/ece429/accu) - gedit
File Edit View Search Tools Documents Help
timing.rep.5.final x
#####
# Generated by: Cadence Encounter 10.13-s292_1
# OS: Linux x86_64(Host ID uranus.ece.iit.edu)
# Generated on: Thu Dec 3 16:59:45 2020
# Design: cpu
# Command: report_timing -nworst 10 -net > timing.rep.5.final
#####
Path 1: MET Setup Check with Pin mb/ram/mer31/l1/me31/qout_reg/CLK
Endpoint: mb/ram/mer31/l1/me31/qout_reg/D (^) checked with leading edge of
'clk'
Beginpoint: m0pd/bb/me2/qout_reg/Q      (v) triggered by leading edge of
'clk'
Other End Arrival Time      0.321
- Setup                  3.951
+ Phase Shift            15.000
= Required Time          11.370
- Arrival Time           11.291
= Slack Time             0.079
    Clock Rise Edge      0.000
    + Clock Network Latency (Prop) 0.330
    = Beginpoint Arrival Time 0.330

+-----+
|   Pin          | Edge | Net        | Cell     | Delay |
| Arrival | Required |       |          |          |          |
Time   | Time       |       |          |          |          |
|-----+-----+-----+-----+-----+-----+
| m0pd/bb/me2/qout_reg/CLK | ^ | clk_L4_N1 |          |          |
0.330 | 0.409 |          |          |          |          |
| m0nd/bb/me2/qout_reg/Q | v | R121    | DEFPASX1 | 0.283 |
+-----+-----+-----+-----+-----+
Ln 1, Col 1 INS

```

Fig 28: timing.rep.5.final.

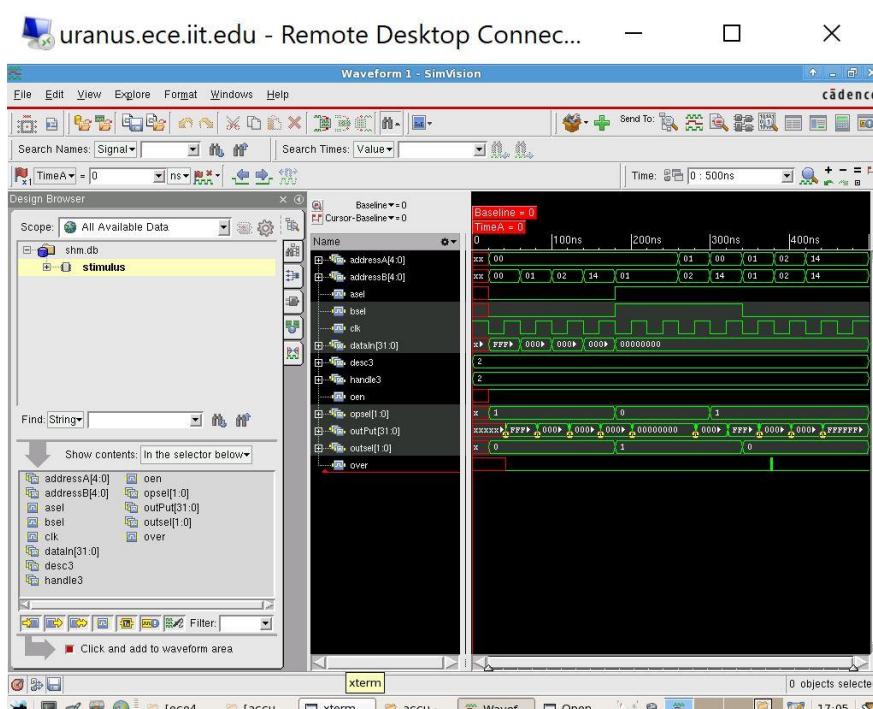
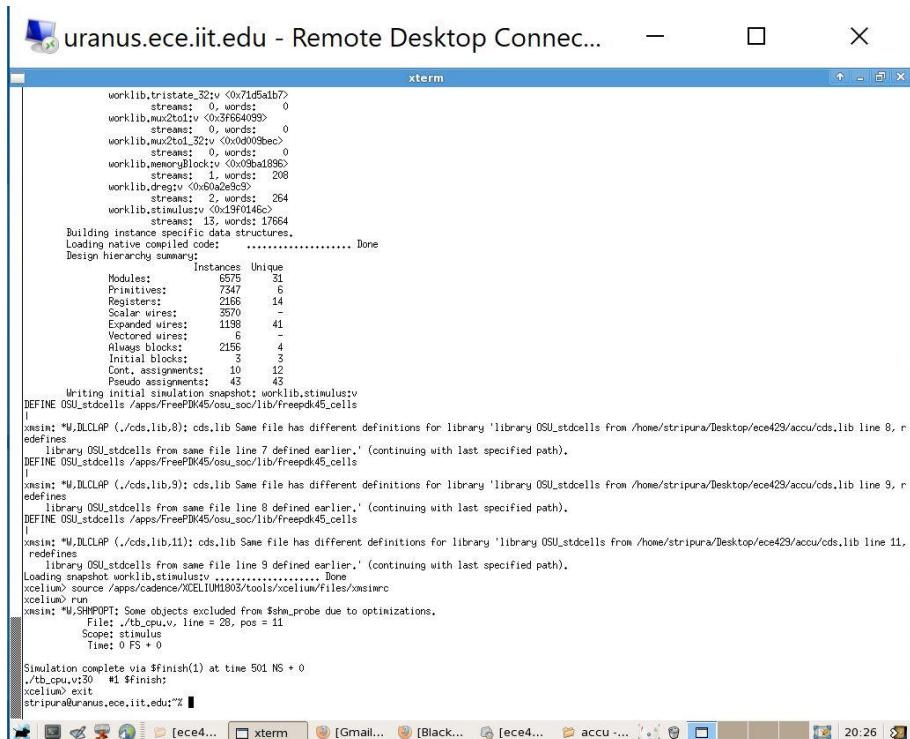


Fig 29: Waveforms Post P&R Simulation.

Encounter is mainly used to place the standard cells and route to the interconnects. The Verilog model output from encounter is used for post P&R simulation. Furthermore, from the output file timing.rep, required time (8.07) is obtained. Therefore, maximum clock frequency should be 12.391MHz.

c. Carry Skip Adder:

The following figures go through the implementation steps explained above.



```

uranus.ece.iit.edu - Remote Desktop Connec... xterm
xterm
worklib.tristate_32xv <0x7d5a1b>
streams: 0 words: 0
worklib.mux2to1v <0x3f664099>
streams: 0 words: 0
worklib.mux2to1_32v <0x0d019bec>
streams: 0 words: 0
worklib.mux2to1_block <0x0e0a199c>
streams: 1 words: 208
worklib.dregv <0x6a2a9c9>
streams: 2 words: 264
worklib.stimulusv <0x19f014c>
streams: 3 words: 17664
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
      Instances Unique
      Modules:      189       31
      Primitives:   7247       6
      Registers:    2166      14
      Scalar wires: 3570      14
      Expanded wires: 1198      41
      Vectorized wires: 6
      Initial blocks: 255       4
      Initial blocks: 3         3
      Cont. assignments: 10       12
      Pseudo assignments: 43       43
Writing initial simulation snapshot: worklib,stimulusv
DEFINE OSU_stdcells /apps/FreelDK45/osu_soc/lib/freeldk45_cells
|> xsim: #ULCLCP (.cds.lib,8): cds.lib Same file has different definitions for library 'library OSU_stdcells from /home/stripura/Desktop/ece429/accu/cds.lib line 8, r
defines
|> library OSU_stdcells from same file line 7 defined earlier.' (continuing with last specified path).
|> DEFINE OSU_stdcells /apps/FreelDK45/osu_soc/lib/freeldk45_cells
|> xsim: #ULCLCP (.cds.lib,9): cds.lib Same file has different definitions for library 'library OSU_stdcells from /home/stripura/Desktop/ece429/accu/cds.lib line 9, r
defines
|> library OSU_stdcells from same file line 8 defined earlier.' (continuing with last specified path).
|> DEFINE OSU_stdcells /apps/FreelDK45/osu_soc/lib/freeldk45_cells
|> xsim: #ULCLCP (.cds.lib,11): cds.lib Same file has different definitions for library 'library OSU_stdcells from /home/stripura/Desktop/ece429/accu/cds.lib line 11,
reddefines
|> library OSU_stdcells from same file line 9 defined earlier.' (continuing with last specified path).
Loading snapshot worklib,stimulusv..... Done
xcelium> source /apps/cadence/XCELUM303/tools/xcelium/files/xsimrc
xcelium> run
xsim: #USIMOPT: Some objects excluded from $shm_probe due to optimizations.
      File: ./tb_cpv.v30, line = 28, pos = 11
      Scope: stimulus
      Time: 0 FS + 0
Simulation complete via #finish(1) at time 501 NS + 0
./tb_cpv.v30 #1 $finish;
xcelium> exit
stripura@uranus.ece.iit.edu:~
```

Fig 30: RTL Simulation of CSA.

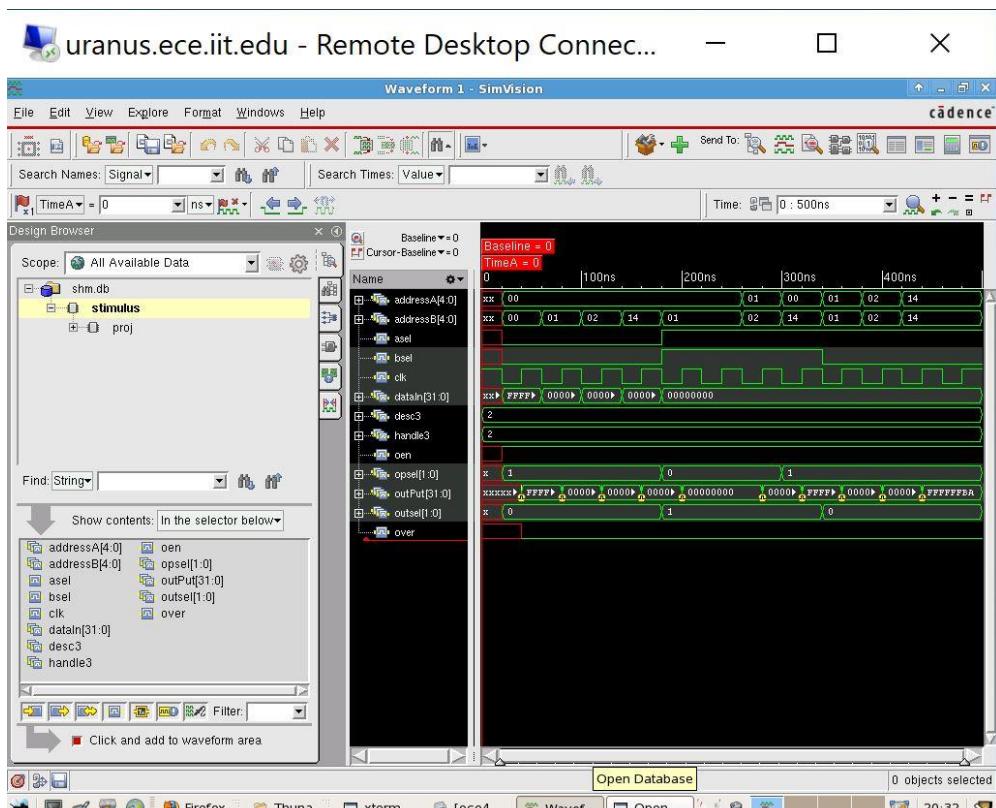


Fig 31: Waveforms of RTL Simulation of CSA.

```

Beginning Mapping Optimizations (Medium effort) (Incremental)
-----
Beginning Incremental Implementation Selection
-----
Beginning Delay Optimization Phase
-----
ELAPSED      WORST NEG TOTAL NEG DESIGN
TIME        AREA   SLACK  SLACK RULE COST    ENDPOINT
-----
0:00:02     48862.6 0.00   0.0   2.9
0:00:03     48862.6 0.00   0.0   2.9
0:00:03     48862.6 0.00   0.0   2.9

Beginning Design Rule Fixing (max_capacitance)
-----
ELAPSED      WORST NEG TOTAL NEG DESIGN
TIME        AREA   SLACK  SLACK RULE COST    ENDPOINT
-----
0:00:03     48862.6 0.00   0.0   2.9
Loading db file '/apps/FredPDK45/osu_soc/lib/files/gsc145nm.db'

Optimization Complete
-----
Warning: Design 'cpu' contains 1 high-fanout nets. A fanout number of 1000 will be used for delay calculations involving these nets. (TIM-134)
  Net 'clk': 1624 load(s), 1 driver(s)
1
check_design
1
#report_constraint -all_violators
set filename [format "%sX%s" $my_toplevel ".vh"]
cpu.vh
write -f verilog -output $filename
Writing verilog file '/home/stripura/Desktop/ece429/accu/cpu.vh'.
1
set filename [format "%sX%s" $my_toplevel ".sdc"]
cpu.sdc
write_sdc $filename
1
#set filename [format "%sX%s" $my_toplevel ".db"]
#write -f db -hier -output $filename -xg_force_db
redirect timing,rep { report_timing }
redirect cell,rep { report_cell }
redirect power,rep { report_power }
quit

Thank you...
Elapsed Time = 2:28.61, CPU Time = 146.301
stripura@uranus.ece.iit.edu:~% 

```

Fig 32: Logic Synthesis using Design Compiler.

	Time	Value	Unit
a/l3/f257/1230/U5/Y (XNOR2X1)	0.00	5.04	r
a/l3/f256/U2/Y (XOR2X1)	0.07	5.91	r
a/l3/f265/U5/Y (XNOR2X1)	0.06	5.97	r
a/l3/f265/U2/Y (XOR2X1)	0.07	6.04	r
a/l3/f274/U5/Y (XNOR2X1)	0.06	6.11	r
a/l3/f274/U2/Y (XOR2X1)	0.07	6.18	r
a/l3/f283/U5/Y (XNOR2X1)	0.06	6.24	r
a/l3/f283/U2/Y (XOR2X1)	0.07	6.31	r
a/l3/f292/U5/Y (XNOR2X1)	0.06	6.37	r
a/l3/f292/U2/Y (XOR2X1)	0.07	6.44	r
a/l3/h301/U2/Y (XOR2X1)	0.04	6.48	f
a/U26/Y (AOI22X1)	0.03	6.52	r
U224/Y (BUF2X2)	0.04	6.56	r
U66/Y (AND2X1)	0.06	6.61	r
U1823/Y (INVX1)	0.21	6.83	f
mb/ram/mer0/m0/m31/U3/Y (AOI22X1)	0.10	6.93	r
U3357/Y (INVX1)	0.02	6.95	f
mb/ram/mer0/l1/me31/qout_reg/D (DFFPOSX1)	0.00	6.95	f
data arrival time		6.95	
clock clk (rise edge)	16.00	16.00	
clock network delay (ideal)	0.00	16.00	
mb/ram/mer0/l1/me31/qout_reg/CLK (DFFPOSX1)	0.00	16.00	r
library setup time	-0.06	15.94	
data required time		15.94	

data required time		15.94	
data arrival time		-6.95	

slack (MET)		8.99	
1			

Fig 33: timing.rep from synthesis of CLA.

uranus.ece.iit.edu - Remote Desktop Connec...

cell.rep (~/Desktop/ece429/accu) - gedit

```

File Edit View Search Tools Documents Help
cell.rep x
o/tr/t7/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t8/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t9/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t10/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t11/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t12/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t13/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t14/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t15/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t16/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t17/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t18/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t19/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t20/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t21/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t22/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t23/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t24/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t25/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t26/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t27/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t28/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t29/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t30/b1 TBUFX2 gsc145 nm 3.754400 n
o/tr/t31/b1 TBUFX2 gsc145 nm 3.754400 n
wb/bd/me0/qout_reg DFPPOSX1 gsc145 nm 7.978100 n
wb/bd/me1/qout_reg DFPPOSX1 gsc145 nm 7.978100 n
wb/bd/me2/qout_reg DFPPOSX1 gsc145 nm 7.978100 n
wb/bd/me3/qout_reg DFPPOSX1 gsc145 nm 7.978100 n
wb/bd/me4/qout_reg DFPPOSX1 gsc145 nm 7.978100 n
-----
Total 14468 cells 48862.576477
1

```

[accu - File Manager] Ln 1, Col 1 INS

Fig 34: cell.rep from synthesis of CLA.

uranus.ece.iit.edu - Remote Desktop Connec...

power.rep (~/Desktop/ece429/accu) - gedit

```

File Edit View Search Tools Documents Help
power.rep x
write load model mode, top

Global Operating Voltage = 1.1
Power-specific unit information :
  Voltage Units = 1V
  Capacitance Units = 1.000000pf
  Time Units = 1ns
  Dynamic Power Units = 1mW      (derived from V,C,T units)
  Leakage Power Units = 1nW

Cell Internal Power = 1.7161 mW (85%)
Net Switching Power = 306.9190 uW (15%)
-----
Total Dynamic Power = 2.0230 mW (100%)

Cell Leakage Power = 262.5605 uW



| Power Group   | Internal Power | Switching Power | Leakage Power | Total Power | ( % )     | Attrs |
|---------------|----------------|-----------------|---------------|-------------|-----------|-------|
| io_pad        | 0.0000         | 0.0000          | 0.0000        | 0.0000      | ( 0.00%)  |       |
| memory        | 0.0000         | 0.0000          | 0.0000        | 0.0000      | ( 0.00%)  |       |
| black_box     | 0.0000         | 0.0000          | 0.0000        | 0.0000      | ( 0.00%)  |       |
| clock_network | 0.0000         | 0.0000          | 0.0000        | 0.0000      | ( 0.00%)  |       |
| register      | 1.4685         | 4.2974e-02      | 8.9282e+04    | 1.6007      | ( 70.04%) |       |
| sequential    | 0.0000         | 0.0000          | 0.0000        | 0.0000      | ( 0.00%)  |       |
| combinational | 0.2476         | 0.2639          | 1.7327e+05    | 0.6848      | ( 29.96%) |       |
| Total         | 1.7161 mW      | 0.3069 mW       | 2.6255e+05 nW | 2.2856 mW   |           |       |


```

[accu - File Manager] Ln 1, Col 1 INS

Fig 35: power.rep from synthesis of CLA.

```

module worklib.cpuvh
  errors: 0; warnings: 0
  reading library 'worklib' ..... Done
  Elaborating the design hierarchy:
  Top level design units:
    A0I2X1
    BUFX4
    CLKBUF1
    CLKBUF2
    DFF4
    DFF7
    DFFEQ4
    DFFSR
    FA1
    HX1
    INV2
    INX4
    INV8
    INV16
    MTCR
    MUX21
    NOR3X1
    OR12X1
    OR2X2
    TBURXL
    stimulus
  Building instance overlay tables: ..... Done
  Generating native compiled code:
    worklib.cpuvh <0x7c70:35>
      streams: 0, words: 0
    worklib,stimulusiv <0x416cb96f>
      streams: 13, words: 17664
  Building instance specific data structures.
  Loading native compiled code: ..... Done
  Design hierarchy summary:
    Instances Unique
    Modules: 14488 34
    UDPS: 1628 4
    Primitives: 25413 6
    Timing outputs: 14488 19
    Registers: 1638 18
    Scalar wires: 16346 -
    Block wires: 46 5
    Always blocks: 1 1
    Initial blocks: 3 3
    Pseudo assignments: 9 9
    Timing checks: 9769 1625
    Simulation timescale: 10ps
  Writing initial simulation snapshot: worklib,A0I2X1:v
  Loading snapshot worklib,A0I2X1:v ..... Done
  xcclium> source /apps/cadence/XCEL10M103/tools/xsim/xsimrc
  xcclium> run
  Simulation complete via $finish(1) at time 501 NS + 0
  ./tb.cpu,v30 #1 $finish;
  xcclium> exit
  stripura@uranus.ece.iit.edu:"% "

```

Fig 36: Post Synthesis Simulation.

```

2020-Dec-03 17:56:34 (2020-Dec-03 23:56:34 GMT): 10%
2020-Dec-03 17:56:34 (2020-Dec-03 23:56:34 GMT): 15%
2020-Dec-03 17:56:34 (2020-Dec-03 23:56:34 GMT): 20%
2020-Dec-03 17:56:34 (2020-Dec-03 23:56:34 GMT): 25%
2020-Dec-03 17:56:34 (2020-Dec-03 23:56:34 GMT): 30%
2020-Dec-03 17:56:34 (2020-Dec-03 23:56:34 GMT): 35%
2020-Dec-03 17:56:34 (2020-Dec-03 23:56:34 GMT): 40%
2020-Dec-03 17:56:34 (2020-Dec-03 23:56:34 GMT): 45%
... Calculating internal and leakage power
2020-Dec-03 17:56:34 (2020-Dec-03 23:56:34 GMT): 50%
2020-Dec-03 17:56:34 (2020-Dec-03 23:56:34 GMT): 55%
2020-Dec-03 17:56:35 (2020-Dec-03 23:56:35 GMT): 60%
2020-Dec-03 17:56:35 (2020-Dec-03 23:56:35 GMT): 65%
2020-Dec-03 17:56:35 (2020-Dec-03 23:56:35 GMT): 70%
2020-Dec-03 17:56:35 (2020-Dec-03 23:56:35 GMT): 75%
2020-Dec-03 17:56:35 (2020-Dec-03 23:56:35 GMT): 80%
2020-Dec-03 17:56:35 (2020-Dec-03 23:56:35 GMT): 85%
2020-Dec-03 17:56:35 (2020-Dec-03 23:56:35 GMT): 90%
2020-Dec-03 17:56:35 (2020-Dec-03 23:56:35 GMT): 95%
Finished Calculating power
2020-Dec-03 17:56:35 (2020-Dec-03 23:56:35 GMT)
*

Total Power
-----
Total Internal Power: 5.277 55.35%
Total Switching Power: 3.992 41.87%
Total Leakage Power: 0.2646 2.776%
Total Power: 9.533
-----
report_power consumed time (real time) 00:00:03 : peak memory (591M)
Output file is power.final
*****
* Encounter script finished *
* Results: *
* -----
* Layout: final.gds2 *
* Netlist: final.v *
* Timing: timing.rep.5.final *
* Area: area.final *
* Power: power.final *
* Type 'win' to get the Main Window *
* or type 'exit' to quit *
* ****
encounter 1> reportGateCount -limit 0
Gate area 2.8158 um^2
[0] cpu Gates=15840 Cells=14551 Area=44603.7 um^2
Xfce Menu

```

Fig 37: Area Report.

uranus.ece.iit.edu - Remote Desktop Connec... — □ ×

xterm

```
Total Power
-----
Total Internal Power: 5.277 55.35%
Total Switching Power: 3.992 41.87%
Total Leakage Power: 0.2846 2.776%
Total Power: 9.533

Group Internal Switching Leakage Total Percentage
----- Power Power Power (%)
Sequential 2,451 0,2165 0,08928 2,757 28.92
Macro 0 0 0 0 0
IO 0 0 0 0 0
Combinational 2,729 2,546 0,1733 5,448 57.15
Clock (Combinational) 0,09621 1,23 0,002047 1,328 13.93
Clock (Sequential) 0 0 0 0 0
Total 5,277 3,992 0,2646 9,533 100

Rail Voltage Internal Switching Leakage Total Percentage
----- Power Power Power (%)
vdd 1.1 5.277 3.992 0,2646 9,533 100

Clock Internal Switching Leakage Total Percentage
----- Power Power (%)
clk 0,09621 1,23 0,002047 1,328 13.93
Total 0,09621 1,23 0,002047 1,328 13.93

* Power Distribution Summary:
* Highest Average Power: clk_L4_I20 (INVX8): 0,01942
* Highest Leakage Power: mb/ram/mer2/11/me31/qout_reg (DFFPOSX1): 5,498e-05
* Total Cells: 1,1524e+15 F
* Total Instances in design: 14951
* Total Instances in design with no power: 0
* Total Instances in design with no activity: 0
* Total Fillers and Decaps: 0

report_power consumed time (real time) 00:00:00 : peak memory (591M)
1
encounter > [ece429 - File Manager]
```

[ece429 - File Manager] [accu - File M... xterm accu - File Ma... 18:01

Fig 38: Power Report.

uranus.ece.iit.edu - Remote Desktop Connec... — □ ×

timing.rep.5.final (~/Desktop/ece429/accu) - gedit

```
File Edit View Search Tools Documents Help
timing.rep.5.final x

#####
# Generated by: Cadence Encounter 10.13-s292_1
# OS: Linux x86_64(Host ID uranus.ece.iit.edu)
# Generated on: Thu Dec 3 17:56:18 2020
# Design: cpu
# Command: report timing -nworst 10 -net > timing.rep.5.final
#####
Path 1: MET Setup Check with Pin mb/ram/mer3/ll/me31/qout_reg/CLK
Endpoint: mb/ram/mer3/ll/me31/qout_reg/D (^) checked with leading edge of
'clk'
Beginpoint: m0pd/bb/me2/qout_reg/Q (v) triggered by leading edge of
'clk'
Other End Arrival Time 0.351
- Setup 3.783
+ Phase Shift 16.000
= Required Time 12.568
- Arrival Time 11.504
= Slack Time 1.064
    Clock Rise Edge 0.000
    + Clock Network Latency (Prop) 0.360
    = Beginpoint Arrival Time 0.360

+-----+
| Pin | Edge | Net | Cell | Delay |
Arrival | Required | | | | | |
Time | Time | | | | | |
+-----+-----+-----+-----+
| m0pd/bb/me2/qout_reg/CLK | ^ | clk_L4_N8 | | | |
0.360 | 1.423 | | v | R121 | | DEFPASY1 | A_261 |
```

[ece429 - File Manager] Ln 1, Col 1 INS
[ece429 - File M... xterm accu - File Ma... timing.re... 18:02

Fig 39: timing.rep.5.final

```

uranus.ece.iit.edu - Remote Desktop Connec... - xterm
xrun: 18.03-s001: (c) Copyright 1995-2018 Cadence Design Systems, Inc.
file: final.v
  module worklib,cpuv
    errors: 0, warnings: 0
    Coding library 'worklib' ..... Done
  Elaborating the design hierarchy:
  Top level design units:
    AOI21X1
    BUF4X1
    CLKBUFL
    CLKBUFL2
    CLKBUFL3
    DFFNEGX1
    DFFSR
    FANL
    H4X1
    INVX2
    INVX4
    LATCH
    MUX2X1
    NOR3X1
    OA122X1
    O2X2
    TBUF4X1
    stimulus
  Building instance overlay tables: ..... Done
  Generating native compiled code:
  worklib.cpuv <>0xd07882d6>
    streams: 0, words: 0
  Building instance specific data structures.
  Loading native compiled code: ..... Done
  Design hierarchy summary:
    Instances Unique
    Modules: 14570 34
    UDPs: 1628 4
    Primitives: 25495 6
    Timing outputs: 14570 19
    Registers: 1638 18
    Scalar wires: 16428 -
    Expanded wires: 46 5
    Always blocks: 1 1
    Initial blocks: 3 3
    Pseudo assignments: 9 9
    Timing checker: 9769 1625
    Simulation timescale: 10ps
  Writing initial simulation snapshot: worklib.AOI21X1iv
  Loading snapshot worklib.AOI21X1iv ..... Done
  xcelium> source /apps/cadence/XCELUM1803/tools/xcelium/files/xsimrc
  xcelium> run
  Simulation complete via $finish(1) at time 501 NS + 0
  ./tb_cpu.v:30 #1 $finish;
  xcelium> exit
  stripr@uranus.ece.iit.edu:"[ece429 - File Manager]"

```

Fig 40: Post P&R Simulation.

Encounter is mainly used to place the standard cells and route to the interconnects. The Verilog model output from encounter is used for post P&R simulation. Furthermore, from the output file timing.rep, required time (8.99) is obtained. Therefore, maximum clock frequency should be 11.123MHz.

d. Carry Select Adder:

The following figures go through the implementation steps explained above.

```

uranus.ece.iit.edu - Remote Desktop Connec... - xterm
xsimlab: *U,CMMSP (./cpu_CSeA.v,95318); 1 output port was not connected;
xsimlab: (./cpu_CSeA.v,953); over
  Top level design units:
    stimulus
  Building instance overlay tables: ..... Done
  Generating native compiled code:
  worklib.stimulusv <>0x25000000>
    streams: 32, words: 6720
  worklib.CSeA_iv <>0x6890234>
    streams: 1, words: 379
  worklib.ass2d2iv <>0x5d203101>
    streams: 2, words: 420
  worklib.bcm_iv <>0x6890fa5d5>
    streams: 1, words: 1113
  worklib.aluv <>0x61260600>
    streams: 1, words: 1246
  worklib.bcm_32iv <>0x7d7d5ab7>
    streams: 0, words: 0
  worklib.mux2to1iv <>0x3f684099>
    streams: 0, words: 0
  worklib.mux2to1_32iv <>0x7d7d59bec>
    streams: 0, words: 0
  worklib.memoryBlockv <>0x05ba1895>
    streams: 1, words: 208
  worklib.dregiv <>0x60a2e9c9>
    streams: 2, words: 264
  Building instance specific data structures.
  Loading native compiled code: ..... Done
  Design hierarchy summary:
    Instances Unique
    Modules: 6507 31
    Primitives: 7507 6
    Registers: 2166 14
    Scalar wires: 3571 -
    Expanded wires: 1239 49
    Factored wires: 6 6
    Always blocks: 2156 4
    Initial blocks: 3 3
    Cont. assignments: 9 11
    Pseudo assignments: 45 43
  Writing initial simulation snapshot: worklib.stimulusv
  Loading snapshot worklib.stimulusv ..... Done
  xcelium> source /apps/cadence/XCELUM1803/tools/xcelium/files/xsimrc
  xcelium> run
  xsim: *U,DPNOT: Some objects excluded from $shm_probe due to optimizations.
  File: ./tb_cpu.v, line = 28, pos = 11
  Scope: stimulus
  Time: 0 FS + 0
  Simulation complete via $finish(1) at time 501 NS + 0
  ./tb_cpu.v:30 #1 $finish;
  xcelium> exit
  stripr@uranus.ece.iit.edu:"
```

Fig 41: RTL Simulation for CSeA.

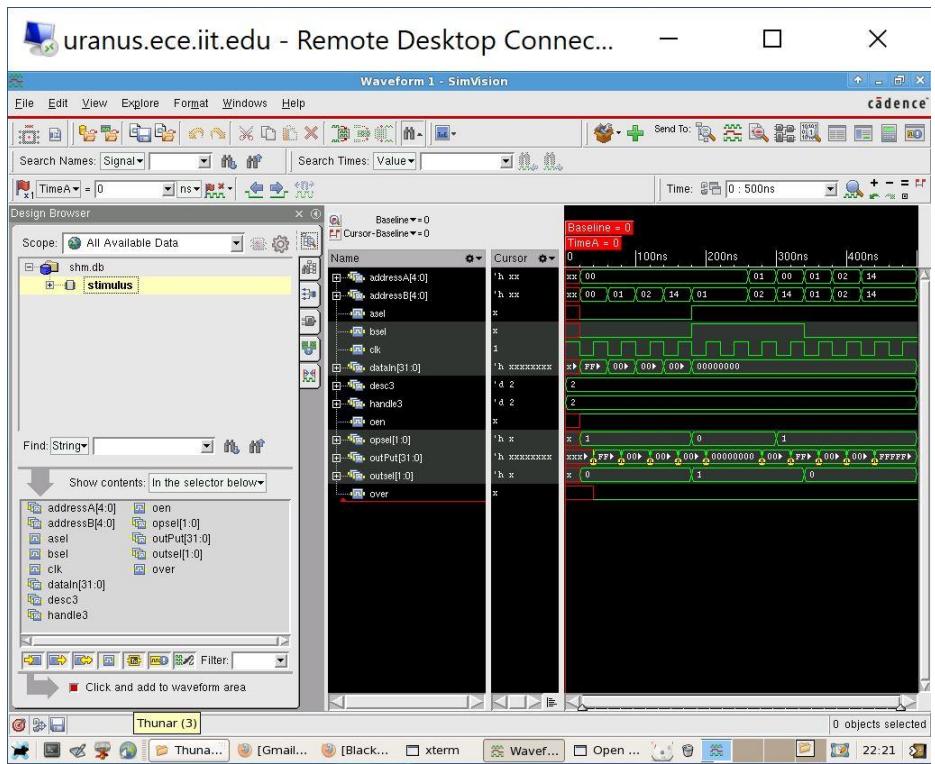


Fig 42: Waveforms in Simvision of RTL Simulation.

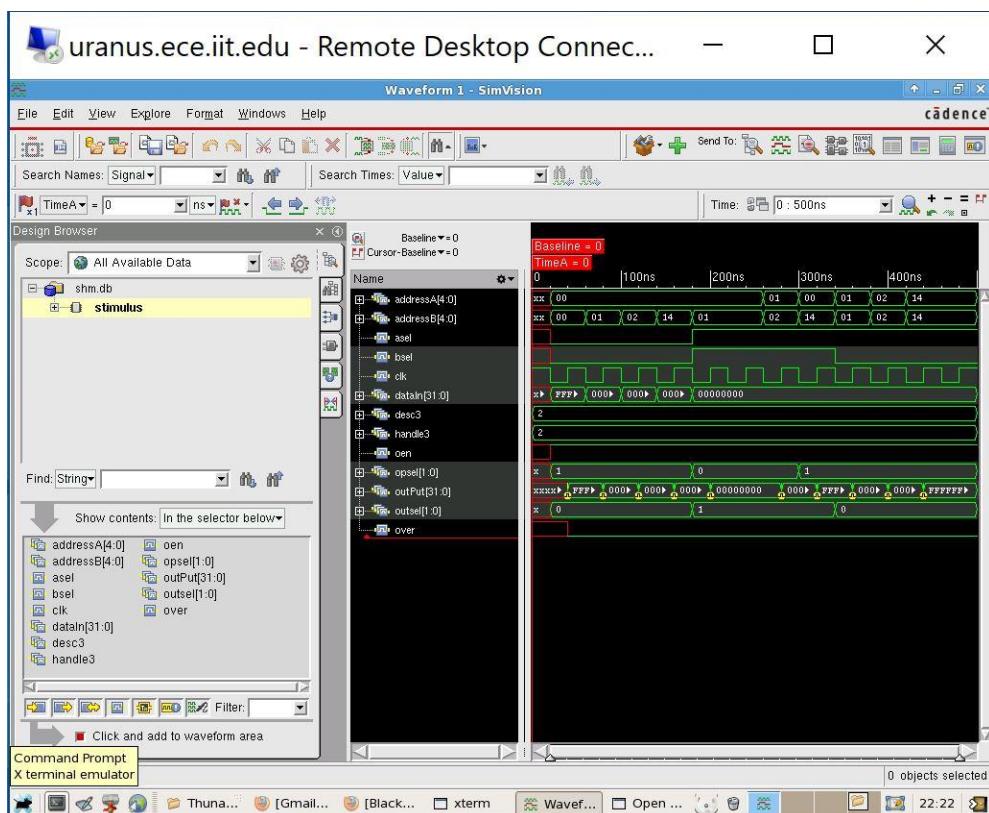


Fig 43: Complete Waveforms in Simvision of RTL Simulation.

```

Beginning Mapping Optimizations (Medium effort) (Incremental)
-----
Beginning Incremental Implementation Selection
-----
Beginning Delay Optimization Phase
-----
ELAPSED          WORST NEG TOTAL NEG DESIGN
TIME           AREA  SLACK  SLACK RULE COST      ENDPOINT
-----          -----  -----  -----  -----
0:00:02        49149.3 0.00   0.0    3.0
0:00:03        49149.3 0.00   0.0    3.0
0:00:03        49149.3 0.00   0.0    3.0

Beginning Design Rule Fixing (max_capacitance)
-----
ELAPSED          WORST NEG TOTAL NEG DESIGN
TIME           AREA  SLACK  SLACK RULE COST      ENDPOINT
-----          -----  -----  -----  -----
0:00:03        49149.3 0.00   0.0    3.0
Loading db file '/apps/FreePDK45/osu_soc/lib/files/gsc145nm.db'
Optimization Complete
-----
Warnings: Design 'cpu' contains 1 high-fanout nets. A fanout number of 1000 will be used for delay calculations involving these nets. (TIN-134)
Net 'clk': 1624 load(s), 1 driver(s)
1
check_design
1
#report_constraint -all_violators
set filename [Format "%s%s" $my_toplevel ".vh"]
cpu.vh
write -f verilog -output $filename
Writing verilog file '/home/stripura/Desktop/ece429/accu/cpu.vh'.
1
set filename [Format "%s%s" $my_toplevel ".sdc"]
cpu.sdc
write_sdc $filename
1
#set filename [Format "%s%s" $my_toplevel ".db"]
#write -f db -quiet -output $filename -xg_force_db
redirect timing.rep { report_timing }
redirect cell,rep { report_cell }
redirect power,rep { report_power }
quit
Thank you...
Elapsed time = 2:28.47, CPU Time = 146.326
stripura@uranus.ece.iit.edu:"
```

Fig 44: Logic Synthesis using Design Compiler.

```

File Edit View Search Tools Documents Help
timing.rep x
----- (Timing Report) -----
U3574/Y (INVX1)          0.04  0.02 r
a/l3/f3028/U3/Y (0AI21X1) 0.04  6.06 f
U3576/Y (INVX1)          0.04  6.10 r
a/l3/f3029/U3/Y (0AI21X1) 0.04  6.14 f
U3884/Y (INVX1)          0.04  6.18 r
a/l3/f3030/U3/Y (0AI21X1) 0.04  6.21 f
U3885/Y (INVX1)          0.04  6.26 r
a/l3/f3031/U3/Y (0AI21X1) 0.04  6.29 f
U3578/Y (INVX1)          0.04  6.33 r
a/l3/f3032/U2/Y (XOR2X1) 0.03  6.37 f
a/U29/Y (AOI22X1)         0.05  6.40 f
U243/Y (BUFX2)            0.04  6.45 r
U75/Y (AND2X1)             0.06  6.48 r
U1331/Y (INVX1)            0.21  6.54 r
mb/ram/mer0/m0/m30/U3/Y (A0I22X1) 0.10  6.76 f
U3415/Y (INVX1)            0.02  6.85 r
mb/ram/mer0/ll/me30/qout_reg/D (DFFP0SX1) 0.00  6.88 f
data arrival time          6.88

clock clk (rise edge)      15.00 15.00
clock network delay (ideal) 0.00 15.00
mb/ram/mer0/ll/me30/qout_reg/CLK (DFFP0SX1) 0.00 15.00 r
library setup time          -0.06 14.94
data required time          14.94

----- (Timing Report) -----
data required time          14.94
data arrival time            -6.88

slack (MET)                 8.07

1
[accu - File Manager] Ln 16, Col 1 INS
[accu - File Manager] xterm accu - File... timing.re... 16:29
```

Fig 45: timing.rep from synthesis of CRA.

uranus.ece.iit.edu - Remote Desktop Connec...

cell.rep (~/Desktop/ece429/accu) - gedit

```

File Edit View Search Tools Documents Help
cell.rep x
-----v
o/tr/t7/b1    TBUFX2    gscl45nm  3.754400 n
o/tr/t8/b1    TBUFX2    gscl45nm  3.754400 n
o/tr/t9/b1    TBUFX2    gscl45nm  3.754400 n
o/tr/t10/b1   TBUFX2    gscl45nm  3.754400 n
o/tr/t11/b1   TBUFX2    gscl45nm  3.754400 n
o/tr/t12/b1   TBUFX2    gscl45nm  3.754400 n
o/tr/t13/b1   TBUFX2    gscl45nm  3.754400 n
o/tr/t14/b1   TBUFX2    gscl45nm  3.754400 n
o/tr/t15/b1   TBUFX2    gscl45nm  3.754400 n
o/tr/t16/b1   TBUFX2    gscl45nm  3.754400 n
o/tr/t17/b1   TBUFX2    gscl45nm  3.754400 n
o/tr/t18/b1   TBUFX2    gscl45nm  3.754400 n
o/tr/t19/b1   TBUFX2    gscl45nm  3.754400 n
o/tr/t20/b1   TBUFX2    gscl45nm  3.754400 n
o/tr/t21/b1   TBUFX2    gscl45nm  3.754400 n
o/tr/t22/b1   TBUFX2    gscl45nm  3.754400 n
o/tr/t23/b1   TBUFX2    gscl45nm  3.754400 n
o/tr/t24/b1   TBUFX2    gscl45nm  3.754400 n
o/tr/t25/b1   TBUFX2    gscl45nm  3.754400 n
o/tr/t26/b1   TBUFX2    gscl45nm  3.754400 n
o/tr/t27/b1   TBUFX2    gscl45nm  3.754400 n
o/tr/t28/b1   TBUFX2    gscl45nm  3.754400 n
o/tr/t29/b1   TBUFX2    gscl45nm  3.754400 n
o/tr/t30/b1   TBUFX2    gscl45nm  3.754400 n
o/tr/t31/b1   TBUFX2    gscl45nm  3.754400 n
wb/bd/me0/qout_reg DFFPOSX1  gscl45nm  7.978100 n
wb/bd/me1/qout_reg DFFPOSX1  gscl45nm  7.978100 n
wb/bd/me2/qout_reg DFFPOSX1  gscl45nm  7.978100 n
wb/bd/me3/qout_reg DFFPOSX1  gscl45nm  7.978100 n
wb/bd/me4/qout_reg DFFPOSX1  gscl45nm  7.978100 n
-----
Total 14576 cells          49149.318772
1

```

[ece429 - File Manager]

Ln 1, Col 1 INS

File Edit View Search Tools Documents Help

power.rep (~/Desktop/ece429/accu) - gedit

Fig 46: cell.rep from synthesis of CRA.

uranus.ece.iit.edu - Remote Desktop Connec...

power.rep (~/Desktop/ece429/accu) - gedit

```

File Edit View Search Tools Documents Help
power.rep x
-----v
write load model mode: top

Global Operating Voltage = 1.1
Power-specific unit information :
  Voltage Units = 1V
  Capacitance Units = 1.000000pf
  Time Units = 1ns
  Dynamic Power Units = 1mW      (derived from V,C,T units)
  Leakage Power Units = 1nW

Cell Internal Power = 1.8377 mW (85%)
Net Switching Power = 334.1051 uW (15%)
-----
Total Dynamic Power = 2.1718 mW (100%)

Cell Leakage Power = 263.6269 uW



| Power Group   | Internal Power | Switching Power | Leakage Power | Total Power | ( % )     | Attrs |
|---------------|----------------|-----------------|---------------|-------------|-----------|-------|
| io_pad        | 0.0000         | 0.0000          | 0.0000        | 0.0000      | ( 0.00%)  |       |
| memory        | 0.0000         | 0.0000          | 0.0000        | 0.0000      | ( 0.00%)  |       |
| black_box     | 0.0000         | 0.0000          | 0.0000        | 0.0000      | ( 0.00%)  |       |
| clock_network | 0.0000         | 0.0000          | 0.0000        | 0.0000      | ( 0.00%)  |       |
| register      | 1.5664         | 4.5838e-02      | 8.9282e+04    | 1.7015      | ( 69.87%) |       |
| sequential    | 0.0000         | 0.0000          | 0.0000        | 0.0000      | ( 0.00%)  |       |
| combinational | 0.2713         | 0.2883          | 1.7433e+05    | 0.7339      | ( 30.13%) |       |
| Total         | 1.8377 mW      | 0.3341 mW       | 2.6362e+05 nW | 2.4354 mW   |           |       |


```

[ece429 - File Manager]

Ln 1, Col 1 INS

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Fig 47: power.rep from synthesis of CRA.

```

errors: 0, warnings: 0
Caching library 'worklib' ..... Done
Elaborating the design hierarchy:
Top level design units:
  R0I2X1
  INV4
  CLKBUF1
  CLKBUF2
  CLKBUF3
  IFFNEGX1
  DFFSR
  FAK1
  INV1
  INV2
  INV3
  INV8
  LATCH
  MUX2X1
  NAN03X1
  NOR3X1
  OH2Z2X1
  OR2
  TBUF1
  stimulus
Building instance overlay tables: ..... Done
Generating native compiled code:
  worklib.cpuvh <0x69f0117>
    streams: 0, words: 0
  worklib.bundles: 1, words: 146ccb6f>
    streams: 13, words: 17654
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
  Instances Unique
  Modules: 14597 34
  Cells: 1623
  Primitives: 2547 6
  Timing outputs: 14597 19
  Registers: 1638 18
  Scalar wires: 16455 -
  Expanded wires: 46 5
  Always blocks: 1 1
  Initial blocks: 3 3
  Open assignments: 3 9
  Timing checker: 9769 1625
  Simulation timescale: 10ps
Writing initial simulation snapshot: worklib.R0I2X1.v
Loading snapshot worklib.R0I2X1.vv ..... Done
xcelium> source /apps/cadence/XCELUM103/tools/xcelium/files/xmsimrc
xcelium> run
Simulation complete via $finish(1) at time 501 NS + 0
,`tb_cpu,v:50` $1 $finish;
xcelium> exit

```

Fig 48: Post Synthesis Simulation.

```

2020-Dec-03 16:35:09 (2020-Dec-03 22:35:09 GMT): 10%
2020-Dec-03 16:35:09 (2020-Dec-03 22:35:09 GMT): 15%
2020-Dec-03 16:35:09 (2020-Dec-03 22:35:09 GMT): 20%
2020-Dec-03 16:35:09 (2020-Dec-03 22:35:09 GMT): 25%
2020-Dec-03 16:35:09 (2020-Dec-03 22:35:09 GMT): 30%
2020-Dec-03 16:35:09 (2020-Dec-03 22:35:09 GMT): 35%
2020-Dec-03 16:35:09 (2020-Dec-03 22:35:09 GMT): 40%
2020-Dec-03 16:35:09 (2020-Dec-03 22:35:09 GMT): 45%
... Calculating internal and leakage power
2020-Dec-03 16:35:09 (2020-Dec-03 22:35:09 GMT): 50%
2020-Dec-03 16:35:09 (2020-Dec-03 22:35:09 GMT): 55%
2020-Dec-03 16:35:09 (2020-Dec-03 22:35:09 GMT): 60%
2020-Dec-03 16:35:09 (2020-Dec-03 22:35:09 GMT): 65%
2020-Dec-03 16:35:09 (2020-Dec-03 22:35:09 GMT): 70%
2020-Dec-03 16:35:09 (2020-Dec-03 22:35:09 GMT): 75%
2020-Dec-03 16:35:10 (2020-Dec-03 22:35:10 GMT): 80%
2020-Dec-03 16:35:10 (2020-Dec-03 22:35:10 GMT): 85%
2020-Dec-03 16:35:10 (2020-Dec-03 22:35:10 GMT): 90%
2020-Dec-03 16:35:10 (2020-Dec-03 22:35:10 GMT): 95%
Finished Calculating power
2020-Dec-03 16:35:10 (2020-Dec-03 22:35:10 GMT):
*

Total Power
-----
Total Internal Power: 5.68 55.24%
Total Switching Power: 4.336 42.17%
Total Leakage Power: 0.2657 2.584%
Total Power: 10.28

report_power consumed time (real time) 00:00:03 : peak memory (570M)
Output file is power_final
*****
* Encountered script finished
* Results:
* -----
* Layout: final.gds2
* Netlist: final.v
* Timing: timing.rep_5,final
* Area: area_final
* Power: power_final
* Type 'win' to get the Main Window
* or type 'exit' to quit
* ****
encounter 13 report@lateCount -limit 0
Gate area 2.8158 um^2
[0] cpu Gates=15935 Cells=14651 Area=44969.8 um^2
encounter 23

```

Fig 49: Area Report.

```

uranus.ece.iit.edu - Remote Desktop Connec... - xterm
Total Power
-----
Total Internal Power: 5.68 55.24%
Total Switching Power: 4.336 42.17%
Total Leakage Power: 0.2657 2.584%
Total Power: 10.28

Group Internal Power Switching Power Leakage Power Total Power Percentage
-----
Sequential 2,612 0,2378 0,08928 2,94 28.6
Macro 0 0 0 0 0
IO 0 0 0 0 0
Combinational 2,967 2,783 0,1743 5,924 57.62
Clock (Combinational) 0,1004 1,315 0,002096 1,418 13.79
Clock (Sequential) 0 0 0 0 0

Total 5.68 4.336 0.2657 10.28 100

Rail Voltage Internal Power Switching Power Leakage Power Total Power Percentage
-----
vdd 1.1 5.68 4.336 0.2657 10.28 100

Clock Internal Power Switching Power Leakage Power Total Power Percentage
-----
clk 0,1004 1,315 0,002096 1,418 13.79
Total 0,1004 1,315 0,002096 1,418 13.79

Power Distribution Summary
* Highest Average Power: clk_L4_I9 (INV08): 0.02094
* Highest Leakage Power: mb/ram/mem2/11/me31/qout_reg (DFP05X1): 5.498e-05
* Total Cap: 1.8442e-10 F
* Total instances in design: 14661
* Total instances in design with power: 0
* Total instances in design with no activity: 0
* Total Fillers and Decap: 0

report_power consumed time (real time) 00:00:00 : peak memory (570M)
1
encounter 32

```

Fig 50: Power Report.

```

uranus.ece.iit.edu - Remote Desktop Connec... - xterm
xrun: 18.03-s001: (c) Copyright 1995-2018 Cadence Design Systems, Inc.
file: final.v
    module worklib.tbcpu
        error: 0 warnings: 0
        Caching library 'worklib' ..... Done
    Elaborating the design hierarchy;
    Top level design units:
        A0I21X1
        BUFX4
        CLKBUF1
        CLKBUF2
        CLKBUF3
        DFFBUF1
        DFFSR
        FOX1
        H0X1
        INVX2
        INVX4
        LATCH
        MUX2X1
        NAND3X1
        NOR3X1
        OR122X1
        OR222
        TBUF4
        stimulus
    Building instance overlay tables: ..... Done
    Generating native compiled code;
        worklib.tbcpu: <0x61440b37>
            streams: 0 words: 0
    Building instance specific data structures.
    Loading native compiled code: ..... Done
    Design hierarchy summary:
        Instances Unique
        Modules: 14681 34
        UDPs: 153 4
        Primitives: 25731 6
        Timing outputs: 14681 19
        Registers: 1638 18
        Scalar wires: 16539 -
        Expanded wires: 46 5
        Always blocks: 1 1
        Initial blocks: 3 3
        Pseudo assignments: 9 9
        Timing checks: 9769 1625
        Simulation timescale: 10ps
    Writing initial simulation snapshot: worklib.A0I21X1;
Loading snapshot worklib.A0I21X1; ..... Done
xcelium source /apps/cadence/XCELUM1803/tools/xcelium/files/xmsimrc
xcelium run
Simulation complete via $finish(1) at time 501 NS + 0
./tb_cpu.v30 "#$finish;
xcelium exit
stripura@uranus.ece.iit.edu:"% "

```

Fig 51: Post P&R Simulation.

```

uranus.ece.iit.edu - Remote Desktop Connec... - timing.rep.5.final (~/Desktop/ece429/accu) - gedit
File Edit View Search Tools Documents Help
timing.rep.5.final x
#####
# Generated by: Cadence Encounter 10.13-s292_1
# OS: Linux x86_64(Host ID uranus.ece.iit.edu)
# Generated on: Thu Dec 3 16:34:53 2020
# Design: cpu
# Command: report_timing -nworst 10 -net > timing.rep.5.final
#####
Path 1: MET Setup Check with Pin mb/ram/mer16/ll/me31/qout_reg/CLK
Endpoint: mb/ram/mer16/ll/me31/qout_reg/D (^) checked with leading edge of
'clk'
Beginpoint: m0pd/bb/me1/qout_reg/Q (v) triggered by leading edge of
'clk'
Other End Arrival Time 0.342
- Setup 3.838
+ Phase Shift 15.000
= Required Time 11.504
- Arrival Time 10.911
= Slack Time 0.593
    Clock Rise Edge 0.000
    + Clock Network Latency (Prop) 0.350
    = Beginpoint Arrival Time 0.350
+-----+
+-----+-----+-----+-----+-----+-----+
| Arrival | Required |           | Net       | Cell     | Delay |
| Time   | Time     |           |           |          |          |
+-----+-----+-----+-----+-----+-----+
| 0.350  | 0.943   |           | clk_L4_N1 |          |          |
| m0pd/bb/me1/qout_reg/CLK | ^ | R[1] | DEEPSY1 | 0.252 |
+-----+-----+-----+-----+-----+-----+

```

Fig 52: timing.rep.5.final.

Encounter is mainly used to place the standard cells and route to the interconnects. The Verilog model output from encounter is used for post P&R simulation. Furthermore, from the output file timing.rep, required time (8.07) is obtained. Therefore, maximum clock frequency should be 12.391MHz.

e. Simulation with New Test Bench:

1. The new testbench code is given below.

```

// Stimulate the Input Signals
initial
begin
// 1. store (0000_0005) in [0]
#T
addressA = 5'b00000;
addressB = 5'b00000;
dataIn = 32'h0000_0005;
opsel = 2'b01;
outsel = 2'b00;
asel = 0;
bsel = 0;
oen = 1;
 #(T*2)
// 2. store AAAA_AAAA in [1]
addressA=5'b00000;
addressB= 5'b00001;
dataIn = 32'hAAAA_AAAA;
opsel = 2'b01;
outsel = 2'b00;
asel = 0;
bsel = 0;
oen = 1;
 #(T*2)
// 3. store 5555_5555 in [2]
addressA = 5'b00000;
addressB = 5'b00010;
dataIn = 32'h5555_5555;
opsel = 2'b01;
outsel = 2'b00;
asel = 0;
bsel = 0;
oen = 1;
 #(T*2)
// 4. store 0000_000A in [3]
addressA = 5'b00000;
addressB = 5'b00011;
dataIn = 32'h0000_000A;
opsel = 2'b01;
outsel = 2'b00;
asel = 0;
bsel = 0;
oen = 1;
 #(T*2)
// 5. store 0000_0001 in [4]
addressA = 5'b00000;
addressB = 5'b00100;
dataIn = 32'h0000_0001;
opsel = 2'b01;
outsel = 2'b00;
asel = 0;
bsel = 0;
oen = 1;
 #(T*2)
// 6. store FFFF_FFFF in [5]
addressA = 5'b00000;
addressB = 5'b00101;
dataIn = 32'hFFFF_FFFF;
opsel = 2'b01;
outsel = 2'b00;
asel = 0;
bsel = 0;
oen = 1;
 #(T*2)
// 7. store 0000_00C8 in [6]
addressA = 5'b00000;
addressB = 5'b00110;
dataIn = 32'h0000_00C8;
opsel = 2'b01;
outsel = 2'b00;
asel = 0;
bsel = 0;
oen = 1;
 #(T*2)
// 8. store 0000_012C in [7]
addressA = 5'b00000;
addressB = 5'b00111;
dataIn = 32'h0000_012C;
opsel = 2'b01;
outsel = 2'b00;
asel = 0;
bsel = 0;
oen = 1;
 #(T*2)
// 9. store 0000_0001 in [8]
addressA = 5'b00000;
addressB = 5'b01000;
dataIn = 32'h0000_0001;

```

```

opsel = 2'b01;          oen = 1;
outsel = 2'b00;          #(T*2)
asel = 0;                //14. ADD [6][7]
bsel = 0;                addressA = 5'd6;
oen = 1;                addressB = 5'd7;
#(T*2)                  dataIn = 32'd0;
// 10. store AAAA_AAAB in [9]  opsel = 2'b00;
addressA = 5'b00000;    outsel = 2'b01;
addressB = 5'b01001;    asel = 1;
dataIn = 32'hAAAA_AAAB; bsel = 1;
opsel = 2'b01;          oen = 1;
outsel = 2'b00;          #(T*2)
asel = 0;                //14. ADD [0][3]
bsel = 0;                addressA = 5'd0;
oen = 1;                addressB = 5'd3;
#(T*2)                  dataIn = 32'd0;
// 11. store 5555_5555 in [10]  opsel = 2'b00;
addressA = 5'b00000;    outsel = 2'b01;
addressB = 5'b01010;    asel = 1;
dataIn = 32'h5555_5555; bsel = 1;
opsel = 2'b01;          oen = 1;
outsel = 2'b00;          #(T*2)
asel = 0;                //15. SUB [5][4]
bsel = 0;                addressA = 5'd5;
oen = 1;                addressB = 5'd4;
#(T*2)                  dataIn = 32'd0;
//12. ADD [2][0]          opsel = 2'b01;
addressA = 5'd2;          outsel = 2'b01;
addressB = 5'd0;          asel = 1;
dataIn = 32'd0;          bsel = 1;
opsel = 2'b00;          oen = 1;
outsel = 2'b01;          #(T*2)
asel = 1;                //16. ADD [5][8]
bsel = 1;                addressA = 5'd5;
oen = 1;                addressB = 5'd8;
#(T*2)                  dataIn = 32'd0;
//13. ADD [1][2]          opsel = 2'b00;
addressA = 5'd1;          outsel = 2'b01;
addressB = 5'd2;          asel = 1;
dataIn = 32'd0;          bsel = 1;
opsel = 2'b00;          oen = 1;
outsel = 2'b01;          #(T*2)
asel = 1;                //17. SUB [2][0]
bsel = 1;                addressA = 5'd2;

```

```

addressB = 5'd0;
dataIn = 32'd0;
opsel = 2'b01;
outsel = 2'b01;
asel = 1;
bsel = 1;
oen = 1;
#(T*2)
//18. ADD [9][10]
addressA = 5'd9;
addressB = 5'd10;
dataIn = 32'd0;
opsel = 2'b00;
outsel = 2'b01;
asel = 1;
bsel = 1;
oen = 1;
#(T*2)
//19. READ [7]
addressA = 5'd7;
addressB = 5'd7;
dataIn = 32'd0;
opsel = 2'b01;
outsel = 2'b00;
asel = 1;
bsel = 1;
oen = 1;
#(T*2)
//20. READ [3]
addressA = 5'd3;
addressB = 5'd3;
dataIn = 32'd0;
opsel = 2'b01;
outsel = 2'b00;
asel = 1;
bsel = 0;
oen = 1;
#(T*2)
//21. READ [1]
addressA = 5'd1;
addressB = 5'd1;
dataIn = 32'd0;
opsel = 2'b01;
outsel = 2'b00;
asel = 1;
bsel = 0;
oen = 1;
end
endmodule

```

2. RTL Simulation and Simvision waveforms of the adders and the new testbench.

a. Carry Ripple Adder:

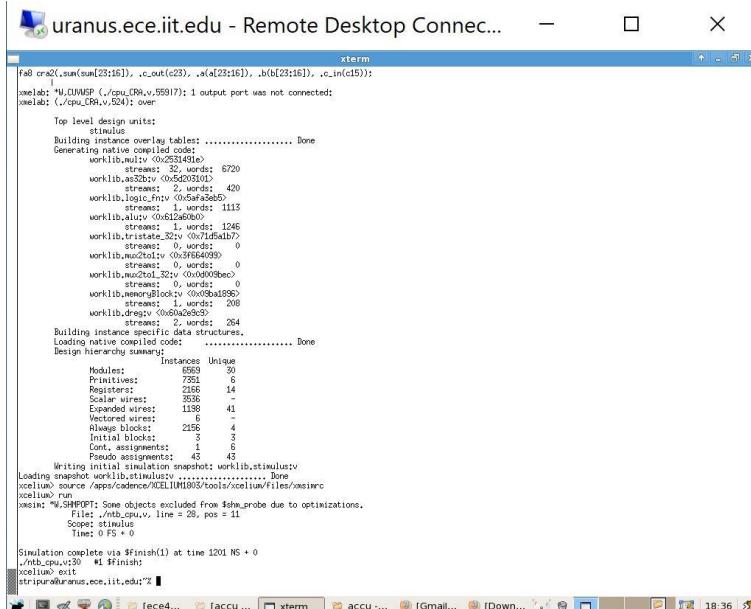


Fig 53: RTL Simulation.

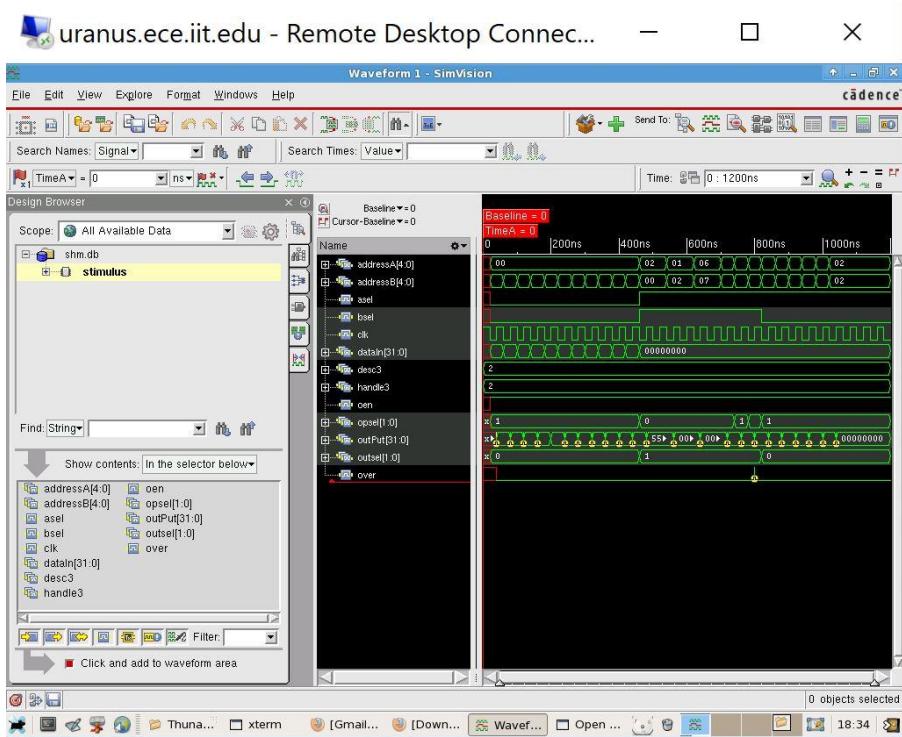


Fig 54: Simvision.

b. Carry Lookahead Adder:

```

uranus.ece.iit.edu - Remote Desktop Connec... — ×
xterm
carrylookahead_4 CLA2(.s(s[11:8]), .a(a[11:8]), .b(b[11:8]), .c0(c8), .c4(c12), .g4(g[2]), .p4(p[2]));
smlab: #U_CUNSP (/cpu_CLA.v:617/12): 1 output port was not connected;
smlab: (/cpu_CLA.v:575): over

Top level design units:
stimulus
Building instance overlay tables: ..... Done
Generating native compiled code:
worklib.muliv <0x2531491>
    streams: 32, words: 6720
worklib.as32bit <0x5d03321>
    streams: 1, words: 420
worklib.logic_fnv <0x5af3a3eb>
    streams: 1, words: 1113
worklib.aluv <0x612a0b0>
    streams: 1, words: 1246
worklib.alu32t <0x74f5d51b>
    streams: 0, words: 0
worklib.mux2tav <0x3f640499>
    streams: 0, words: 0
worklib.bcm2t2d32t <0x3f64049e>
    streams: 0, words: 0
worklib.memcrBlockv <0x09ba1896>
    streams: 1, words: 208
worklib.dregv <0x60a2e9c9>
    streams: 2, words: 264
Building instance specific data structures:
Loading native compiled code: ..... Done
Design hierarchy summary:
Instances Unique
Modules: 6601 33
Primitives: 7197 6
Registers: 2166 14
Scalar wires: 3692 -
Expanded wires: 1198 41
Vectorized wires: 16 -
Altice blocks: 2156 4
Initial blocks: 3 3
Cont. assignments: 11 15
Pseudo assignments: 43 43
Writing stimulus file for simulation: worklib.stimulussv
Loading snapshot worklib.stimulussv ..... Done
xcelium: source /opt/cadence/XCELLUM803/tools/xcelium/files/xmsimrc
xcelium: run
xsim: *W_SHMPT: Some objects excluded from $shm_probe due to optimizations.
File: ./mb_cpu.v, line = 28, pos = 11
Scope: mb_cpu
Time: 0 F3 + 0
Simulation complete via $finish(1) at time 1201 NS + 0
./mb_cpu.v:20 # $finish;
xcelium: exit
Xfce Menu | uranus.ece.iit.edu | 2 |
```

Fig 55: RTL Simulation.

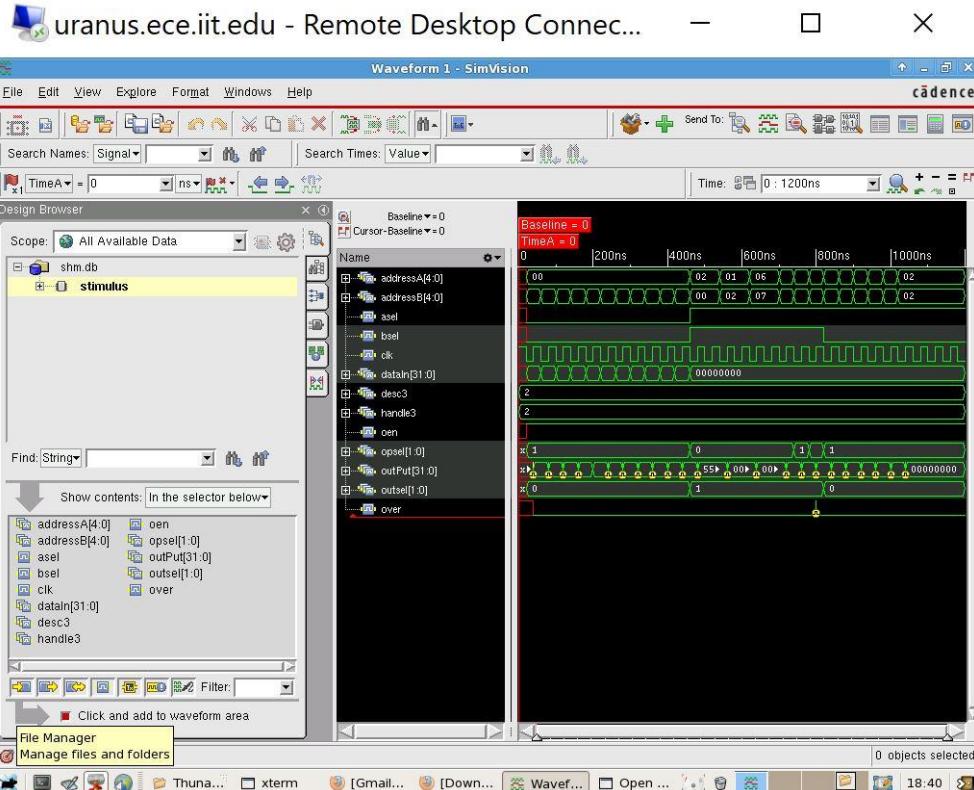


Fig 56: Simvision.

c. Carry Skip Adder:

```

uranus.ece.iit.edu - Remote Desktop Connec... - X

xsimlab: ./cpu_CSR.v:574: c_over_1
xsimlab: ./cpu_CSR.v:574: c_over_2
CSL4 cs0_3(.s(s[3:0]), .cout(c[0]), .a(a[3:0]), .b(b[3:0]), .cin(cin));
xsimlab: MU_CUWSP (.cpu_CSR.v:582[10]: 2 output ports were not connected;
xsimlab: ./cpu_CSR.v:583): c_over_1
xsimlab: ./cpu_CSR.v:583): c_over_2
CSL4 cs4_7(.s(s[7:4]), .cout(c[1]), .a(a[7:4]), .b(b[7:4]), .cin(cin));
xsimlab: MU_CUWSP (.cpu_CSR.v:583[10]: 2 output ports were not connected;
xsimlab: ./cpu_CSR.v:583): c_over_1
xsimlab: ./cpu_CSR.v:583): c_over_2
CSL4 cs0_11(.s(s[11:8]), .cout(c[2]), .a(a[11:8]), .b(b[11:8]), .cin(cin));
xsimlab: MU_CUWSP (.cpu_CSR.v:584[11]: 2 output ports were not connected;
xsimlab: ./cpu_CSR.v:583): c_over_1
xsimlab: ./cpu_CSR.v:583): c_over_2
          Top level design units:
          stimy ..... Done
          Building instance overlay tables: ..... Done
          Generating native compiled code:
          worklib.stimuluv <0x19f0146c>
          streams: 13, words: 32994
          Building instance specific data structures.
          Loading native compiled code:
          Done
          Design hierarchy summary:
          Instances Unique
          Modules: 6575 31
          Primitives: 726 6
          Registers: 2166 14
          Scalar wires: 3570 -
          Expanded wires: 1198 41
          Vectorized wires: 6 -
          Aligned blocks: 2156 4
          Initial blocks: 3 3
          Cont. assignments: 10 12
          Pseudo assignments: 43 43
          Writing initial simulation snapshot: worklib.stimuluv
          Loading snapshot worklib.stimuluv: ..... Done
          xcclium source /apps/cadence/XCCLIMB005/tools/xcclium/files/xsimrc
          xcclium run
          xsim: "U_SharpOff": Some objects excluded from $shm_probe due to optimizations.
          Filter: /tb.cpu.v, line = 28, pos = 11
          Scope: stimulus
          Time: 0 FS + 0
          Simulation complete via $finish(1) at time 1201 NS + 0
          ./tb.cpu.v:20 #1 $finish;
          xcclium exit
stipura@uranus.ece.iit.edu:~% 

```

Fig 57: RTL Simulation.

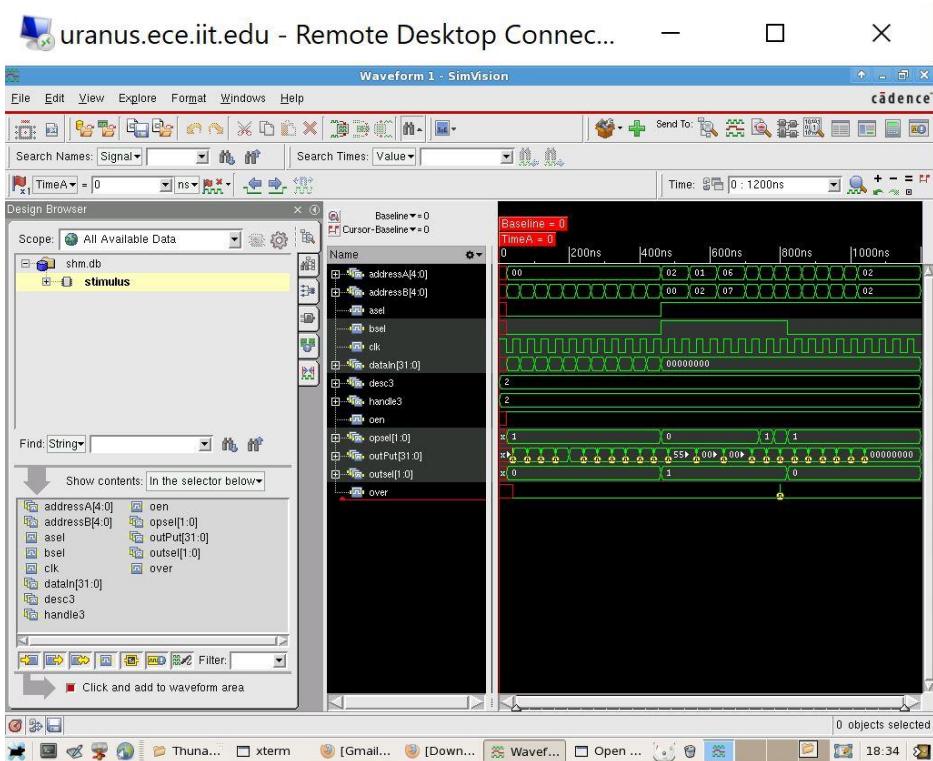


Fig 58: Simvision.

d. Carry Select Adder:

```

uranus.ece.iit.edu - Remote Desktop Connec... - □ X
xterm
[35e4 c3(.sel([11:0]), .cout(c[3]), .a(a[11:0]), .b(b[11:0]), .cin(c[2]));
xwlab: "U_CUMMP (.cpu_CSel.v_59310); 1 output port was not connected;
xwlab: (.cpu_CSel.v_593) : over
Top level design units:
  - stimulus
Building instance overlay tables: ..... Done
Generating native compiled code:
  worklib.aluvv <0x253149fe>
    streams: 32, words: 6720
  worklib.aluvv <0x0d000000>
    streams: 2, words: 420
  worklib.logic.fnv <0x5afab3e5>
    streams: 1, words: 1113
  worklib.aluvv <0x61260000>
    streams: 1, words: 1246
  worklib.aluvv <0x612601d7>
    streams: 0, words: 0
  worklib.aluvv <0x3f564090>
    streams: 0, words: 0
  worklib.aluvv <0x0d000000>
    streams: 0, words: 0
  worklib.aluvv <0x61260185>
    streams: 1, words: 208
  worklib.dregv <0x60a2e3c5>
    streams: 2, words: 264
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary
  Instances Unique
  Modules: 6607 31
  Primitives: 7507 6
  Registers: 2156 14
  Scopes: 597 -
  Expanded wires: 1230 49
  Vectorized wires: 6 -
  Always blocks: 2156 4
  Initial blocks: 3 3
  Data flow ports: 9 41
  Pseudo assignments: 43 43
Writing initial simulation snapshot: worklib.stimulus.v
Loading snapshot worklib.stimulus.v ..... Done
xcelium source /apps/cadence/XCELIUM03/tools/xcelium/files/xsimrc
xcelium run
xsim: "U_SHMPORT: Some objects excluded from $shm_probe due to optimizations.
  File: ./tb.cpu.v, line = 28, pos = 11
  Scope: stimulus
  Time: 0 FS + 0
Simulation complete via $finish(1) at time 1201 NS + 0
./tb.cpu.v:30  #1 $finish;
xcelium exit
stipura@uranus [ece429 - File Manager]

```

Fig 59: RTL Simulation.

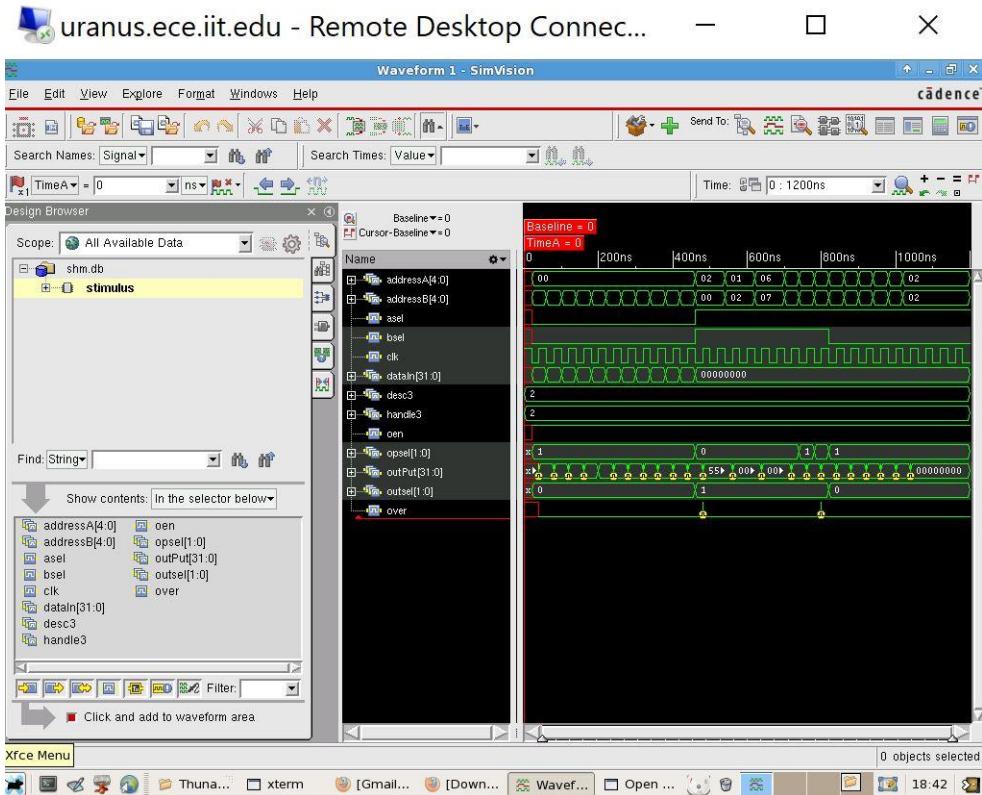


Fig 60: Simvision.

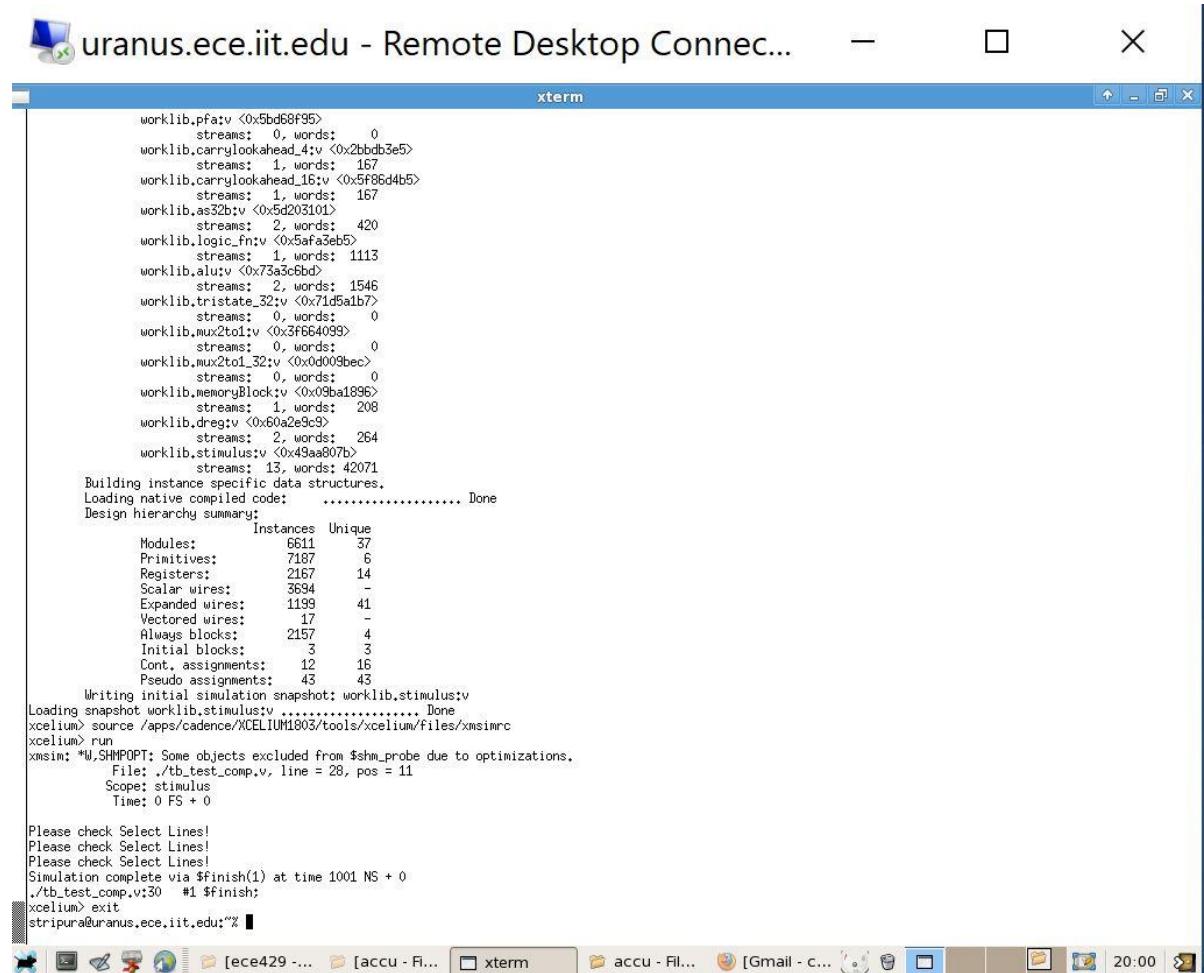
f. Post Synthesis Gate Level Delay:

		CRA (ns)	CLA (ns)	CSA (ns)	CSeA (ns)
Calculate the Path Delay for each Operation (Post-Synthesis Gate-Level Delay)	5555_5555 + 5	2.2	2.1	2.14	1.09
	AAAA_AAAA + 5555_5555	2.675	2.89	2.56	1.45
	0000_00C8 + 0000_012C	2.33	2.68	2.1	1.6
	5 + 0000_000A	2.7	2.5	2.21	1.5
	FFFF_FFFF - 0000_0001	2.65	2.37	2.24	2.01
	FFFF_FFFF + 0000_0001	2.4	2.2	2.2	1.78
	5555_5555 - 5	2.07	2.25	1.7	1.6
	AAAA_AAAB + 5555_5555	2.39	2.29	1.6	1.59

If the design of the adder requires more bits to work, its path delay will be greater than others. Since the Carry Select Adder uses fewer bits to accomplish addition, it has the least path delay.

2. Case Study 2:

In any operating system and device interfaces, the comparison of two binary data for equality is essentially a performed process. As a comparator, a circuit does this process of comparing the equality between binary data. It compares two separate variables of the same length, and the results of the comparison is given. The output can be one of the three possibilities, A>B, A<B, A=B. when f1=1, it implies that the two integers are equal, else f0 is checked. The number of comparators used depends on the number of bits of the input variables. The number of multiplexers used in the higher levels decreases as the tree structure us used to build the comparator. The testbench is attached at the last in appendix.



```
uranus.ece.iit.edu - Remote Desktop Connec... — □ ×
xterm
worklib.pfa:v <0x5bd68f95>
    streams: 0, words: 0
worklib.carrylookahead_4:v <0x2bbdb3e5>
    streams: 1, words: 167
worklib.carrylookahead_16:v <0x5f86d4b5>
    streams: 1, words: 167
worklib.as32bv <0x5d203101>
    streams: 2, words: 420
worklib.logic_fn:v <0x5afa2eb5>
    streams: 1, words: 1113
worklib.aluv <0x73a2c0bd>
    streams: 2, words: 1546
worklib.tristate_32:v <0x71d5a1b7>
    streams: 0, words: 0
worklib.mux2to1v <0x3f664099>
    streams: 0, words: 0
worklib.mux2to1_32:v <0xd0d009bec>
    streams: 0, words: 0
worklib.memoryBlock:v <0x09ba1896>
    streams: 1, words: 208
worklib.dreg:v <0x60a2e9c9>
    streams: 2, words: 264
worklib.stimulus:v <0x43aa807b>
    streams: 13, words: 42071
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
      Instances Unique
Modules:       6611   37
Primitives:    7187    6
Registers:    2167   14
Scalar wires:  3694    -
Expanded wires: 1199   41
Vectorized wires: 17    -
Always blocks: 2157   4
Initial blocks: 3     3
Cont. assignments: 12   16
Pseudo assignments: 43   43
Writing initial simulation snapshot: worklib.stimulus:v
Loading snapshot worklib.stimulus:v ..... Done
xcelium> source /apps/cadence/XCELUM1803/tools/xcelium/files/xmsimrc
xcelium> run
xmsim: #U,SHMPOPT: Some objects excluded from $shm_probe due to optimizations.
File: ./tb_test_comp.v, line = 28, pos = 11
Scope: stimulus
Time: 0 FS + 0

Please check Select Lines!
Please check Select Lines!
Please check Select Lines!
Simulation complete via $finish(1) at time 1001 NS + 0
./tb_test_comp.v:30  #1 $finish;
xcelium> exit
stripura@uranus.ece.iit.edu:"% "
```

Fig 61: RTL Simulation.

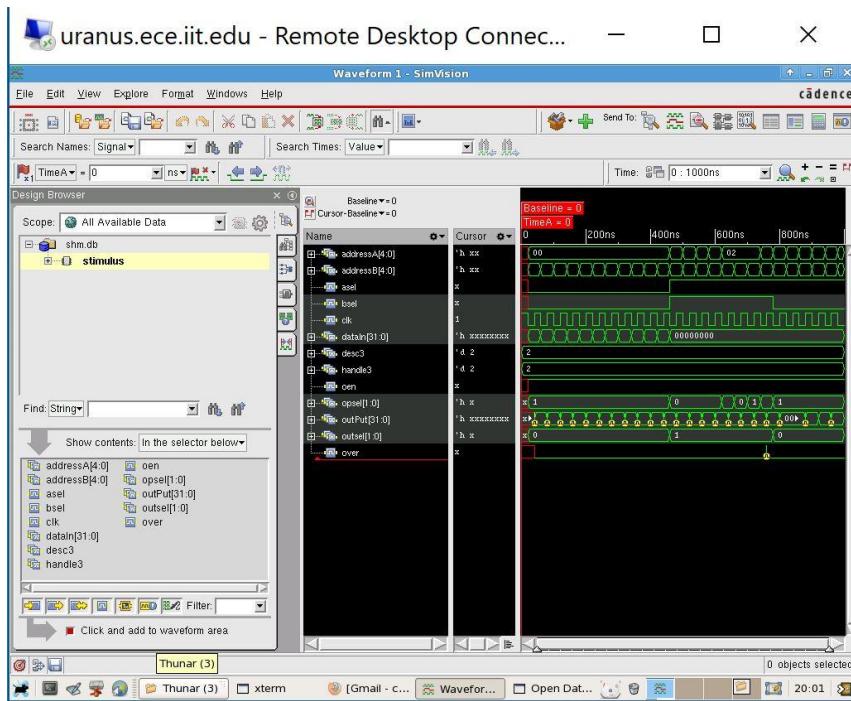


Fig 62: Simvision.

```

0:00:03 48776.2 0.00 0.0 3.0
0:00:03 48776.2 0.00 0.0 3.0

Beginning Design Rule Fixing (max_capacitance)

ELAPSED          WORST NEG TOTAL NEG DESIGN
TIME           SLACK    SLACK    RULE COST   ENDPOINT
-----|-----|-----|-----|-----|-----|
0:00:03 48776.2 0.00 0.0 3.0
Loading db file '/apps/FreePDK45/osu_soc/lib/Files/gsc145nm.db'

Optimization Complete
Warning: Design 'cpu' contains 1 high-fanout nets. A fanout number of 1000 will be used for delay calculations involving these nets. (TIM-134)
Net 'clk': 1628 load(s), 1 driver(s)
1
check_design
*****
check_design summary:
Version: G-2012.06
Date: Thu Dec 3 20:08:41 2020
*****
Name          Total
Designs        1
  Black box (LINT-55) 1

Information: Design 'tree_comp' does not contain any cells or nets. (LINT-55)
1
#report_constraint -all_violators
set filename [format "%s%s" $my_toplevel ".vh"]
cpu.vh
write -f verilog -output $filename
Writing verilog file '/home/stripura/Desktop/ece429/accu/cpu.vh'.
1
set filename [format "%s%s" $my_toplevel ".sdc"]
cpu.sdc
write_sdc $filename
1
#set filename [format "%s%s" $my_toplevel ".db"]
#write -f db -hier -output $filename -xg_Force_db
redirect timing.rep { report_timing }
redirect cell.rep { report_cell }
redirect power.rep { report_power }
quit

Thank you...
Elapsed Time = 2:24.85, CPU Time = 142.565
stripura@uranus.ece.iit.edu:~$ 

```

Fig 63: Logic Synthesis using Design Compiler.

uranus.ece.iit.edu - Remote Desktop Connec...

timing.rep (~/Desktop/ece429/accu) - gedit

```

File Edit View Search Tools Documents Help
timing.rep x
0/20771 (XOR2X1) 0.05 5.44 r
U1266/Y (XOR2X1) 0.07 5.51 r
a/l3/f2308/U5/Y (XNOR2X1) 0.06 5.57 r
a/l3/f2308/U2/Y (XOR2X1) 0.07 5.64 r
a/l3/f247/U5/Y (XNOR2X1) 0.06 5.71 r
a/l3/f247/U2/Y (XOR2X1) 0.07 5.78 r
a/l3/f256/U5/Y (XNOR2X1) 0.06 5.84 r
a/l3/f256/U2/Y (XOR2X1) 0.07 5.91 r
a/l3/f265/U5/Y (XNOR2X1) 0.06 5.97 r
a/l3/f265/U2/Y (XOR2X1) 0.07 6.04 r
a/l3/f274/U5/Y (XNOR2X1) 0.06 6.11 r
a/l3/f274/U2/Y (XOR2X1) 0.07 6.18 r
a/l3/f283/U5/Y (XNOR2X1) 0.06 6.24 r
a/l3/f283/U2/Y (XOR2X1) 0.07 6.31 r
a/l3/f292/U5/Y (XNOR2X1) 0.06 6.37 r
a/l3/f292/U2/Y (XOR2X1) 0.05 6.42 f
U1702/Y (AND2X1) 0.03 6.45 f
a/l3/rc31/qout_reg/D (DFFP0SX1) 0.00 6.45 f
data arrival time 6.45

clock clk (rise edge) 16.00 16.00
clock network delay (ideal) 0.00 16.00
a/l3/rc31/qout_reg/CLK (DFFP0SX1) 0.00 16.00 r
library setup time -0.06 15.94
data required time 15.94

data required time 15.94
data arrival time -6.45

slack (MET) 9.49

1

```

xterm Ln 16, Col 1 INS

Fig 64: timing.rep.

uranus.ece.iit.edu - Remote Desktop Connec...

cell.rep (~/Desktop/ece429/accu) - gedit

```

File Edit View Search Tools Documents Help
cell.rep x
0/1/1/1/1/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t8/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t9/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t10/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t11/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t12/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t13/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t14/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t15/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t16/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t17/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t18/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t19/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t20/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t21/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t22/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t23/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t24/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t25/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t26/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t27/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t28/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t29/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t30/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t31/b1 TBUFX2 gscl45nm 3.754400 n
wb/bd/me0/qout_reg DFFP0SX1 gscl45nm 7.978100 n
wb/bd/me1/qout_reg DFFP0SX1 gscl45nm 7.978100 n
wb/bd/me2/qout_reg DFFP0SX1 gscl45nm 7.978100 n
wb/bd/me3/qout_reg DFFP0SX1 gscl45nm 7.978100 n
wb/bd/me4/qout_reg DFFP0SX1 gscl45nm 7.978100 n

Total 14414 cells 48776.225288
1

```

[accu - File Manager] Ln 1, Col 1 INS

Fig 65: cell.rep.

```

Global Operating Voltage = 1.1
Power-specific unit information :
  Voltage Units = 1V
  Capacitance Units = 1.000000pf
  Time Units = 1ns
  Dynamic Power Units = 1mW    (derived from V,C,T units)
  Leakage Power Units = 1nW

Cell Internal Power = 1.6333 mW (89%)
Net Switching Power = 211.5907 uW (11%)
Total Dynamic Power = 1.8449 mW (100%)
Cell Leakage Power = 262.2271 uW

          Internal      Switching      Leakage      Total
Power Group     Power        Power        Power       Power  ( %   ) Attrs
-----
io_pad          0.0000      0.0000      0.0000      0.0000 ( 0.00%)
memory          0.0000      0.0000      0.0000      0.0000 ( 0.00%)
black_box        0.0000      1.7251e-05  0.0000      1.7251e-05 ( 0.00%)
clock_network   0.0000      0.0000      0.0000      0.0000 ( 0.00%)
register         1.4557      3.2698e-02  8.9337e+04  1.5777 ( 74.88%)
sequential       5.2460e-03  1.2250e-02  784.1055  1.8280e-02 ( 0.87%)
combinational   0.1723      0.1666      1.7210e+05  0.5111 ( 24.25%)
-----
Total           1.6333 mW    0.2116 mW    2.6222e+05 nW   2.1071 mW
1

```

Fig 66: power.rep.

```

2020-Dec-03 20:17:14 (2020-Dec-04 02:17:14 GMT); 10%
2020-Dec-03 20:17:14 (2020-Dec-04 02:17:14 GMT); 15%
2020-Dec-03 20:17:14 (2020-Dec-04 02:17:14 GMT); 20%
2020-Dec-03 20:17:14 (2020-Dec-04 02:17:14 GMT); 25%
2020-Dec-03 20:17:14 (2020-Dec-04 02:17:14 GMT); 30%
2020-Dec-03 20:17:14 (2020-Dec-04 02:17:14 GMT); 35%
2020-Dec-03 20:17:14 (2020-Dec-04 02:17:14 GMT); 40%
2020-Dec-03 20:17:14 (2020-Dec-04 02:17:14 GMT); 45%
Calculating internal and leaked power
2020-Dec-03 20:17:14 (2020-Dec-04 02:17:14 GMT); 50%
2020-Dec-03 20:17:14 (2020-Dec-04 02:17:14 GMT); 55%
2020-Dec-03 20:17:15 (2020-Dec-04 02:17:15 GMT); 60%
2020-Dec-03 20:17:15 (2020-Dec-04 02:17:15 GMT); 65%
2020-Dec-03 20:17:15 (2020-Dec-04 02:17:15 GMT); 70%
2020-Dec-03 20:17:15 (2020-Dec-04 02:17:15 GMT); 75%
2020-Dec-03 20:17:15 (2020-Dec-04 02:17:15 GMT); 80%
2020-Dec-03 20:17:15 (2020-Dec-04 02:17:15 GMT); 85%
2020-Dec-03 20:17:15 (2020-Dec-04 02:17:15 GMT); 90%
2020-Dec-03 20:17:15 (2020-Dec-04 02:17:15 GMT); 95%
Finished Calculating power
2020-Dec-03 20:17:16 (2020-Dec-04 02:17:16 GMT)
*

Total Power
-----
Total Internal Power: 5.166 56.45%
Total Switching Power: 3.721 40.66%
Total Leakage Power: 0.2643 2.888%
Total Power: 9.152

report_power consumed time (real time) 00:00:03 : peak memory (480M)
Output file is power_final
*****
* Encounter script finished *
* Results: *
* -----
* Layout: final.gds2 *
* Netlist: final.v *
* Timing: timing.rsp_6.final *
* Areas: areas_final *
* Power: power_final *
* Type 'win' to get the Main Window *
* or type 'exit' to quit *
*****
encounter 1> reportGateCount -limit 0
Gate area 2.6158 um^2
[0] cpu Gates=15006 Cells=14498 Area=44508.4 um^2
encounter 2>

```

Fig 67: Area Report.

```

Total Power
-----
Total Internal Power: 5.166 96.45%
Total Switching Power: 3.721 40.55%
Total Leakage Power: 0.2643 2.88%
Total Power: 9.152

Group          Internal Power   Switching Power   Leakage Power   Total Power   Percentage (%)
-----
Sequential      2,444           0,3693          0,09012       2,904       31,73
Macro          0               0               0               0               0
IO              0               0               0               0               0
Combinational   2,624           2,116           0,1721        4,912       53,67
Clock (Combinational) 0,09753  1,236           0,000296      1,336       14,6
Clock (Sequential) 0               0               0               0               0
Total          5,166           3,721           0,2643        9,152       100

Rail           Voltage Internal Power   Switching Power   Leakage Power   Total Power   Percentage (%)
-----
vdd            1,1    5,166           3,721           0,2643        9,152       100

Clock          Internal Power   Switching Power   Leakage Power   Total Power   Percentage (%)
-----
clk            0,09753         1,236           0,000296      1,336       14,6
Total          0,09753         1,236           0,000296      1,336       14,6

* Power Distribution Summary:
* Highest Average Power: clk_L4_I10 (INVX8): 0.01365
* Highest Leakage Power: ab/ram/mer2/11/we31/qout_reg (DFFPOSX1): 5.498e-05
* Total Cap: 1.79231e+10 F
* Total instances in design: 14498
* Total instances in design with no power: 0
* Total instances in design with no activity: 0
* Total Fillers and Decap: 0

report_power consumed time (real time) 00:00:00 : peak memory (480M)

```

The terminal window also shows the file manager icon in the taskbar.

Fig 68: Power Report.

```

#####
# Generated by: Cadence Encounter 10.13-s292_1
# OS: Linux x86_64(Host ID uranus.ece.iit.edu)
# Generated on: Thu Dec 3 20:16:58 2020
# Design: cpu
# Command: report_timing -nworst 10 -net > timing.rep.5.final
#####

Path 1: MET Setup Check with Pin a/l3/rc31/qout_reg/CLK
Endpoint: a/l3/rc31/qout_reg/D (^) checked with leading edge of 'clk'
Beginpoint: m0pd/bb/me2/qout_reg/Q (v) triggered by leading edge of 'clk'
Other End Arrival Time 0.324
- Setup 3.132
+ Phase Shift 16.000
= Required Time 13.192
- Arrival Time 10.120
= Slack Time 3.072
  Clock Rise Edge 0.000
  + Clock Network Latency (Prop) 0.335
  = Beginpoint Arrival Time 0.335
+-----+
| Pin | Edge | Net | Cell | Delay | Arrival Time | Required Time |
+-----+
| m0pd/bb/me2/qout_reg/CLK | ^ | clk_L4_N63 | DFFPOSX1 | 0.308 | 0.335 | 3.407 |
| m0pd/bb/me2/qout_reg/Q | v | B[2] | AND2X1 | 0.061 | 0.643 | 3.715 |
| U1865/B | v | B[1] | AND2X1 | 0.116 | 0.704 | 3.776 |
| U1865/Y | v | a/l3/p0[2] | AND2X1 | 0.000 | 0.820 | 3.892 |
| U1242/A | v | a/l3/p0[2] | AND2X1 | 0.038 | 0.821 | 3.892 |
| U1242/Y | v | a/l3/f02/n3 | AND2X1 | 0.000 | 0.859 | 3.931 |
| U1243/A | v | a/l3/f02/n3 | INVX1 | 0.000 | 0.859 | 3.931 |
| U1243/Y | ^ | n683 | INVX1 | 0.004 | 0.863 | 3.935 |
| a/l3/f02/U3/C | ^ | n683 | OAI21X1 | 0.000 | 0.863 | 3.935 |
| a/l3/f02/U3/Y | v | a/l3/c0[1] | OAI21X1 | 0.132 | 0.995 | 4.067 |
| U1112/A | v | a/l3/c0[1] | TMVX1 | 0.000 | 0.005 | 4.067 |

```

The terminal window also shows the file manager icon in the taskbar.

Fig 69: timing.rep.5.final.

Encounter is mainly used to place the standard cells and route to the interconnects. The Verilog model output from encounter is used for post P&R simulation. Furthermore, from the output file timing.rep, required time (9.49) is obtained. Therefore, maximum clock frequency should be 10.537MHz.

Conclusion:

In this project, a 32-bit CPU was successfully designed and implemented using four different adders along with the ALU design with the help of a comparator. As discussed above, the RTL Simulations, Logic Synthesis and Post P&R Simulations have been carried out successfully. The maximum frequency at which the circuit can run is determined. We have also determined the timing, number of cells and the power. In addition, a Verilog model of 32-bit comparator is created and added to the ALU. Therefore, we have completed the required tasks and successfully achieved the objective of the program.

APPENDIX:

Case study 2:

```
module stimulus;

parameter T = 20;
reg [31:0] datain;
reg [1:0] opsel, outsel;
reg [4:0] addressA, addressB;
reg asel, bsel, oen, clk;

wire [31:0] outPut;
wire over;
integer handle3,desc3;
// Instantiate the design block counter
cpu proj(addressA, addressB, dataIn, asel, bsel, clk, opsel, outsel, oen, outPut, over);
initial
begin
clk = 1'b1;
forever #T clk = ~clk;
end
initial
begin
handle3 = $fopen ("stim_proj.out");
$shm_open("shm.db",1);
$shm_probe(stimulus,"AS");
#1000 $shm_close();
#1 $finish;
end
always
begin
desc3=handle3;
#1 $fdisplay(desc3, $time, "clk=%b, addressA=%d, addressB=%d, dataIn=%d, opsel=%d,
outsel=%d, asel=%d, bsel=%d, oen=%d, OUT=%d", clk, addressA, addressB, dataIn, opsel,
outsel, asel, bsel, oen, outPut);
end
// Stimulate the Input Signals
initial
begin
// 1. store 0000_0005 in [0]
#T
addressA = 5'b00000;
addressB = 5'b00000;
dataIn = 32'h0000_0005;
opsel = 2'b01;
outsel = 2'b00;
asel = 0;
bsel = 0;
```

```

oen = 1;
#(T*2)
// 2. store AAAA_AAAA in [1]
addressA=5'b00000;
addressB= 5'b00001;
dataIn = 32'hAAAA_AAAA;y
opsel = 2'b01;
outsel = 2'b00;
asel = 0;
bsel = 0;
oen = 1;
#(T*2)
// 3. store 5555_5555 in [2]
addressA = 5'b00000;
addressB = 5'b00010;
dataIn = 32'h5555_5555;
opsel = 2'b01;
outsel =2'b00;
asel = 0;
bsel = 0;
oen = 1;
#(T*2)
// 4. store 0000_000A in [3]y
addressA = 5'b00000;
addressB = 5'b00011;
dataIn = 32'h0000_000A;
opsel = 2'b01;
outsel =2'b00;
asel = 0;
bsel = 0;
oen = 1;
#(T*2)
// 5. store 0000_0001 in [4]
addressA = 5'b00000;
addressB = 5'b00100;
dataIn = 32'h0000_0001;
opsel = 2'b01;
outsel =2'b00;
asel = 0;
bsel = 0;
oen = 1;
#(T*2)
// 6. store FFFF_FFFF in [5]
addressA = 5'b00000;
addressB = 5'b00101;
dataIn = 32'hFFFF_FFFF;
opsel = 2'b01;
outsel =2'b00;

```

```

asel = 0;
bsel = 0;
oen = 1;
#(T*2)
// 7. store 0000_00C8 in [6]
addressA = 5'b00000;
addressB = 5'b00110;
dataIn = 32'h0000_00C8;
opsel = 2'b01;
outsel =2'b00;
asel = 0;
bsel = 0;
oen = 1;
#(T*2)
// 8. store 0000_012C in [7]
addressA = 5'b00000;
addressB = 5'b00111;
dataIn = 32'h0000_012C;
opsel = 2'b01;
outsel =2'b00;
asel = 0;
bsel = 0;
oen = 1;
#(T*2)
// 9. store 0000_0001 in [8]
addressA = 5'b00000;
addressB = 5'b01000;
dataIn = 32'h0000_0001;
opsel = 2'b01;
outsel =2'b00;
asel = 0;
bsel = 0;
oen = 1;y
#(T*2)
// 10. store AAAA_AAAB in [9]
addressA = 5'b00000;
addressB = 5'b01001;
dataIn = 32'hAAAA_AAAB;
opsel = 2'b01;
outsel =2'b00;
asel = 0;
bsel = 0;
oen = 1;
#(T*2)
// 11. store AAAA_AAAB in [10]
addressA = 5'b00000;
addressB = 5'b01010;
dataIn = 32'h5555_5555;

```

```
opsel = 2'b01;
outsel =2'b00;
asel = 0;
bsel = 0;
oen = 1;
 #(T*2)
//12. ADD [2][0]
addressA = 5'd2;
addressB = 5'd0;
dataIn = 32'd0;
opsel = 2'b00;
outsel =2'b01;
asel = 1;
bsel = 1;
oen = 1;
 #(T*2)
//13. ADD [1][2]
addressA = 5'd1;
addressB = 5'd2;
dataIn = 32'd0;
opsel = 2'b00;
outsel =2'b01;
asel = 1;
bsel = 1;
oen = 1;
 #(T*2)
//14. ADD [6][7]
addressA = 5'd6;
addressB = 5'd7;
dataIn = 32'd0;
opsel = 2'b00;
outsel =2'b01;
asel = 1;
bsel = 1;
oen = 1;
 #(T*2)
//15. ADD [0][3]
addressA = 5'd0;
addressB = 5'd3;
dataIn = 32'd0;
opsel = 2'b00;
outsel =2'b01;
asel = 1;
bsel = 1;
oen = 1;
 #(T*2)
//16. SUB [2][4]
addressA = 5'd2;
```

```
addressB = 5'd4;
dataIn = 32'd0;
opsel = 2'b01;
outsel =2'b01;
asel = 1;
bsel = 1;
oen = 1;
 #(T*2)
//17. ADD [2][8]
addressA = 5'd2;
addressB = 5'd8;
dataIn = 32'd0;
opsel = 2'b00;
outsel =2'b01;
asel = 1;
bsel = 1;
oen = 1;
 #(T*2)
//18. SUB [2][0]
addressA = 5'd2;
addressB = 5'd0;
dataIn = 32'd0;
opsel = 2'b01;
outsel =2'b01;
asel = 1;
bsel = 1;
oen = 1;
 #(T*2)
//19. ADD [9][10]
addressA = 5'd9;
addressB = 5'd10;
dataIn = 32'd0;
opsel = 2'b00;
outsel =2'b01;
asel = 1;
bsel = 1;
oen = 1;
 #(T*2)
//20.READ [8]
addressA = 5'd8;
addressB = 5'd8;
dataIn = 32'd0;
opsel = 2'b01;
outsel =3'b000;
asel = 1;
bsel = 0;
oen = 1;
 #(T*2)
```

```
//21.READ [10]
addressA = 5'd10;
addressB = 5'd10;
dataIn = 32'd0;
opsel = 2'b01;
outsel =3'b000;
asel = 1;
bsel = 0;
oen = 1;
 #(T*2)
//22.READ [4]
addressA = 5'd4;
addressB = 5'd4;
dataIn = 32'd0;
opsel = 2'b01;
outsel =3'b000;
asel = 1;
bsel = 0;
oen = 1;
 #(T*2)
//23.READ [2]
addressA = 5'd2;
addressB = 5'd2;
dataIn = 32'd0;
opsel = 2'b01;
outsel =3'b000;
asel = 1;
bsel = 0;
oen = 1;
 #(T*2)
//24. READ [7]
addressA = 5'd7;
addressB = 5'd7;
dataIn = 32'd0;
opsel = 2'b01;
outsel =3'b000;
asel = 1;
bsel = 0;
oen = 1;
 #(T*2)
//25. READ [3]
addressA = 5'd3;
addressB = 5'd3;
dataIn = 32'd0;
opsel = 2'b01;
outsel =3'b000;
asel = 1;
bsel = 0;
```

```
oen = 1;
 #(T*2)
 //26. CMP [8][10]
 addressA = 5'd8;
 addressB = 5'd10;
 dataIn = 32'd0;
 opsel = 2'b00;
 outsel =3'b100;
 asel = 1;
 bsel = 1;
 oen = 1;
 #(T*2)
 //27. CMP [4][2]
 addressA = 5'd4;
 addressB = 5'd2;
 dataIn = 32'd0;
 opsel = 2'b00;
 outsel =3'b100;
 asel = 1;
 bsel = 1;
 oen = 1;
 #(T*2)
 //28. CMP [3][7]
 addressA = 5'd3;
 addressB = 5'd7;
 dataIn = 32'd0;
 opsel = 2'b00;
 outsel =3'b100;
 asel = 1;
 bsel = 1;
 oen = 1;
 #(T*2)
 //29. READ [10]
 addressA = 5'd10;
 addressB = 5'd10;
 dataIn = 32'd0;
 opsel = 2'b01;
 outsel =3'b000;
 asel = 1;
 bsel = 0;
 oen = 1;
 #(T*2)
 //30. READ [2]
 addressA = 5'd2;
 addressB = 5'd2;
 dataIn = 32'd0;
 opsel = 2'b01;
 outsel =3'b000;
```

```
asel = 1;
bsel = 0;
oen = 1;
#(T*2)
//31. READ [7]
addressA = 5'd7;
addressB = 5'd7;
dataIn = 32'd0;
opsel = 2'b01;
outsel =3'b000;
asel = 1;
bsel = 0;
oen = 1;
end
endmodule
```