Name: Simon Gezae

ID: 19830

Exercise: Lab 7

1. What is the fastest clock frequency given the following circuit and delay values?
2. Is there potential for a hold violation?

**Diagram

Description automatically generated**

We have three paths two of them are DFF -> NOR -> NOR -> DFF and the third one is DFF -> NOR-> DFF. The critical path is DFF -> NOR -> NOR -> DFF and we will use it to find the maximum delay the circuit should have to avoid any violation.

Delay = Tclock-Q + Tnor+Tnor+Tsu\_max+Tskew

Max Delay = 5+3+3+1+1 = 13ns

Given the delay value the fastest clock frequency is:

Clock Frequency = 1/delay = 1/13ns = 76.923077 MHz

Hold time Thold is minimum amount of time that the receiving component must hold a data input signal after it is received to ensure that it is correctly registered.

Thold

Since T hold of the circuit is 2ns and it is less than 3ns we don’t have hold time violation