Lab\_1 assignment

1. Result after running the Verilog program in EDA playground.

Graphical user interface, text, application

Description automatically generated

1. Based on the module *gates*, draw the digital circuit schematic

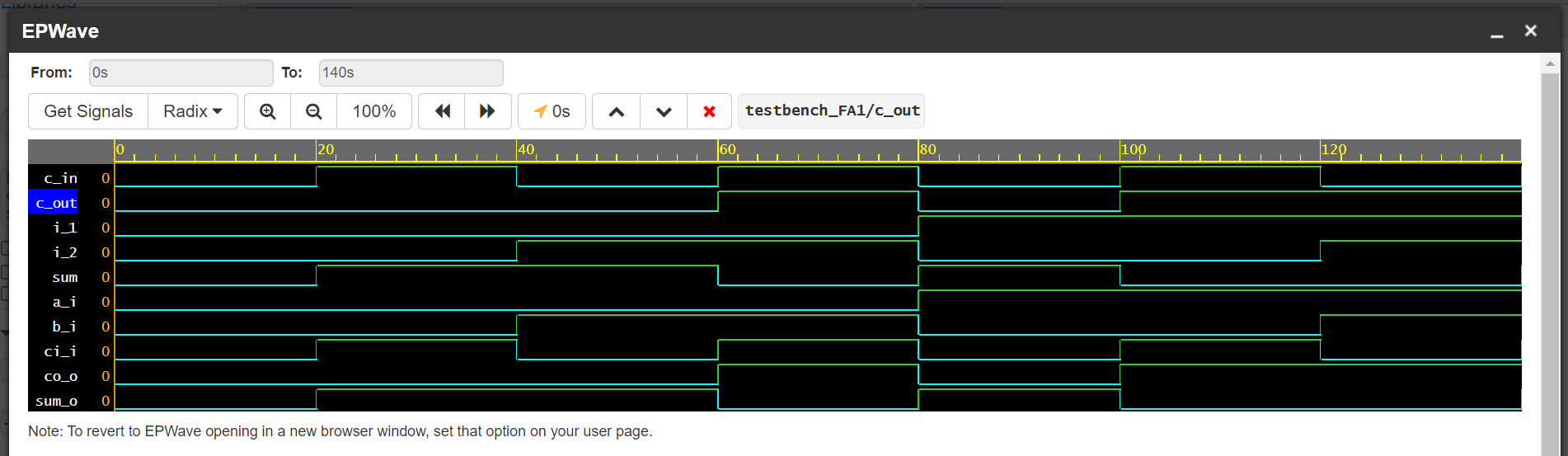
Graphical user interface, text

Description automatically generated

Diagram

Description automatically generated

3)



Testbench

Graphical user interface, text, application, whiteboard

Description automatically generated

A picture containing table

Description automatically generated