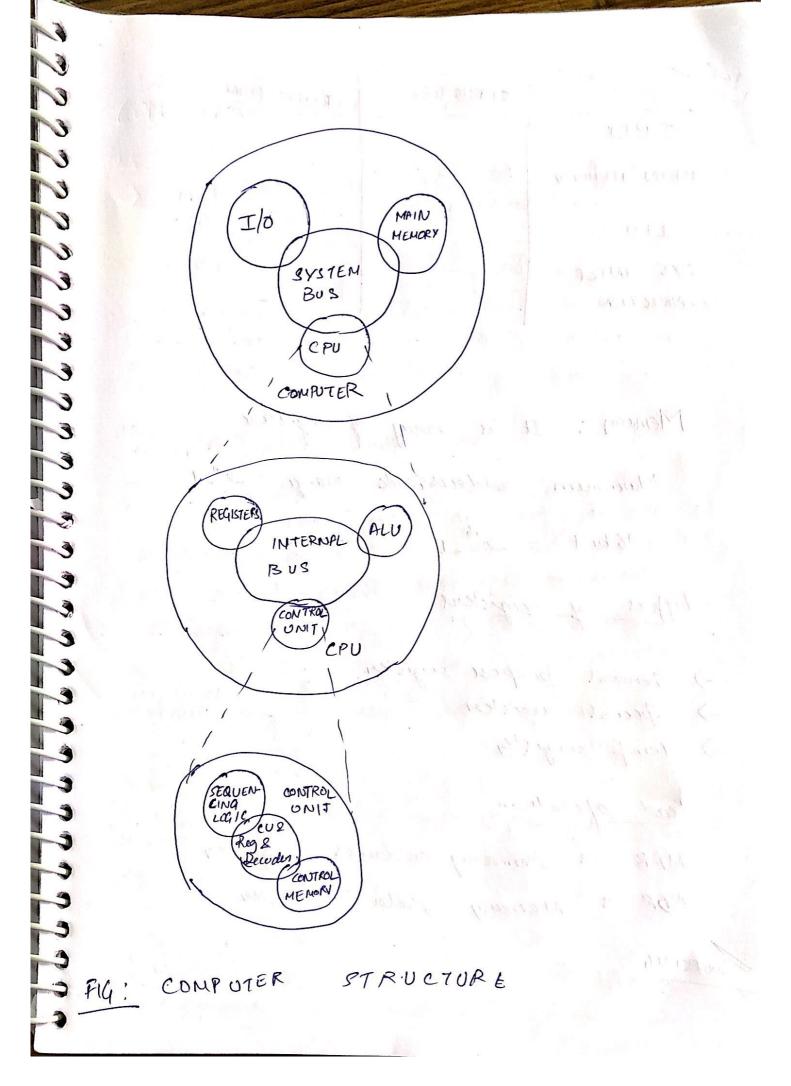
1

WELLER BEILLUS CINE 28 2 2 23 110 86 871 AND Computer Auchitecture (cA) enfers to those attributes of a system visible to a programmer on those attoributes the logical dinect impact on Instanction set Derchitecture (ISA) is a often used interchangabelly with Computer Auchitecture ONEDTE REPRESENTE CHURE of the tent in MICROARCHITECTURE AR CHITECTURE NS - Abstraction Layer provided to estware (3/w). Duogrammer vicible state CMEM l REq) operatore CINST & How they work) Execution Semantics (INTERRUPTS) 6 IMPUT / OUTPUT 2 6 DATA TYPES /3/2E 6 MICROARCHITECTURE / ORGANUISATION ES TRAPE OFF ON HON TO MAPLEMENT ISA FOR -SOME METRIC (SPEED, ENERGY, COST). 17 Li 40: PIPELINE PEPTH, NO. OF PIPELINES,

CACHE SIZE, 4' AREA, PEAR POWER & EXECUTION,



CPU MAIN MEMORY 110 SYS INTER-CONNECTION Memory: It is array of negisters Maximum addoussable orange = 2 1-1 16 bit = 216_1 Types of orgisters -) General purpost origister. -> Special origister. -) Temp ougistly Read operation MPR -s Memory address register MOR & memory data orgister WORKING 8 110 MINO 3