Lab 02

Lab02

Part 1:

Objective: **To become familiar with the Circuit Simulation using ModelSim:**

1) Perform the tutorial "***ModelSim_GUI_introduction(22).pdf***"

- Create a new folder, called Lab2Tutorial in your ENSC252 folder. Create a project in Quartus II directed to this folder. Use the VHDL code provided in Section 3 of the tutorial.
- Thereafter when you are ready to simulate the design, launch Modelsim, redirecting project location to this project folder (as directed in pg. 3).
- Modelsim will create a "work" folder in your project folder. This is a default "modelsim" library and folder name used to compile your design in Modelsim (versus Quartus).
- Write notes summarizing the procedures and tasks that are performed when simulating a circuit using ModelSim. We will be using the Modelsim method for majority of the semester.

Part 2:

Objective: **Creating Structural descriptions in VHDL:**

2) Create another new folder called OddThing in your ENSC252 folder.

- Write the **truth table** for a circuit that determines whether a 4-bit pattern has an ODD count of '1's. Assume that this circuit is called **OddThing**.
- Determine and write down the canonical SOP for OddThing. Simplify if possible.
- Start Quartus II. Create a new project and folder called OddThing in a newly created Lab2 directory. Create a new VHDL file called OddThing.vhd using Quartus. Design the VHDL entity and description for OddThing based on your function. Synthesize and ensure there are no syntax issues.
- Compile the design and run a simulation using **ModelSim**. Verify that the results are correct.

Part 3:

Objective: **Using VHDL Testbenches with Modelsim**

3) Continuation of previous project OddThing. Exit Modelsim.

- You have been provided with a file called **OddThing_tb.vhd**. This is a testbench written in VHDL, equivalent to a coded version of the waveform you developed to test your circuit. Copy this file to your project folder using the Windows file explorer.
- Open the testbench in Quartus and analyze the code. Understand each line, and how they are used to collectively form your waveform simulation. A testbench is a way to input stimulus to your Device Under Test (DUT, i.e your system, OddThing, in this case), observe its output and verify correct functionality. **Read through the comments carefully**.
- Compile the OddThing project in Quartus. Once finished, launch ModelSim and navigate to your project's folder. Create a new Modelsim project called OddThing.
- Next, we must compile the design again in ModelSim. Go to "Compile" – "Compile All". Assuming your design is correct, the files will compile. Ensure that Modelsim has compiled the testbench file.

Part 3: Cont'd

➢In ModelSim, select "Simulate" – "Start Simulation". Expand the **work** folder and highlight **OddThing_tb.vhdl**. Ensure *work.OddThing_tb* appears in the "Design Unit(s)" field. Press OK.

➢In ModelSim, select "Simulate" – "Start Simulation". Expand the **work** folder and highlight **OddThing_tb.vhdl**. Ensure *work.OddThing_tb* appears in the "Design Unit(s)" field. Press OK.

- ➢ Next you will see various messages and windows appearing for simulation. Highlight the "**DUT**" field in the **sim-Default** window. Right-click the field and select "Add to" – "Wave" – "All Items in Region". This will open a waveform window.
- ➢ In the waveform window, press the (run –all) icon. Once the simulation stops running, press the black magnifying glass to view the entire simulation.

- ➢ Verify that you have obtained the same results as your hand assembled waveform and truth table
- ➢ To exit the simulation window, go to the main window and select "Simulate" - "End Simulation".

- ➢ **Each time you have finished simulating or re-adjust your VHDL files, you must compile (in ModelSim) and simulate again, repeating the steps presented in this section**.

Part 4:

Objective: **Instantiating VHDL components**

4) New Project.

➢Create a new folder called **OddCounter** in your Lab2 folder, and copy "***lights.vhd***" designed in Lab1 into this folder.
Setup a new project called **OddCounter**.
Add the file "***lights.vhd***" to this project. (***project -> add/remove files in project***)

➢Write a **truth table** for the circuit, described in "***lights.vhd***".

➢**Draw a structural diagram** showing how lights.vhd can be used (instantiated) three times to become OddThing. Label ALL **internal signal wires** and ALL **instances of lights**. Label the **ports**.
Refer to your lecture notes for the details.

➢Create a new file called OddCounter.vhd. (***file -> new -> Design Files -> VHDL***)
Translate your structural diagram into a VHDL Entity and description.
This will require you to instantiate lights.vhd and port map the components as described by your structural diagrams. Refer to your lecture notes and textbook for details of port maps.

➢Compile the design and Run a simulation using ModelSim. Create a file called **OddCounter_tb.vhd** to verify that the results are correct.