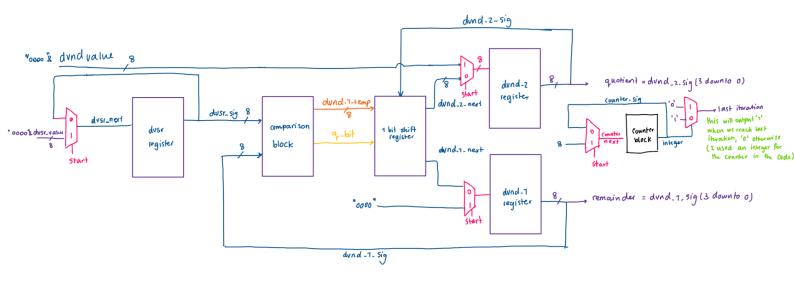
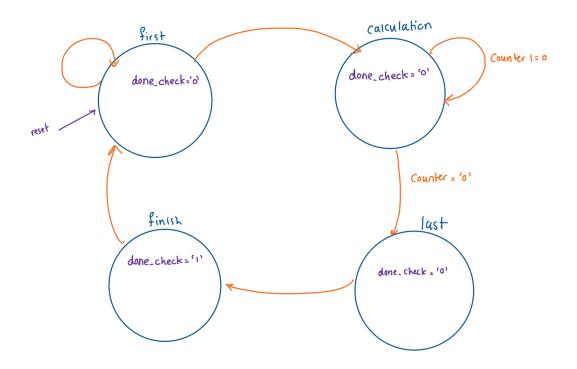
Datapath



FSM



Explanation

- For the datapath we have 4 registers where one of them is to store the divisor, 2 of them is to store the dividend and there is one left shift register which shifts the input to left by one bit.
- The inputs are the dividend and divisor and the outputs are the quotient, the remainder and the done_check value. They are all 4 bits long(which store numbers up to 15) and done_check is only 1 bit.
- In the FSM, we initially enter the first state where we input and assign the dividend and the divisor to an 8 bit signal as we add "0000" in front of them. Then we move to the calculation state where we continuously compare the value of the signal storing the dividend and the signal storing the divisor to output 1 or 0 for the quotient and subtract the values and shift the signal to left if required. We also have a counter value to store the number of iterations and we stay in the calculation state until the counter reaches 0 which means that is the last iteration and we enter the last state of the FSM. In this state there is no need to shift the dividend signal since the calculation has ended. Now we enter the finish state which indicates that the division operation is done and it outputs done_check='1' as well as the quotient and the remainder.

Modelsim Output for the test cases

```
🖳 Transcript 💳
 ** Note: Expected result for remainder = 3 Actual result for remainder = 3
    Time: 2080 ns Iteration: 2 Instance: /div tb
 ** Note: Expected result for quotient= 0 Actual result for quotient= 0
    Time: 2080 ns Iteration: 2 Instance: /div_tb
 ** Note: -----
    Time: 2080 ns Iteration: 2 Instance: /div tb
 ** Note: Test case 19: divisor = 2 dividend = 4
    Time: 2080 ns Iteration: 2 Instance: /div tb
 ** Note: Expected result for remainder = 0 Actual result for remainder = 0
    Time: 2190 ns Iteration: 2 Instance: /div_tb
 ** Note: Expected result for quotient= 2 Actual result for quotient= 2
    Time: 2190 ns Iteration: 2 Instance: /div tb
 ** Note: -----
    Time: 2190 ns Iteration: 2 Instance: /div tb
 ** Note: Test case 20: divisor = 2 dividend = 5
    Time: 2190 ns Iteration: 2 Instance: /div_tb
 ** Note: Expected result for remainder = 1 Actual result for remainder = 1
    Time: 2300 ns Iteration: 2 Instance: /div tb
 ** Note: Expected result for quotient= 2 Actual result for quotient= 2
    Time: 2300 ns Iteration: 2 Instance: /div tb
 ** Note: ========= ALL TESTS PASSED ==============
    Time: 2300 ns Iteration: 2 Instance: /div_tb
```

Modelsim waveforms for a few test cases

Divisor = 1
Dividend =0
Quotient = 0

Remainder =0

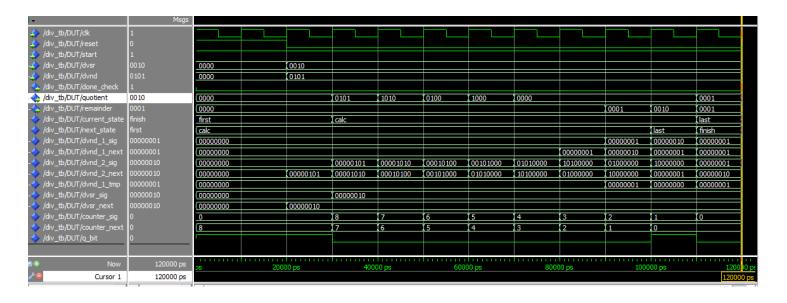
♦	Msgs												
	0												
/div_tb/DUT/reset	0												
/div_tb/DUT/start	1												
	0001	0000	0001										
 → /div_tb/DUT/dvnd	0000	0000											
/div_tb/DUT/done_check	1												
 _ /div_tb/DUT/quotient	0000	(0000											
 _ /div_tb/DUT/remainder	0000	(0000											
/div_tb/DUT/current_state	finish	first		calc								last	finish
/div_tb/DUT/next_state	first	calc									last	finish	first
+- /div_tb/DUT/dvnd_1_sig	00000000	00000000											
/div_tb/DUT/dvnd_1_next	00000000	00000000											
	00000000	00000000											
- - - - - - - - - -	00000000	(00000000)		00000000									
	00000000	00000000											
→ /div_tb/DUT/dvsr_sig →	00000001	(00000000)		00000001									
- → /div_tb/DUT/dvsr_next	00000001	00000000	00000001										
/div_tb/DUT/counter_sig	0	0		8	7	6	5	4	3	2	1	0	
/div_tb/DUT/counter_next	0	(8		7	6	5	4	3	2	1	0		
/div_tb/DUT/q_bit	0												
•													

Divisor = 2 Dividend =1 Quotient = 0

Remainder =1

<u>^</u>	Msgs												
♦ /div_tb/DUT/dk	0												
/div_tb/DUT/reset	0												
/div_tb/DUT/start	1												
≖-	0010	0000		0010									
 	0001	0000		0001									
👍 /div_tb/DUT/done_check	0												
	0000	0000			0001	0010	0100	1000	0000				
≖– <pre> /div_tb/DUT/remainder</pre>	0001	0000											0001
/div_tb/DUT/current_state		first			calc								last
/div_tb/DUT/next_state	finish	calc										last	finish
- → /div_tb/DUT/dvnd_1_sig	00000001	00000000											00000001
≖ - /div_tb/DUT/dvnd_1_next	00000001	00000000										00000001	00000001
📭 🔷 /div_tb/DUT/dvnd_2_sig	00000000	00000000			00000001	00000010	00000100	00001000	00010000	00100000	01000000	10000000	00000000
/div_tb/DUT/dvnd_2_next	00000000	00000000		00000001	00000010	00000100	00001000	00010000	00100000	01000000	10000000	00000000	
- → /div_tb/DUT/dvnd_1_tmp	00000001	00000000											00000001
∓ - ∜ /div_tb/DUT/dvsr_sig	00000010	00000000			00000010								
-	00000010	00000000		00000010									
/div_tb/DUT/counter_sig	0	0			8	7	6	5	4	3	2	1	Ĭ O
/div_tb/DUT/counter_next	0	8			7	6	5	4	3	2	1	0	
/div_tb/DUT/q_bit	0												
Now Now	120000 ps			1		000 ps	600	11111111111 000 ps		00 ps		000 ps	120
Gursor 1	119896 ps		200								100		1198

Divisor = 2 Dividend = 5 Quotient = 2 Remainder = 1



Divisor = 4
Dividend =8
Quotient = 2
Remainder =0

₽	Msgs											
√ /div_tb/DUT/dk	1											
/div_tb/DUT/reset	0											
/div_tb/DUT/start	1											
	0100	0000	0100									
II -	1000	0000	1000									
/div_tb/DUT/done_check	1											
/div_tb/DUT/quotient	0010	0000		1000	0000							0001
IIIIIIIIIIIII	0000	0000							0001	0010	0100	0000
/div_tb/DUT/current_state	finish	first		calc								last
/div_tb/DUT/next_state	first	calc									last	finish
+	00000000	00000000							00000001	00000010	00000100	00000000
/div_tb/DUT/dvnd_1_next	00000000	00000000						00000001	00000010	00000100	00000000	
/div_tb/DUT/dvnd_2_sig	00000010	00000000		00001000	00010000	00100000	01000000	10000000	00000000			00000001
/div_tb/DUT/dvnd_2_next	00000010	00000000	00001000	00010000	00100000	01000000	10000000	00000000			00000001	00000010
<u>→</u> /div_tb/DUT/dvnd_1_tmp	00000000	00000000							00000001	00000010	00000000	
+	00000100	00000000		00000100								
<pre>/div_tb/DUT/dvsr_next</pre>	00000100	00000000	00000100									
/div_tb/DUT/counter_sig	0	0		8	7	6	5	4	3	2	1	0
/div_tb/DUT/counter_next	0	8		7	6	5	4	3	2	1	0	
<pre>/div_tb/DUT/q_bit</pre>	0											

Divisor = 6
Dividend =14
Quotient = 2
Remainder =2

\$ 1+	Msgs											
/div_tb/DUT/dk	1											
/div_tb/DUT/reset	0											
/div_tb/DUT/start	1											
<u>→</u> /div_tb/DUT/dvsr	0110	0000	0110									
	1110	0000	1110									
/div_tb/DUT/done_check	1											
<u>→</u> /div_tb/DUT/quotient	0010	0000		1110	1100	1000	0000					0001
<u>-</u>	0010	0000							0001	0011	0111	0010
/div_tb/DUT/current_state	finish	first		calc								last
/div_tb/DUT/next_state	first	calc									last	finish
+> /div_tb/DUT/dvnd_1_sig	00000010	00000000							00000001	00000011	00000111	00000010
<u>→</u> /div_tb/DUT/dvnd_1_next	00000010	00000000						00000001	00000011	00000111	00000010	00000010
/div_tb/DUT/dvnd_2_sig	00000010	00000000		00001110	00011100	00111000	01110000	11100000	11000000	10000000	00000000	00000001
<u>→</u> /div_tb/DUT/dvnd_2_next	00000010	00000000	00001110	00011100	00111000	01110000	11100000	11000000	10000000	00000000	00000001	00000010
I → /div_tb/DUT/dvnd_1_tmp I → /div_tb/DUT/dvnd_1_tmp	00000010	00000000							00000001	00000011	00000001	00000010
-	00000110	00000000		00000110								
	00000110	00000000	00000110									
/div_tb/DUT/counter_sig	0	0		8	7	6	5	4	3	2	1	(0
/div_tb/DUT/counter_next	0	8		7	6	5	4	3	2	1	Į0	
/div_tb/DUT/q_bit	0											

Divisor = 4
Dividend =15
Quotient = 3
Remainder =3

% +	Msgs												
∳ /div_tb/DUT/dk	0												
/div_tb/DUT/reset	0												
/div_tb/DUT/start	1												
II -	0100	0000	0100										
	1111	0000	1111										
/div_tb/DUT/done_check													
II - 4 /div_tb/DUT/quotient	0011	(0000		1111	1110	1100	1000	0000				0001	0011
II - ♦ /div_tb/DUT/remainder	0011	(0000							0001	0011	0111		0011
/div_tb/DUT/current_s		first		calc								last	finish
/div_tb/DUT/next_state	first	calc									last	finish	first
II - /div_tb/DUT/dvnd_1_sig		(00000000								00000011	00000111		0000001
I → /div_tb/DUT/dvnd_1_n		00000000							00000011			00000011	
II -		00000000			00011110		01111000					00000001	0000001
I → /div_tb/DUT/dvnd_2_n		00000000	00001111	00011110	00111100	01111000	11110000	11100000			00000001	00000011	
		00000000							00000001	00000011			
+- /div_tb/DUT/dvsr_sig	00000100	00000000		00000100									
/div_tb/DUT/dvsr_next	00000100	00000000	00000100										
/div_tb/DUT/counter_sig	0	0		8	7	6	5	4	3	2	1	0	
/div_tb/DUT/counter	0	(8		7	6	5	4	3	2	1	0		
/div_tb/DUT/q_bit	0	'											

Divisor = 7 Dividend =12 Quotient = 1 Remainder =5

% -	Msgs												
∳ /div_tb/DUT/dk	0												
/div_tb/DUT/reset	0												
/div_tb/DUT/start	1												
	0111	0000	0111										
	1100	0000	1100										
/div_tb/DUT/done_check	1												
- _ /div_tb/DUT/quotient	0001	0000		1100	1000	0000							0001
≖ – 4 /div_tb/DUT/remainder	0101	0000							0001	0011	0110	1100	0101
/div_tb/DUT/current_state	finish	first		calc								last	finish
/div_tb/DUT/next_state	first	calc									last	finish	first
	00000101	00000000							00000001	00000011	00000110	00001100	00000101
- - - - - - - - - -	00000101	00000000						00000001	00000011	00000110	00001100	00000101	
 div_tb/DUT/dvnd_2_sig	00000001	00000000		00001100	00011000	00110000	01100000	11000000	10000000	00000000			00000001
 div_tb/DUT/dvnd_2_next	00000001	00000000	00001100	00011000	00110000	01100000	11000000	10000000	00000000			00000001	
 div_tb/DUT/dvnd_1_tmp	00000101	00000000							00000001	00000011	00000110	00000101	
- → /div_tb/DUT/dvsr_sig	00000111	00000000		00000111									
- - - - - - - - - -	00000111	00000000	00000111										
/div_tb/DUT/counter_sig	0	0		8	7	6	5	4	3	2	1	0	
/div_tb/DUT/counter_next	0	8		7	6	5	4	3	2	1	0		
/div_tb/DUT/q_bit	0												

Divisor = 3
Dividend =9
Quotient = 3
Remainder =0

≨ 1 +	Msgs												
	0												
/div_tb/DUT/reset	0												
<pre>/div_tb/DUT/start</pre>	1												
+- /div_tb/DUT/dvsr	0011	0000	0011										
	1001	0000	1001										
/div_tb/DUT/done_check	1												
∓ - / /div_tb/DUT/quotient	0011	0000		1001	0010	0100	1000	0000				0001	0011
 _ /div_tb/DUT/remainder	0000	0000							0001	0010	0100	0011	0000
/div_tb/DUT/current_state	finish	first		calc								last	finish
/div_tb/DUT/next_state	first	calc									last	finish	first
	00000000	00000000							00000001	00000010	00000100	00000011	00000000
/div_tb/DUT/dvnd_1_next	00000000	00000000						00000001	00000010	00000100	00000011	00000000	
/div_tb/DUT/dvnd_2_sig	00000011	00000000		00001001	00010010	00100100	01001000	10010000	00100000	01000000	10000000	00000001	00000011
/div_tb/DUT/dvnd_2_next	00000011	00000000	00001001	00010010	00100100	01001000	10010000	00100000	01000000	10000000	00000001	00000011	
+	00000000	00000000							00000001	00000010	00000001	00000000	
+ /div_tb/DUT/dvsr_sig	00000011	00000000		00000011									
IIIIIIIIIIIII	00000011	00000000	00000011										
/div_tb/DUT/counter_sig	0	0		8	7	6	5	4	3	2	1	0	
/div_tb/DUT/counter_next	0	8		7	6	5	4	3	2	1	0		
<pre>/div_tb/DUT/q_bit</pre>	0												