Datapath

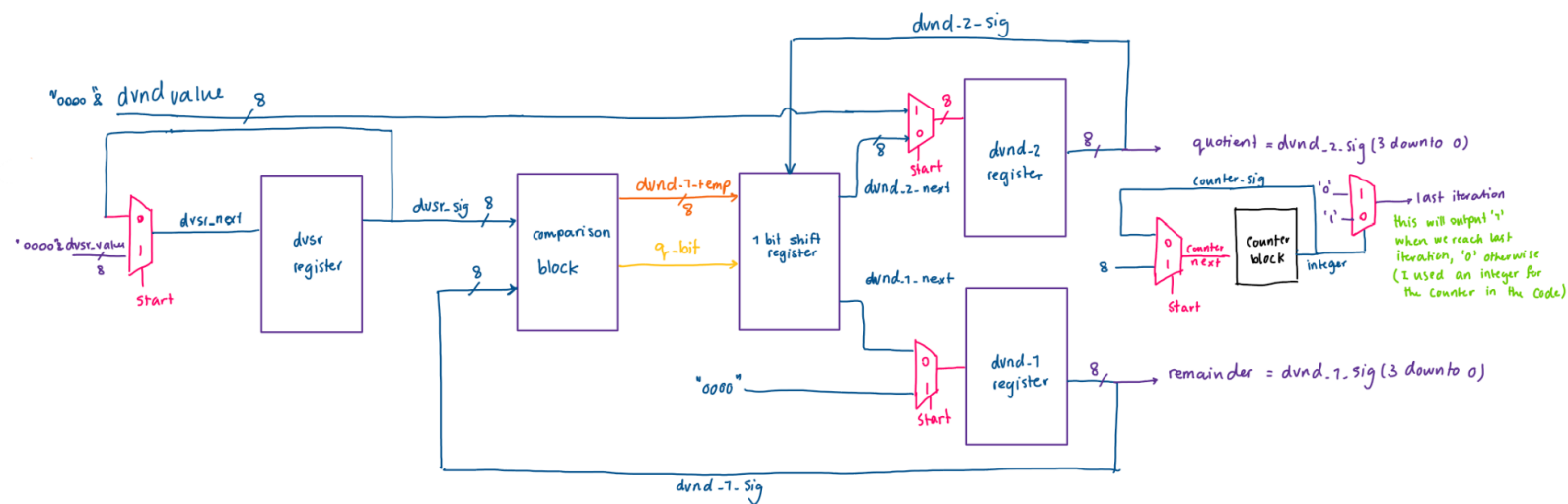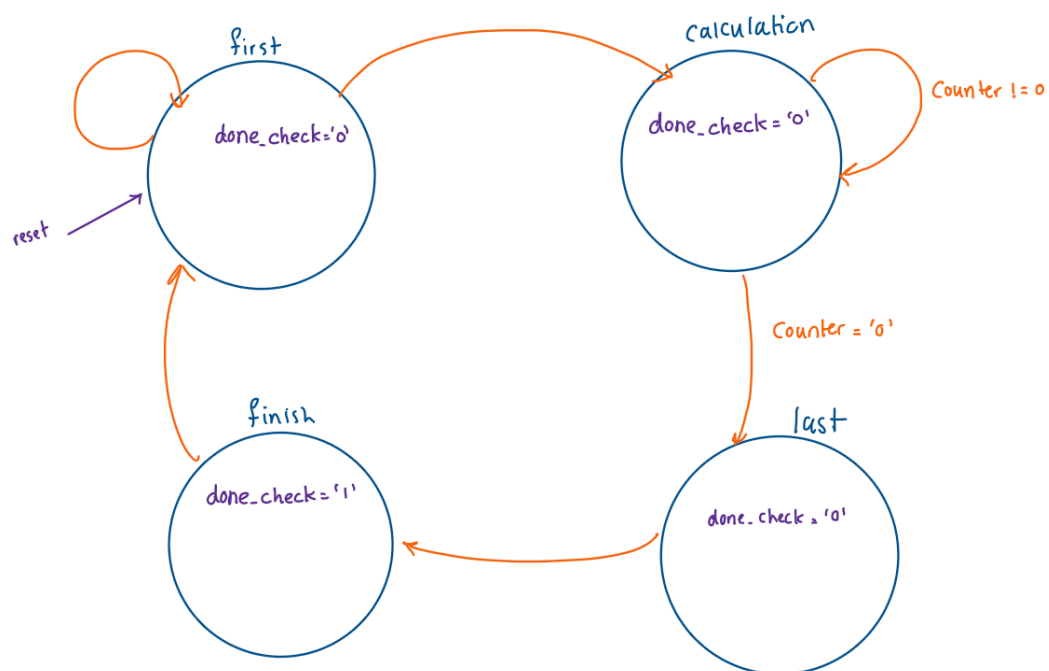**FSM**

Explanation
- For the datapath we have 4 registers where one of them is to store the divisor, 2 of them is to store the dividend and there is one left shift register which shifts the input to left by one bit.
- The inputs are the dividend and divisor and the outputs are the quotient, the remainder and the done_check value. They are all 4 bits long(which store numbers up to 15) and done_check is only 1 bit.
- In the FSM, we initially enter the first state where we input and assign the dividend and the divisor to an 8 bit signal as we add "0000" in front of them. Then we move to the calculation state where we continuously compare the value of the signal storing the dividend and the signal storing the divisor to output 1 or 0 for the quotient and subtract the values and shift the signal to left if required. We also have a counter value to store the number of iterations and we stay in the calculation state until the counter reaches 0 which means that is the last iteration and we enter the last state of the FSM. In this state there is no need to shift the dividend signal since the calculation has ended. Now we enter the finish state which indicates that the division operation is done and it outputs done_check='1' as well as the quotient and the remainder.

Modelsim Output for the test cases

```
Transcript

# ** Note: Expected result for remainder = 3  Actual result for remainder= 3
#    Time: 2080 ns  Iteration: 2  Instance: /div_tb
# ** Note: Expected result for quotient= 0  Actual result for quotient= 0
#    Time: 2080 ns  Iteration: 2  Instance: /div_tb
# ** Note: ------------------------------------------
#    Time: 2080 ns  Iteration: 2  Instance: /div_tb
# ** Note: Test case 19: divisor = 2 dividend = 4
#    Time: 2080 ns  Iteration: 2  Instance: /div_tb
# ** Note: Expected result for remainder = 0  Actual result for remainder= 0
#    Time: 2190 ns  Iteration: 2  Instance: /div_tb
# ** Note: Expected result for quotient= 2  Actual result for quotient= 2
#    Time: 2190 ns  Iteration: 2  Instance: /div_tb
# ** Note: ------------------------------------------
#    Time: 2190 ns  Iteration: 2  Instance: /div_tb
# ** Note: Test case 20: divisor = 2 dividend = 5
#    Time: 2190 ns  Iteration: 2  Instance: /div_tb
# ** Note: Expected result for remainder = 1  Actual result for remainder= 1
#    Time: 2300 ns  Iteration: 2  Instance: /div_tb
# ** Note: Expected result for quotient= 2  Actual result for quotient= 2
#    Time: 2300 ns  Iteration: 2  Instance: /div_tb
# ** Note: ================= ALL TESTS PASSED ============================
#    Time: 2300 ns  Iteration: 2  Instance: /div_tb
```

Modelsim waveforms for a few test cases

Divisor = 1
Dividend =0
Quotient = 0
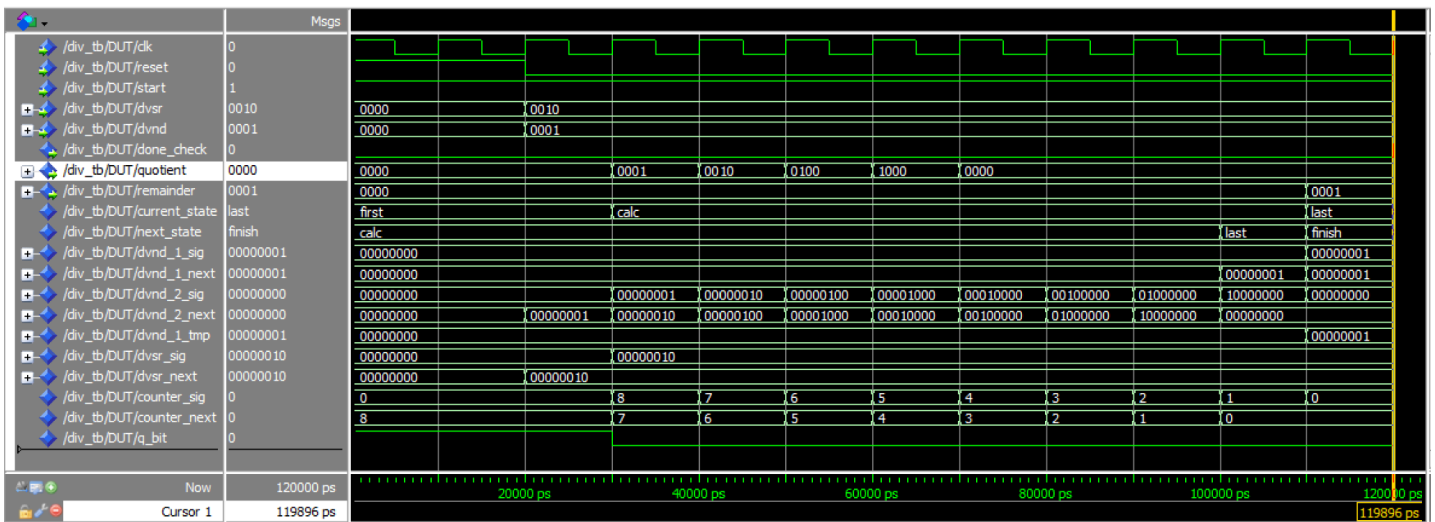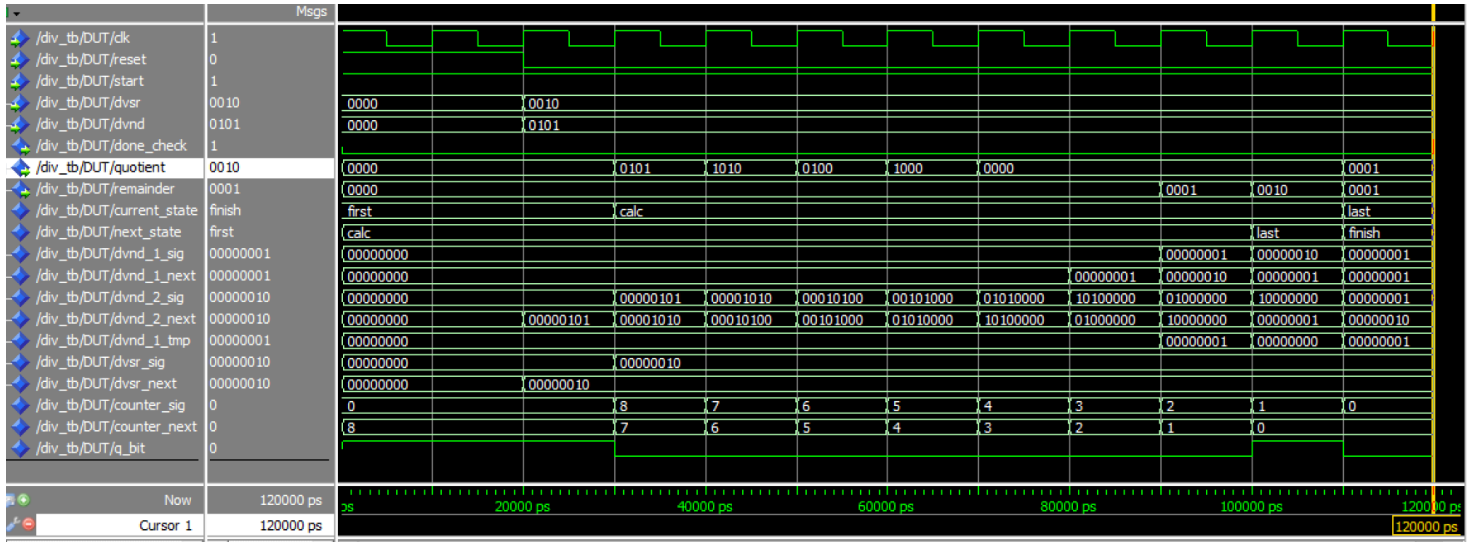**Remainder =0**
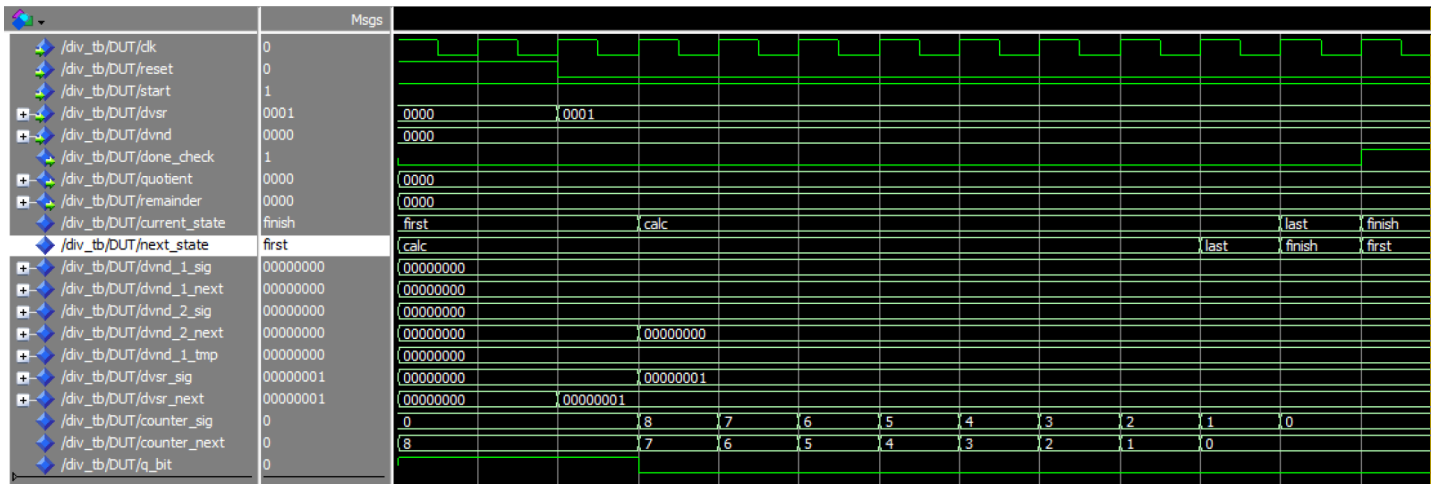
Divisor = 2
Dividend =1
Quotient = 0
Remainder =1

Divisor = 2
Dividend = 5
Quotient = 2
Remainder = 1

Divisor = 4
Dividend = 8
Quotient = 2
Remainder = 0
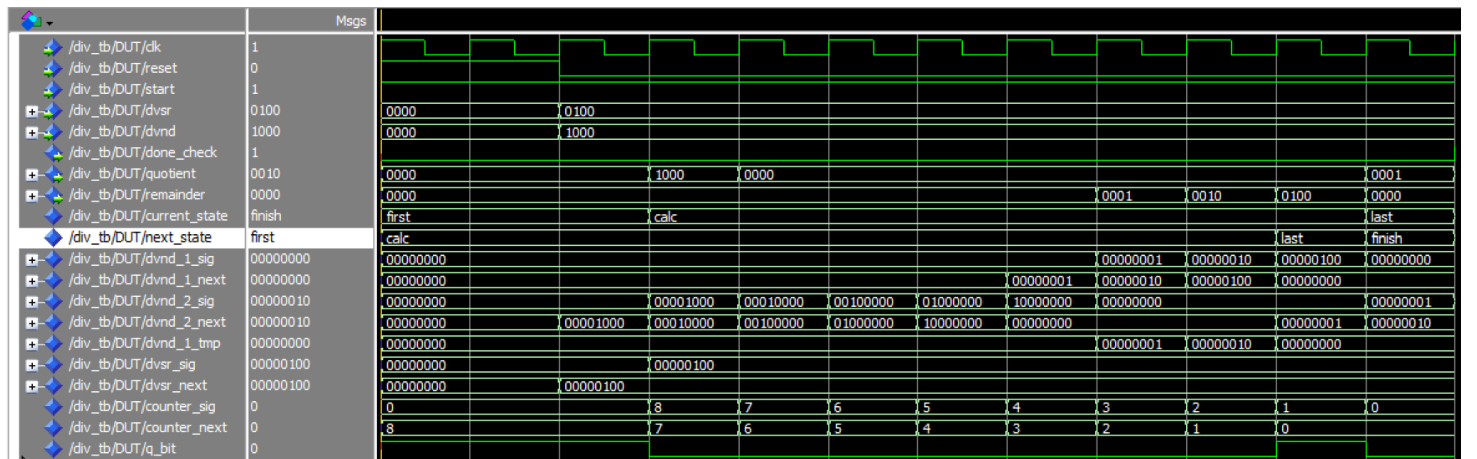
Divisor = 6
Dividend =14
Quotient = 2
Remainder =2

/div_tb/DUT/clk	1
/div_tb/DUT/reset	0
/div_tb/DUT/start	1
/div_tb/DUT/dvsr	0110
/div_tb/DUT/dvnd	1110
/div_tb/DUT/done_check	1
/div_tb/DUT/quotient	0010
/div_tb/DUT/remainder	0010
/div_tb/DUT/current_state	finish
/div_tb/DUT/next_state	first
/div_tb/DUT/dvnd_1_sig	00000010
/div_tb/DUT/dvnd_1_next	00000010
/div_tb/DUT/dvnd_2_sig	00000010
/div_tb/DUT/dvnd_2_next	00000010
/div_tb/DUT/dvnd_1_tmp	00000010
/div_tb/DUT/dvsr_sig	00000110
/div_tb/DUT/dvsr_next	00000110
/div_tb/DUT/counter_sig	0
/div_tb/DUT/counter_next	0
/div_tb/DUT/q_bit	0

Divisor = 4
Dividend =15
Quotient = 3
Remainder =3

/div_tb/DUT/clk	0
/div_tb/DUT/reset	0
/div_tb/DUT/start	1
/div_tb/DUT/dvsr	0100
/div_tb/DUT/dvnd	1111
/div_tb/DUT/done_check	
/div_tb/DUT/quotient	0011
/div_tb/DUT/remainder	0011
/div_tb/DUT/current_s...	finish
/div_tb/DUT/next_state	first
/div_tb/DUT/dvnd_1_sig	00000011
/div_tb/DUT/dvnd_1_n...	00000011
/div_tb/DUT/dvnd_2_sig	00000011
/div_tb/DUT/dvnd_2_n...	00000011
/div_tb/DUT/dvnd_1_tmp	00000011
/div_tb/DUT/dvsr_sig	00000100
/div_tb/DUT/dvsr_next	00000100
/div_tb/DUT/counter_sig	0
/div_tb/DUT/counter_...	0
/div_tb/DUT/q_bit	0

Divisor = 7
Dividend =12
Quotient = 1
Remainder =5
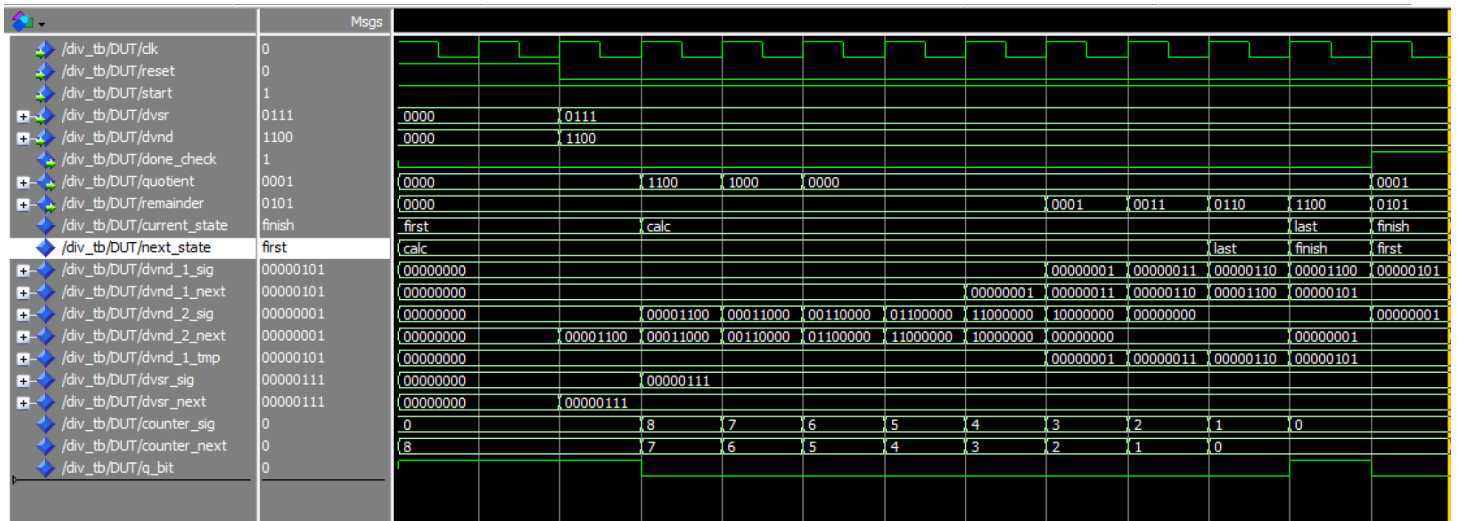
Divisor = 3
Dividend =9
Quotient = 3
Remainder =0