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MOUNT ANNAPURNA CAMPUS
Pokhara-5, Parshyang

DIGITAL LOGIC

BSC.CSIT

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OBJECTIVE:

TO STUDY AND VERIFY THE TRUTH TABLE OF AND, OR, NOT LOGIC GATES.

COMPONENTS:

① AND Gate: 96C76RM SN74AS11AN
② OR Gate: P89189 C04095BCN MM5765BN
③ NOT Gate: EP0118SD 74E04PC

APPARATUS:

Smart digital logic trainer kit, AC Power supply, connecting wires

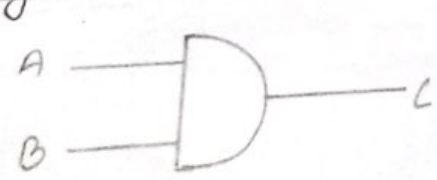
THEORY:

Logic gate is a simple switching circuit that determine wheather and input pulse can passed through to output in digital circuit. Logic gate are the building blocks of digital circuit. Basically gates can be take two or more input and produce one output

Types of Logic Gates:

① AND Gate

② Symbol



(b) Truth table

Inputs		Output
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

(c) Venn-diagram

C = A∩B

(c) Boolean Expression

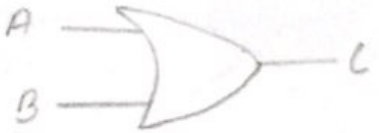
C = A · B

(d) Gist:

Output is 1, when all input are 1

2. OR Gate:

(a) Symbol



(b) Truth table

Inputs		Output
A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

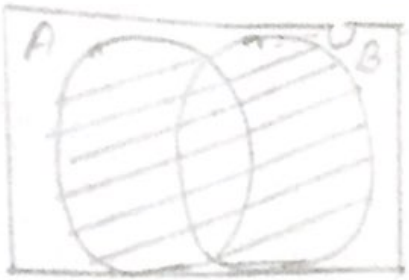
(c) Boolean Expression:

C = A + B

(d) Gist

Output is 1, when at least one input is 1.

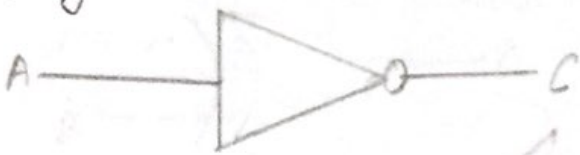
(e) Venn-diagram



C = A∪B

(3) NOT Gate:

(a) Symbol



(b) Truth table

~~Inputs~~ ~~Output~~

~~A~~	~~B~~	~~C~~
~~0~~	~~0~~	
~~0~~	~~1~~	
~~1~~	~~0~~	
1	1	

Input	output
A	$\bar{A}$
0	1
1	0

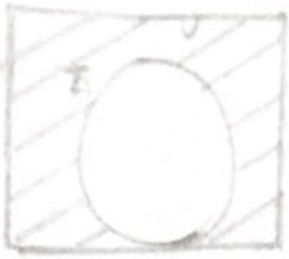
(c) Boolean expression

$C = \bar{A}$

(d) Gist

Output is opposite of input.

(c) venn



$C = \bar{A}$

PROCEDURE:

- Test required all IC's.
- Give various combinations of inputs and check the outputs.
- Repeat the praedure for each IC's.

OBSERVATION TABLE:

For AND and OR Gate

	Inputs			Outputs	
	LED 1	LED 2	LED 3	AND(LED)	OR(LED)
0	Off	Off	Off	Off	Off
1	Off	Off	Green	Off	Green
2	Off	Green	Off	Off	Green
3	Off	Green	Green	Off	Green
4	Green	Off	Off	Off	Green
5	Green	Off	Green	Off	Green
6	Green	Green	Off	Off	Green
7	Green	Green	Green	Green	Green

FOr NOT Gate

S.N	Input	Output
	LED 1	NOT(LED)
1.	Off	ON
2.	Green	OFF

RESULT AND ANALYSIS:

AND GATE:

The Output of an AND Gate is only 1 if all its input are 1. for all other possible inputs and outputs is 0. When all the Ika LED's are green, then the Output LED is green otherwise output LED is off.

OR GATE:

The output of an OR Gate is a 1 if inputs are 1, but output is 0 if all inputs are 0. When one or all inputs LEDs are green, output LED is green Otherwise LED is off.

NOT GATE:

When Logic 1 is applied to NOT Gate, then output becomes zero. When input LED is green, the output LED off vice versa.

CONCLUSION:

Boolean expression was realised for AND, OR, NOT gates.

OBJECTIVE: TO STUDY AND VERIFY THE TRUTH TABLE OF FULL ADDER USING XOR, AND, OR GATE

COMPONENTS:

(a) SN74511N (AND Gate)
(b) 74HCS6AN (X-OR)
(c) CD4075BE (OR)

APPARATUS

(a) Smart Digital logical trainer kit
(b) AC Power supply
(c) Connecting Circuit

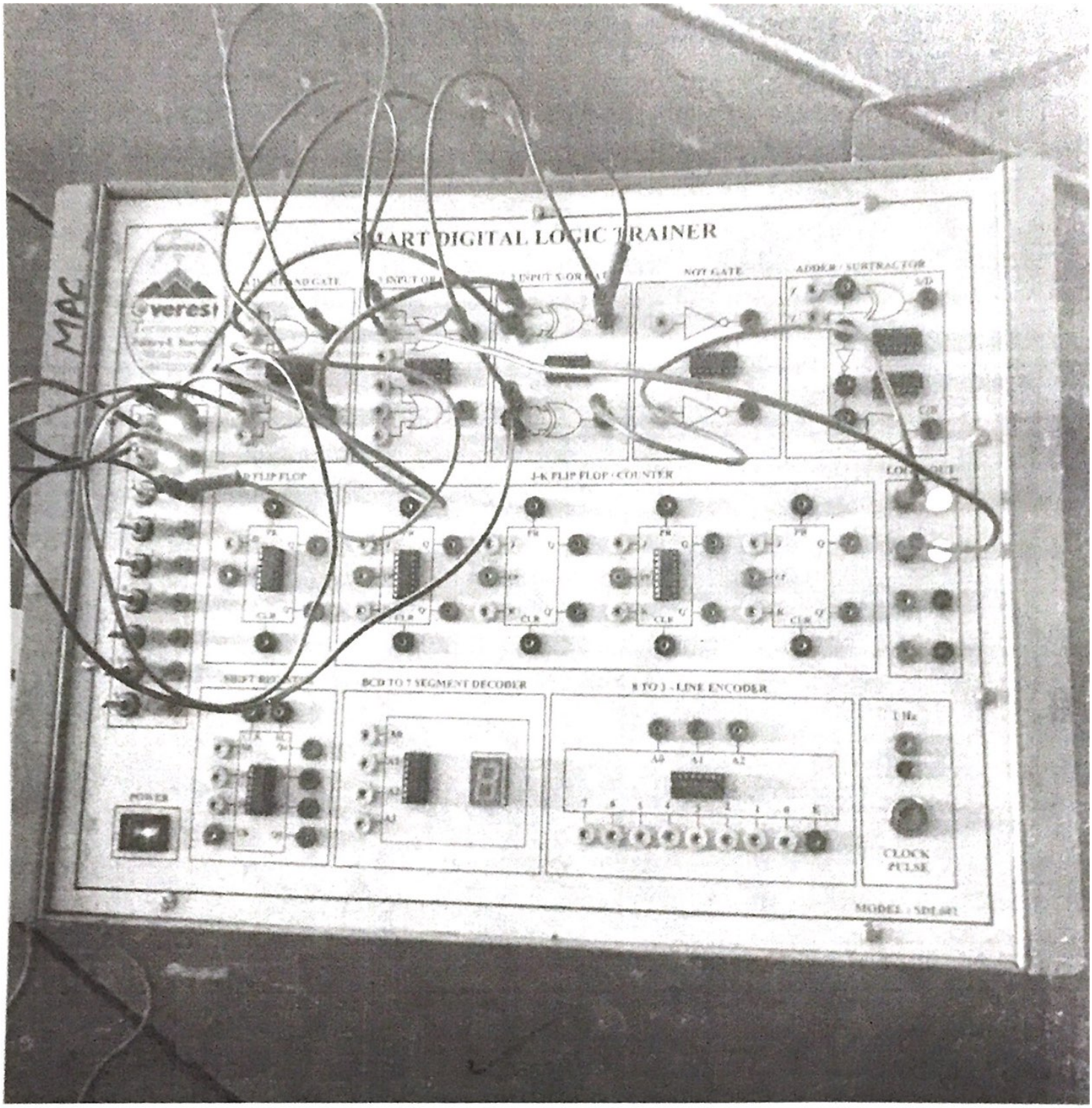
THEORY:

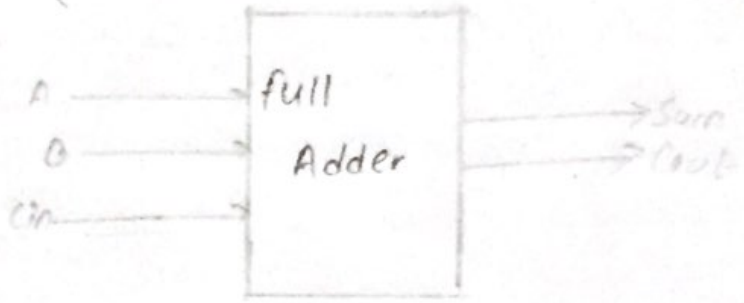
In Half Adder adding of carry is not possible. So, to overcome the limitation faced with Half adder. full adder are implemented.

It is a arithematic combinational logic circuit that performs addition of three single bits. It contains three input (A, B, Cin) and produces two outputs (Sum and Cout).

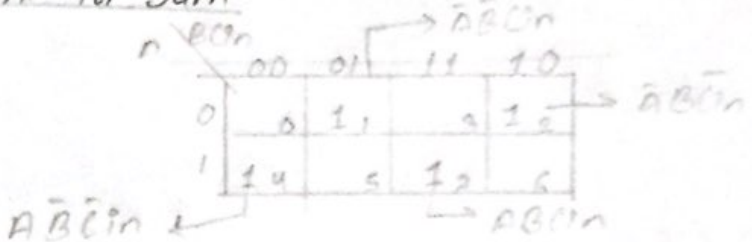
Truth table:

Inputs			Outputs	
A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1


MAC
veresi
SMART DIGITAL LOGIC TRAINER
NOT GATE
ADDER / SUBTRACTOR
J-K FLIP FLOP / COUNTER
BCD TO 7 SEGMENT DECODER
8 TO 3 - LINE ENCODER
POWER
CLOCK PULSE



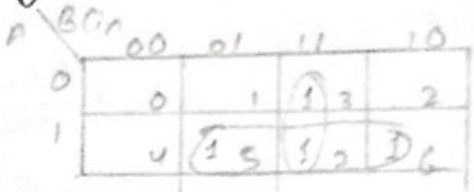
K-MAP For Sum



The equation obtained is

Sum = A XOR B XOR Cin [Check board condition]

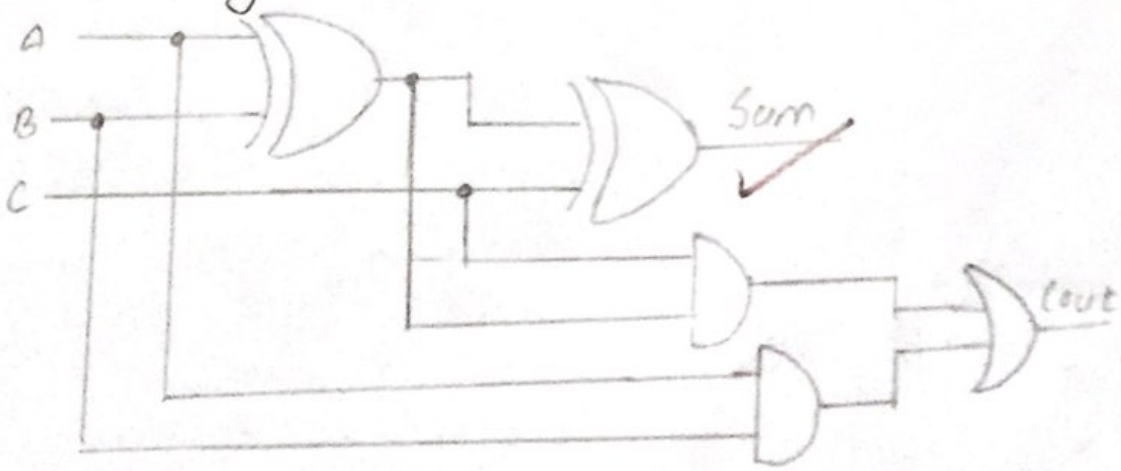
K-Map For Carry (Cout)



The equation obtained is

Cout = AB + BCin + ACin
= AB + (A XOR B) Cin

Circuit Diagrom of Full Adder



OBSERVATION TABLE

SN	J LED	K LED	Q(t+1) LED
1	OFF	OFF	HOLD
2	OFF	GREEN	OFF
3	GREEN	OFF	RED
4	GREEN	GREEN	TOGGLE

RESULT AND ANALYSIS:

→ The output of the JK-flip is changed by bringing a small change in input signal. This change can be brought with the help of clockpulse. So, the output is changed only when the clockpulse is RED(HIGH).

→ When the both the inputs are off the ~~input~~ output is on hold that means no changes appear. When the inputs J is OFF and K is GREEN. the output is OFF. And when the inputs 'J' is GREEN the output is OFF. And the when the inputs 'J' is GREEN and 'K' is OFF the output is RED (ON). And when both the inputs are GREEN the output toggles.

CONCLUSION:

→ The "invalid" state of SR flip-flop is eliminated by the use of JK-flipflop.

OBJECTIVE: DESIGN AND IMPLEMENTATION OF JK FLIP-FLOP

COMPONENTS:

HD74LS76P

APPARATUS:

ⓐ Smart digital trainer kit
ⓑ AC Power supply
ⓒ connecting wires.

THEORY:

The name JK flip-flop is termed from the inventor Jack Kilby from texas instruments. Due to its versatility they are available as IC packages. The major application of JK flipflop are shift register, storage registers, counters and control circuit. Inspite of the simple wiring of D type flipflop, JK flipflop has a toggling nature. This has been an added advantage. Hence they are mostly used in counters and PWM generation, etc. Here we are using NAND gates for demonstrating the JK flip flop.

Whenever the clock signal is low, the input is never going to affect output state. The clock to be high for the inputs to get active. Thus, JK flipflop is a controlled Bi-stable Latch where the clock signal is the control signal. Thus, th

OBJECTIVE: DESIGN AND IMPLEMENTATION OF JK FLIP-FLOP

COMPONENTS:

HD74LS76P

APPARATUS:

(a) Smart digital trainer kit
(b) AC Power supply
(c) connecting wires.

THEORY:

The name JK flip-flop is termed from the invertor Jack Kilby from texas instruments. Due to its versatility they are available as IC packages. The major application of JK flipflop are shift register, storage registers, counters and control circuit. Inspite of the simple wiring of D type flipflop, JK flipflop has a toggling nature. This has been an added advantage. Hence they are mostly used in counters and PWM generation, etc. Here we are using NAND gates for demonstrating the JK Flip flop.

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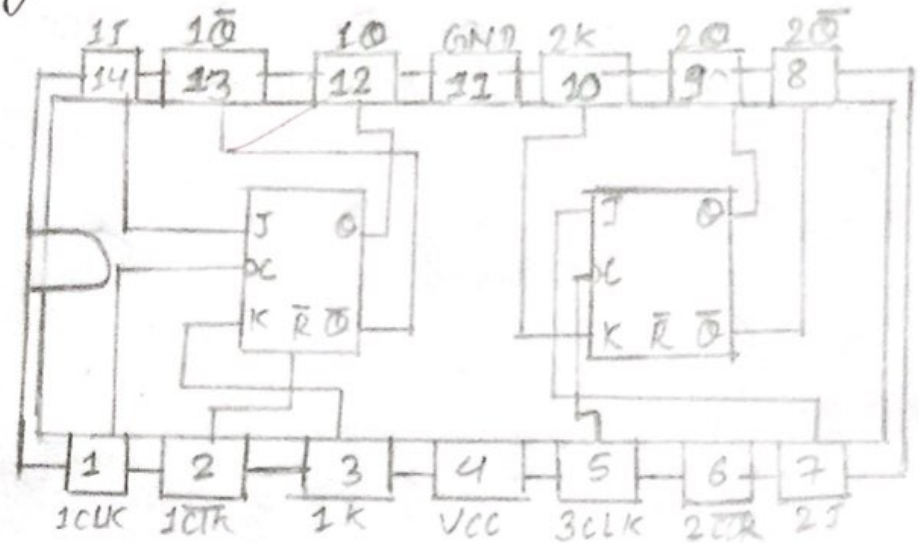
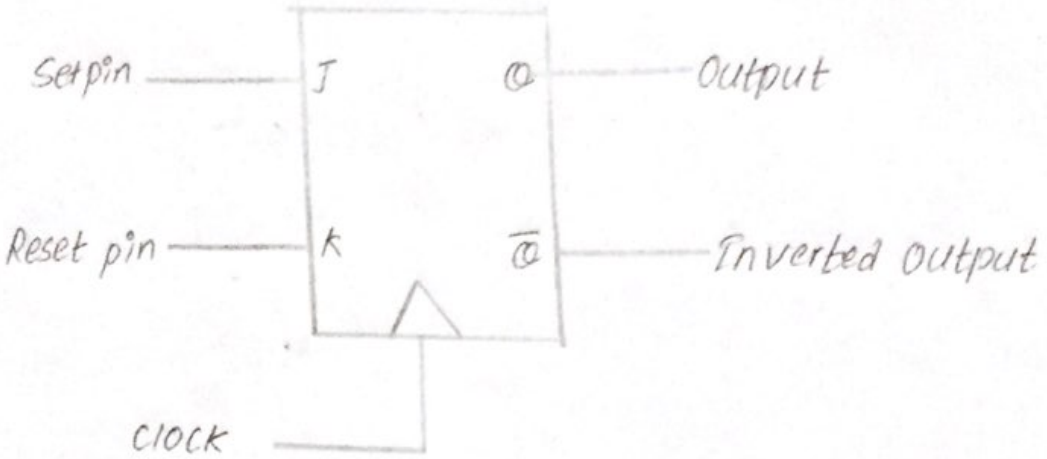
in between the inputs (J, k, Clk and CLR) and ground. These switches helps to shift the inputs between High and Low voltage ground. These switches helps to shift the inputs between High and Low. Voltages. When the switch is off, corresponding input will be High. Similarly, if the switch is ON, corresponding input will be Low. 5V is given from a 5V voltage regulator Output ~~ON, corresponding input will be low. 5V is give~~ is connected to LED's through current limiting registors.



Pinout diagram of 7473

Pinout diagram of 7473 is given below. Each 7473 has two master-slave Jk flipflop. Half portion of IC, above VCC and ground constitutes the first flip-flop and the half portion below VCC and Ground constitutes the second master-slave flip-flop.

Jk output has two stable states based on the inputs which have been discused below.



Symbol: Jk flip-flop

7473 is a commonly used master-slave J-k flipflop IC. These IC's have two independent master slave flipflop with two complementary output.

During the positive transition of clock, data from J and K input is transferred to master and during the negative transistion of clock, data from master get transferred to the slave. If the clock is HIGH, no change will happen to the output (Q and Q bar), even if the value of J and K change. Output will change only during the negative transitions of clock. A logical low of CLR button will reset the outputs (Q and Q bar) and the outputs (Q and Q bar) will not change even if the J, k or CLK is changed. CLR should be set to HIGH after clearing the outputs.

Circuit diagram to put one master-slave flipflop in circuit is given below. Input pins (J, K, CLK and CLR) of the flipflop is connected to 5V through pull up resistors. Push button switches are connected

CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	H	H	H
H	↓	H	L	H	L
H	↓	L	L	Retains previous state	
H	↓	H	H	Toggle	

Truth table of 7473

Truth table of 7473

CLK	J	K	Output
LOW			
HIGH	0	0	Hold
HIGH	0	1	0
HIGH	1	0	1
HIGH	1	1	toggle

CIRCUIT DIAGRAM:

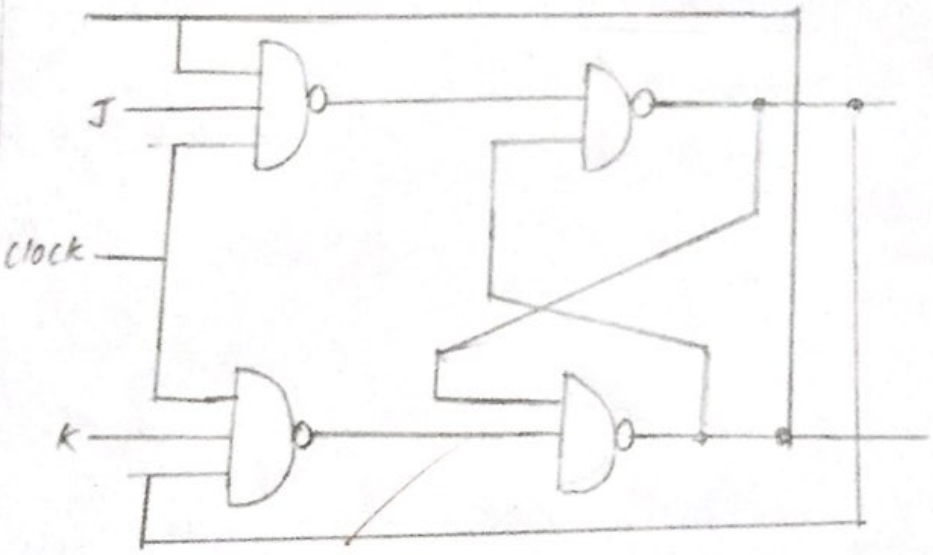
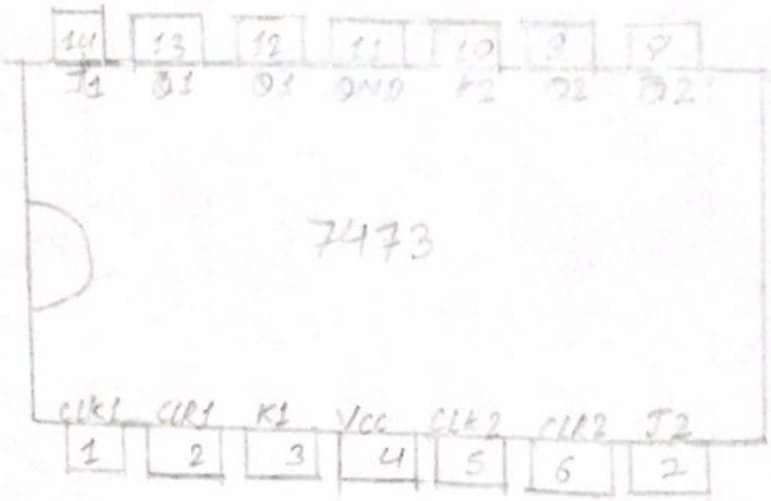


Diagram: Jk-flipflop



~~Truth table of 7473~~

From the truth table, we can conclude that

1. When CLR is LOW, Q will be LOW and Q bar will be high. These outputs will not change, even if the other inputs (J, k and clk) change, until CLR is set to HIGH.
2. When CLR becomes HIGH, If J is LOW and k is HIGH, Q becomes LOW and Q bar becomes HIGH during the next negative transition.
3. When CLR becomes HIGH, if J is HIGH and k is LOW, Q becomes HIGH and Q bar becomes LOW during the next negative transition.
4. When CLR becomes HIGH, if J and k are HIGH, Q and Q bar will toggle in each.
5. When CLR becomes HIGH, if J and k are LOW Q and Q bar will remain in the previous state and is independent of the state of Clk input.

OBSERVATION TABLE

Inputs			Outputs	
LED1	LED2	LED3	Sum (LED)	Carry (LED)
OFF	OFF	OFF	OFF	OFF
OFF	OFF	GREEN	GREEN	OFF
OFF	GREEN	OFF	GREEN	OFF
OFF	GREEN	GREEN	OFF	GREEN
GREEN	GREEN OFF	OFF	GREEN	OFF
GREEN	GREEN	GREEN	OFF	GREEN
GREEN	GREEN	OFF	OFF	GREEN
GREEN	GREEN	GREEN	GREEN	GREEN

RESULT AND ANALYSIS:

The output of the full adder 'sum' and 'Cout' both are '1' when all the inputs are one(1). So, when the inputs A, B, Cin all are Green the output LED of Sum and Carry both are Green. Otherwise, the outputs are different based on the values obtained after the addition of input values. If the sum is 1 with carry '0' then only the ~~lead~~ LED of Sum is 'Green'(on). and if the sum is '0' but carry is '1' then only the LED of carry is GREEN.

CONCLUSION:

Addition of three single bits can be performed by the use of full adder.

Objective: TO DESIGN A CIRCUIT FROM GIVEN BOOLEAN EXPRESSION

COMPONENTS:

1. AND Gate
2. OR Gate
3. NOT Gate

APPARATUS:

(a) Smart digital trainer kit
(b) AC Power supply
(c) connecting wire.

Theory

THEORY:

Canonical form and Standard form

- If each term of boolean expression contains all input variables either in true form or in complement form; it is called canonical form.

eg: $F(A \cdot B \cdot C) = A'BC + ABC + AB'C$ → (Sum of Product) (SOP)

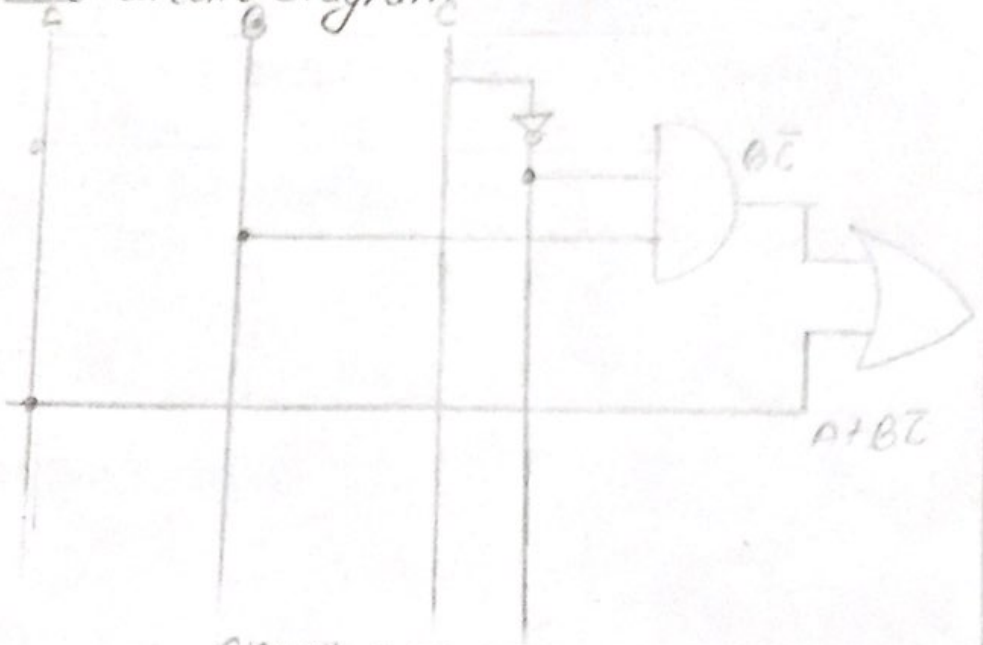
$F(A \cdot B) = AB' + A'B' + AB$ → SOP

$F(A \cdot B \cdot C) = (A'+B+C)(A+B+C)(A+B'+C)$ → POS

$F(A \cdot B) = (A+B')(A'+B')(A+B)$. Product of Sum (POS)

If there exist at least one term that doesnot contain all the variables then it is

(iv) ~~Make~~ circuit diagram



Circuit diagram

OBSERVATION TABLE:

~~LED1~~ ~~A~~ ~~B~~	~~LED2~~ ~~C~~	~~LED3~~ ~~E~~	~~LED4~~ ~~F~~
~~OFF~~	~~OFF~~	~~OFF~~	
~~OFF~~	~~GREEN~~ OFF	GREEN	
~~OFF~~	~~GREEN~~	~~OFF~~	
~~OFF~~	~~GREEN~~	~~GREEN~~	
~~RED~~	~~OFF~~		
~~RED~~	~~OFF~~		
~~RED~~	~~GREEN~~		

said to be standard form.

eg: $F(A \cdot B \cdot C) \Rightarrow A'BC + ABC + AB'C \Rightarrow$ CSSOP

$F(A \cdot B) \Rightarrow A \cdot B' + A \rightarrow$ SSOP

$F(A \cdot B \cdot C) \Rightarrow (A'+B) \cdot (A+B+C)(A+B'C) \Rightarrow$ SPOS

$F(A \cdot B) \Rightarrow (A+B')(A'+B') \cdot (A) \Rightarrow$ SPOS

Question:

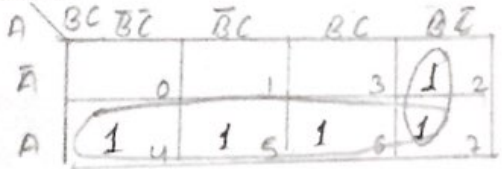
$F = \bar{A}B\bar{C} + A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C} + ABC$

(i) Truth table

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

(ii) Standard Boolean Expression

(ii) K-MAP



(iii) Standard Boolean Expression

$F = A + B\bar{C}$

Inputs			Outputs
LED 1	LED 2	LED 3	LED 4
OFF	OFF	OFF	OFF
OFF	OFF	GREEN	OFF
OFF	GREEN	OFF	GREEN
OFF	GREEN	GREEN	OFF
GREEN	OFF	OFF	GREEN
GREEN	OFF	GREEN	GREEN
GREEN	GREEN	GREEN	GREEN
GREEN	GREEN	GREEN	GREEN

CONCLUSION:

Hence given expression was converted to standard form and realized using trainers kit obtaining some output as truth table.