

# Lecture 3: ARM, Cortex-M, and STM32 Families

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Microprocessors

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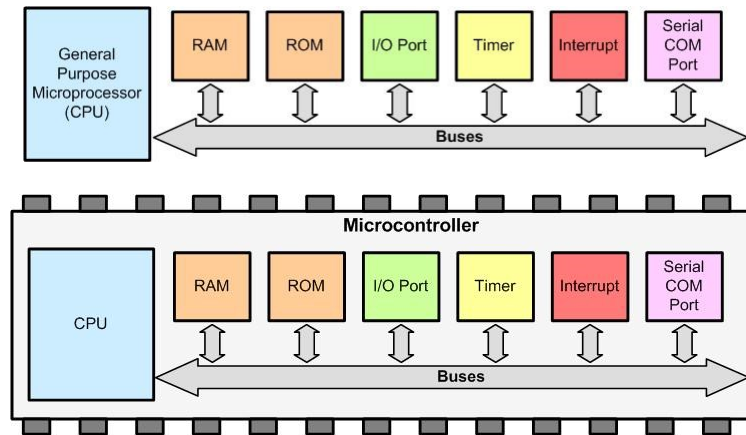
## Outline

- ARM processors
- ARM Cortex-M processor cores
- STM32 microcontrollers
  - Architecture

Microprocessors

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## Microprocessors and Microcontrollers



Microprocessors

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## Available Microcontrollers

### 32-bit

- ARM
- AVR32 (Atmel)
- ColdFire (Freescale)
- MIPS32
- PIC32 (Microchip)
- PowerPC
- TriCore
- (Infineon)
- SuperH

### 16-bit

- MSP430 (TI)
- HCS12 (Freescale)
- PIC24 (Microchip)
- dsPIC (Microchip)

### 8-bit

- 8051
- AVR (Atmel)
- HCS08 (Freescale)
- PIC16
- PIC18

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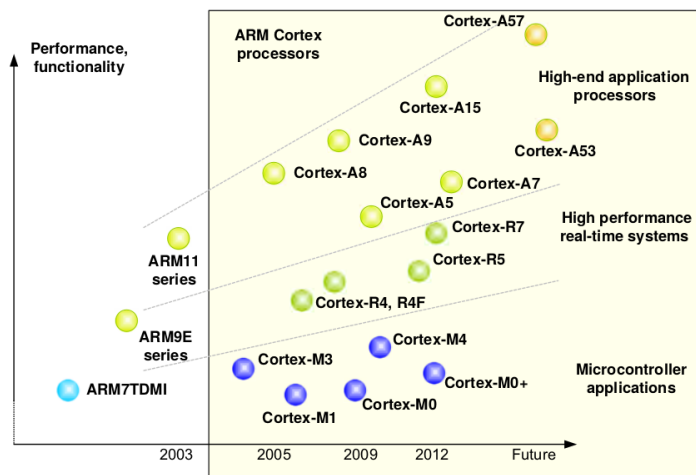
# ARM PROCESSORS

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## ARM Family

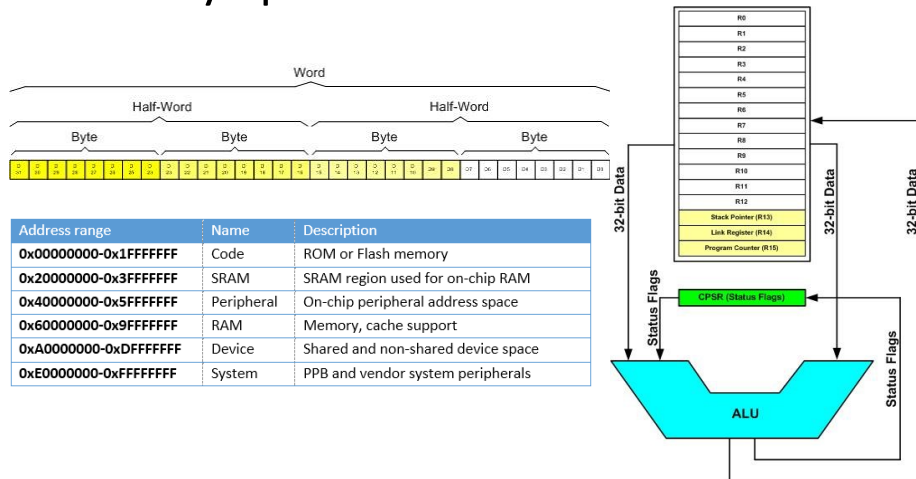
Diversity of processor products for three areas in the Cortex processor family



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# The General Purpose Registers and Memory Space Allocation in the ARM



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## Recap: How to Increase the CPU Performance?

Increase the clock frequency of the chip

- Power dissipation

Increase the number of data buses to bring more information (code and data)

- Von Neumann vs Harvard architectures

Change the internal architecture of the CPU to overlap the execution of more instructions

- Superpipeline vs superscalar

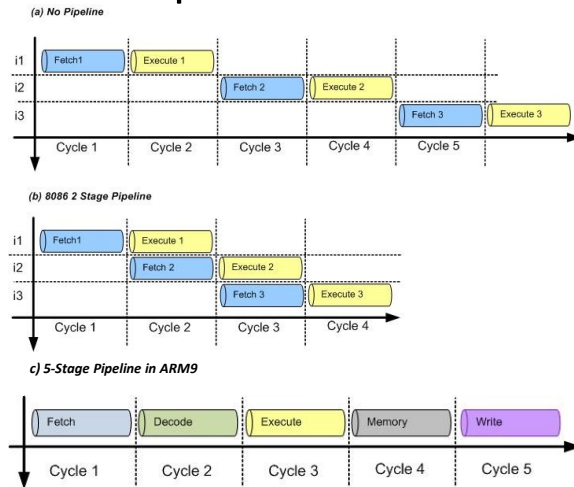
Combining more than one core in a single processor

- Cortex-A up to four cores

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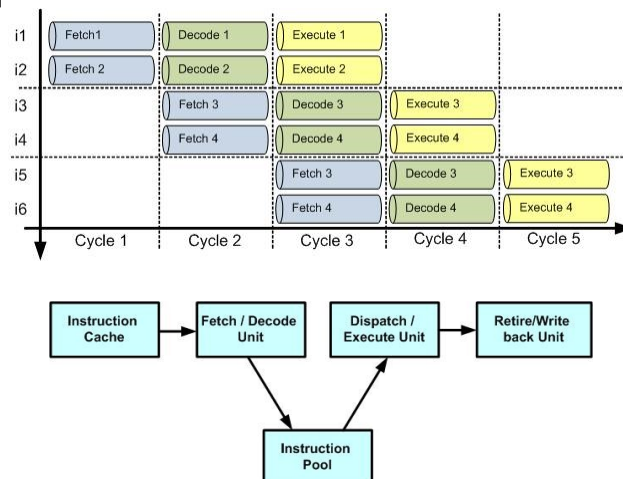
## Recap: Pipelined Architecture



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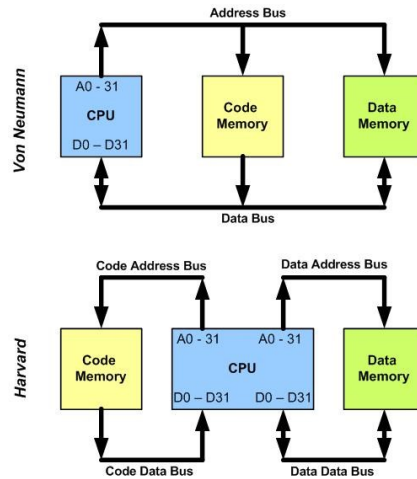
## Recap: Superscalar and Out-of-Order CPUs



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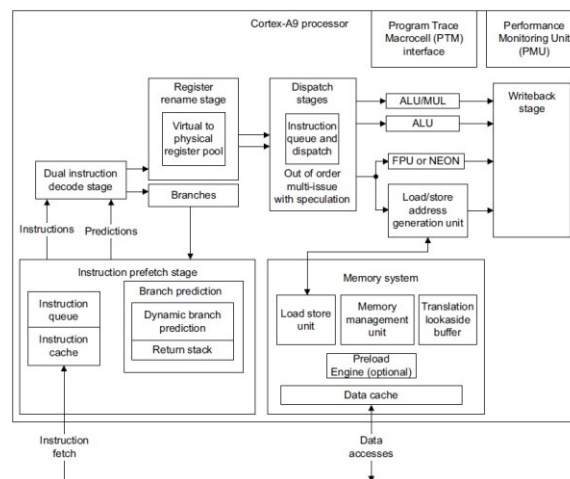
## Recap: Von Neumann vs. Harvard Architecture



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## Top-level diagram of the ARM Cortex-A9 processor

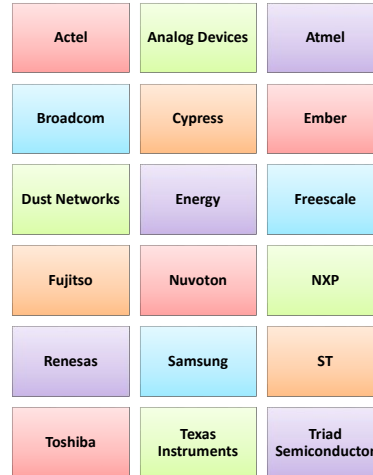


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## One CPU, many peripherals

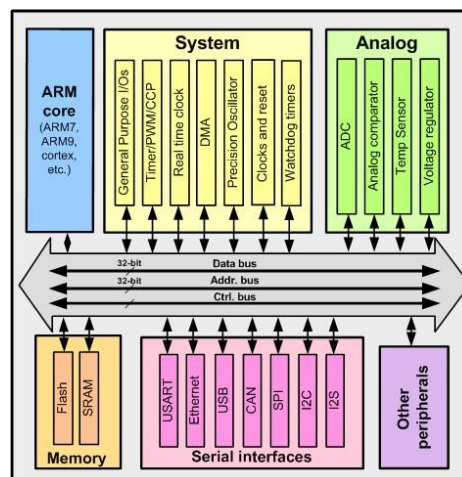
- ARM has defined the architecture, registers, instruction set, memory map, and timing of the ARM CPU and holds the copyright to it.
- Other companies add their own peripherals.
- So, the codes are not compatible



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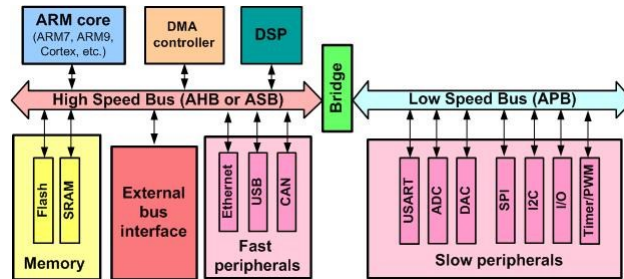
## ARM Simplified Block Diagram



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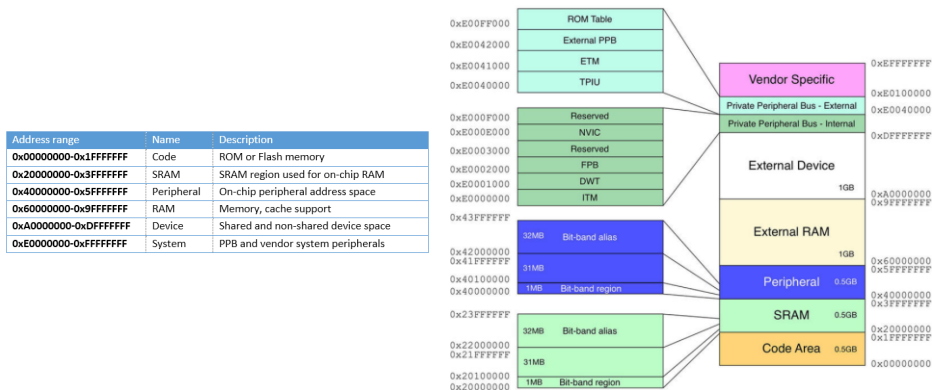
# AHB and APB in ARM



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## Sample Memory Space Allocation in ARM



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# ARM CORTEX-M PROCESSORS

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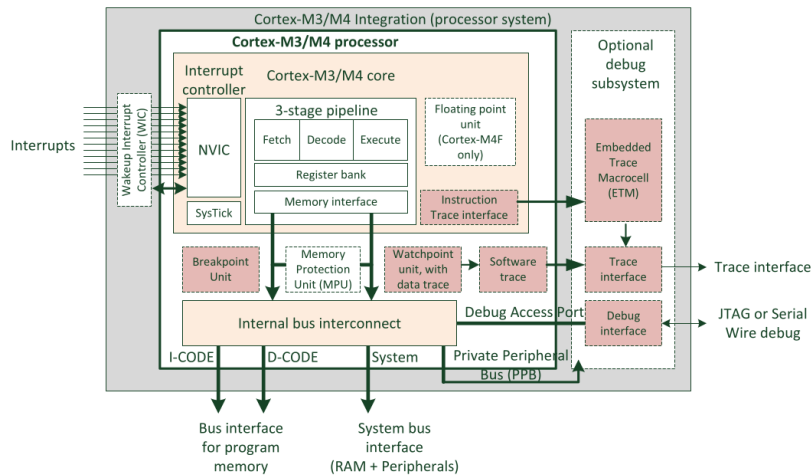
## Cortex-M3 and Cortex-M4 Processors

- Use an **ARMv7-M, 32-bit architecture**
  - Internal registers, data path, and bus interfaces
- Considered as a **RISC** with advanced CISC-like features
- ISA is called **Thumb ISA** and is based on Thumb-2 Technology
- **Three-stage pipeline** design
- **Harvard bus architecture** with unified memory space
- On-chip bus interfaces based on ARM **AMBA**
- An **interrupt controller** called NVIC
- Support for various features for **OS**
- Sleep mode support and various **low power** features
- Optional MPU (**Memory Protection Unit**)
- Bit-data accesses in specific memory regions using **Bit Band**
- Used in single processor or **multi-processor** designs

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# Block Diagram of Cortex-M3/4

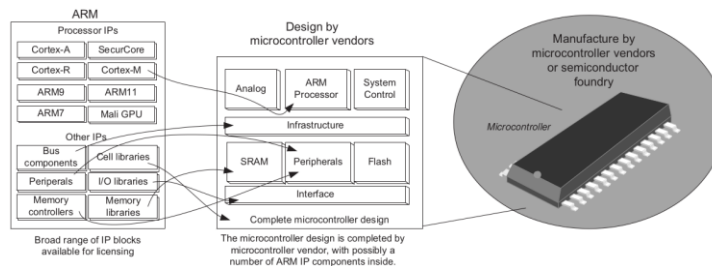


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## ARM and the Microcontroller Vendors

- Many silicon vendors provide ARM Cortex-M3 or Cortex-M4 microcontrollers
- ARM provides
  - The processor source in Verilog
  - Intellectual Property (IP) products
    - ARM Physical IP
    - Peripherals and AMBA infrastructure components
    - Debug components for linking debug systems
  - Cortex-M System Design Kit (CMSDK) for chip designers
  - Software development platforms
    - Keil Microcontroller Development Kit (MDK-ARM)
    - ARM Development Studio 5 (DS-5)



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## How to Choose a Microcontroller?

- Peripherals and interface features
- Memory size requirements of the application
- Low power requirements
- Performance and maximum frequency
- Chip package
- Operation conditions (voltage, temperature, electromagnetic interference)
- Cost and availability
- Software development tool support and development kits
- Future upgradability
- Firmware packages and firmware security
- Availability of application notes, design examples, and support

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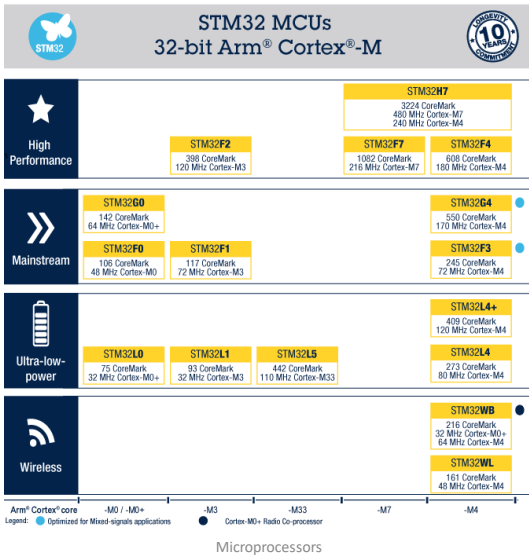
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## STM32 MICROCONTROLLERS

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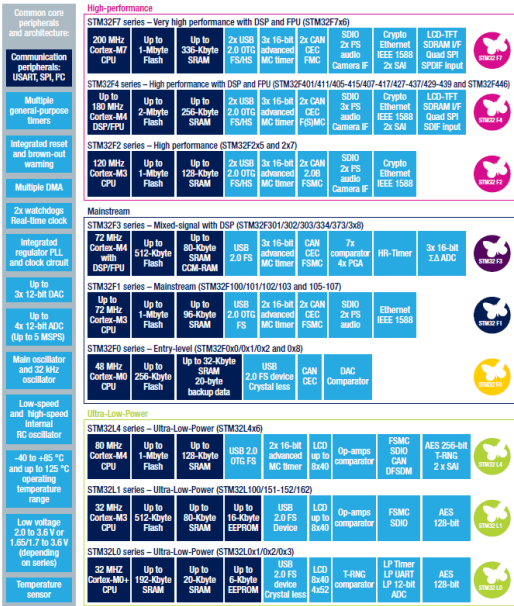
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# STM32 ARM Cortex Portfolio



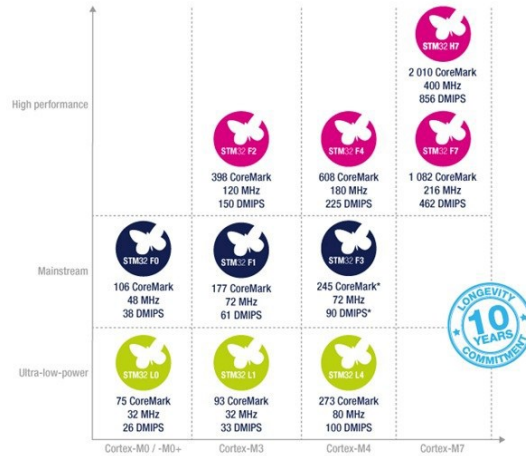
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## STM32 ARM Cortex Portfolio



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# STM32 ARM Cortex Portfolio



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## STM32 Variations

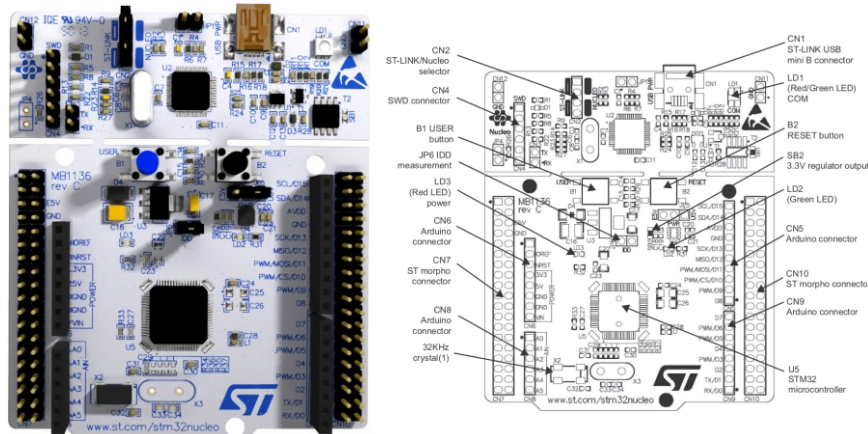
STM32 Family	Cortex-M	Thumb	Thumb-2	Multiply in Hardware	Divide in Hardware	Saturated math	DSP	FPU	ARM Architecture
F0	M0	Most	Some	32-bit result	No	No	No	No	ARMv6-M
L0	M0+	Most	Some	32-bit result	No	No	No	No	ARMv6-M
F1, F2, L1	M3	Entire	Entire	32/64-bit result	Yes	Yes	No	No	ARMv7-M
F3, F4, L4	M4	Entire	Entire	32/64-bit result	Yes	Yes	Yes	Yes SP	ARMv7E-M
F7	M7	Entire	Entire	32/64-bit result	Yes	Yes	Yes	Yes SP & DP	ARMv7E-M

STM32 Family	Cortex-M	SysTick Timer	Bit-Banding	Memory Protection Unit (MPU)	CPU Cache	OS Support	Memory Architecture
F0	M0	Yes	Yes	No	No	Yes	Von Neumann
L0	M0+	Yes	Yes	Yes	No	Yes	Von Neumann
F1, F2, L1	M3	Yes	Yes	Yes	No	Yes	Harvard
F3, F4, L4	M4	Yes	Yes	Yes	No	Yes	Harvard
F7	M7	Yes	No	Yes	Yes	Yes	Harvard

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# STM32 Nucleo-64 Board



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## Note: Types of Technical Material

- Tutorials and getting started guides
- User guides
- Reference manuals
- **Datasheets**
- White papers
- Application notes
- Flyers and brochures
- Presentations and webinars
- Reference designs
- ...

Learn how to  
find & use  
them!

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## STM32F401xE Datasheet

1. Introduction
2. Description
3. Functional overview
4. Pinouts and pin description
5. Memory mapping
6. Electrical characteristics
7. Package characteristics
8. Part numbering
9. Revision history



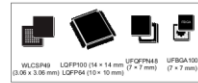
## STM32F401xD STM32F401xE

ARM® Cortex®-M4 32b MCU+FPU, 105 DMIPS,  
512KB Flash/96KB RAM, 11 TIMs, 1 ADC, 11 comm. interfaces

Datasheet - production data

### Features

- Core: ARM® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution from Flash memory, frequency up to 84 MHz, memory protection unit, 105 DMIPS/1.25 DMIPS/MHz (Dhystone 2.1), and DSP instructions
- Memories
  - up to 512 Kbytes of Flash memory
  - up to 96 Kbytes of SRAM
- Clock, reset and supply management
  - 1.7 V to 3.6 V application supply and I/Os
  - POR, PDR, PVD and BOR
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Power consumption
  - Run: 146 µA/MHz (peripheral off)
  - Stop (Flash in Sleep mode, fast wakeup time): 42 µA Typ @ 25°C; 65 µA max @ 25 °C
  - Stop (Flash in Deep power down mode, fast wakeup time): down to 10 µA @ 25 °C; 30 µA max @ 25 °C
  - Standby: 2.4 µA @ 25 °C / 1.7 V without RTC; 12 µA @ 85 °C @ 1.7 V
  - V<sub>BAT</sub> supply for RTC: 1 µA @ 25 °C
  - 11x12-bit, 2.4 MSPS A/D converter: up to 16 channels
- General-purpose DMA: 16-stream DMA controllers with FIFOs and burst support
- Up to 11 timers: up to six 16-bit, two 32-bit timers up to 84 MHz, each with up to four I/OCPWM or pulse controller and quadrature (incremental) encoder input, two watchdog timers (independent and window) and a SysTick timer



- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
  - Cortex®-M Embedded Trace Macrocell™
- Up to 81 I/O ports with interrupt capability
  - Up to 78 fast I/Os up to 42 MHz
  - All I/O ports are 5V-tolerant
- Up to 12 communication interfaces
  - Up to 3 x FC interfaces (SMBus/PMBus)
  - Up to 3 USARTs (2 x 10.5 Mbit/s, 1 x 5.25 Mbit/s), ISO 7816 interface, LIN, I2C, modem control
  - Up to 4 SPIs (up to 42 Mbit/s at f<sub>CLK</sub> = 84 MHz), SPI2 and SPI3 with muxed full-duplex I<sup>2</sup>S to achieve audio class accuracy via internal audio PLL or external clock
  - SDIO interface
  - Advanced connectivity: USB 2.0 full-speed device/host/OTG controller with on-chip PHY
- CRC calculation unit
- 96-bit unique ID
- RTC: subsecond accuracy, hardware calendar
- All packages (WLCSP49, LQFP64/100, UFPQ49, UFBGA100) are ECOPACK™2

Table 1. Device summary

Reference	Part number
STM32F401xD	STM32F401CD
STM32F401xE	STM32F401RD, STM32F401VD
STM32F401xE	STM32F401CE
STM32F401xE	STM32F401RE, STM32F401VE

January 2015

DocID025644 Rev 3

1/135

This is information on a product in full production.

www.st.com

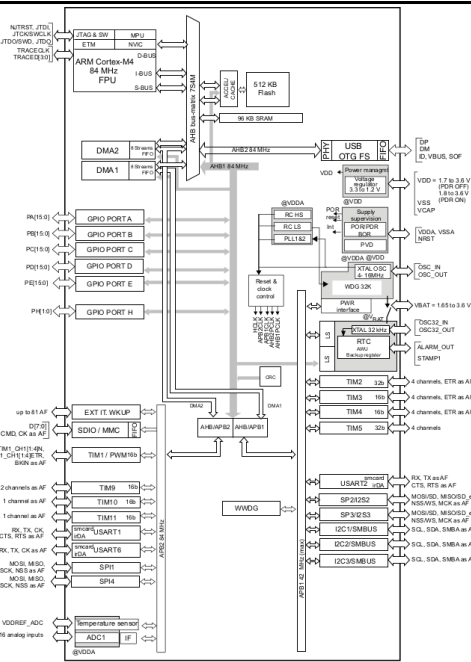
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## STM32F401RE Arm Microcontroller Block Diagram

STM32F4xx LQFP 64 pinout used in Nucleo-F401RE board

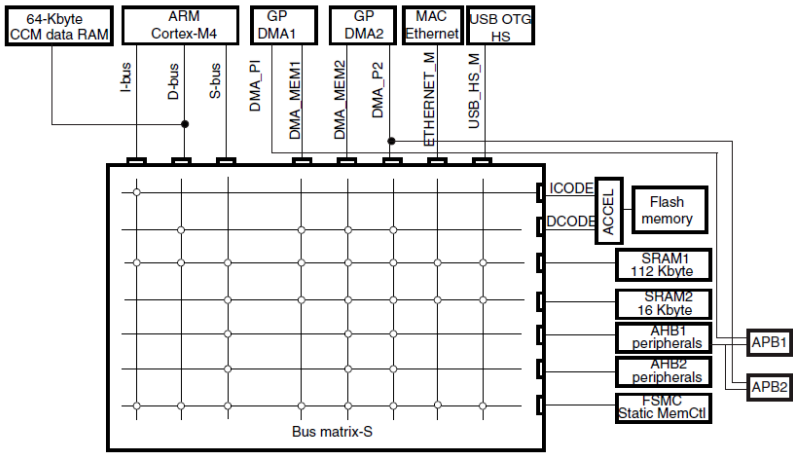
Peripherals	STM32F401d	STM32F401e
Flash memory in Kbytes	384	512
SRAM in Kbytes	System	96
Timers	General-purpose	7
Advanced-control	1	
SPI F/S	3/2 (full duplex)	4/2 (full duplex)
Communication interfaces	FC	3
USART	SDIO	1
USB OTG F/S		1
GPIOs	36	50
12-bit ADC		1
Number of channels	10	16
Maximum CPU frequency		84 MHz
Operating voltage		1.7 to 3.6 V
Operating temperatures		Ambient temperature: -40 to +85 °C; -40 to +105 °C
		Junction temperature: -40 to +125 °C
Package	WLCSP49 LQFP64 UFBGA100 UFPQ49	WLCSP49 LQFP64 UFBGA100 LQFP100



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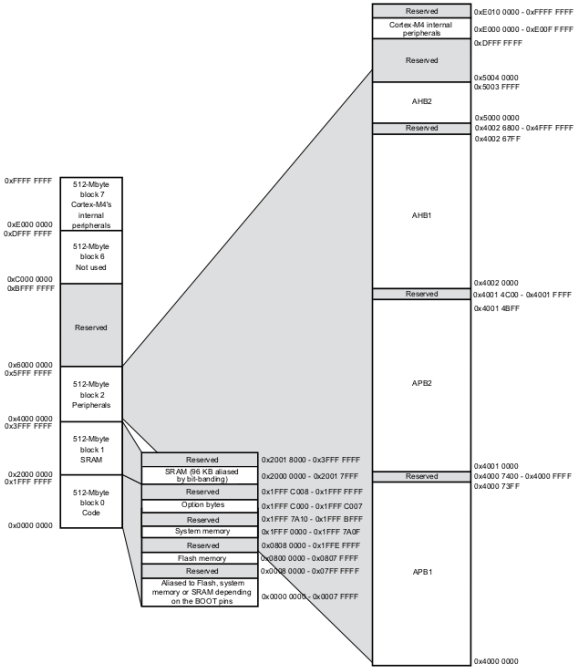
# STM ARM Bus Matrix



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## Memory Map



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# STM32F401

## Register Boundary Addresses I

Bus	Boundary address	Peripheral
Cortex <sup>®</sup> -M4	0xE010 0000 - 0xFFFF FFFF	Reserved
	0xE000 0000 - 0xE00F FFFF	Cortex-M4 internal peripherals
AHB2	0x5004 0000 - 0xDFFF FFFF	Reserved
	0x5000 0000 - 0x5003 FFFF	USB OTG FS
AHB1	0x4002 6800 - 0x4FFF FFFF	Reserved
	0x4002 6400 - 0x4002 67FF	DMA2
	0x4002 6000 - 0x4002 63FF	DMA1
	0x4002 5000 - 0x4002 4FFF	Reserved
	0x4002 3C00 - 0x4002 3FFF	Flash interface register
	0x4002 3800 - 0x4002 3BFF	RCC
	0x4002 3400 - 0x4002 37FF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2000 - 0x4002 2FFF	Reserved
	0x4002 1C00 - 0x4002 1FFF	GPIOH
	0x4002 1400 - 0x4002 1BFF	Reserved
	0x4002 1000 - 0x4002 13FF	GPIOE
	0x4002 0C00 - 0x4002 0FFF	GPIOD
	0x4002 0800 - 0x4002 0BFF	GPIOC
	0x4002 0400 - 0x4002 07FF	GPIOB
	0x4002 0000 - 0x4002 03FF	GPIOA

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# STM32F401

## Register Boundary Addresses II

Bus	Boundary address	Peripheral
APB2	0x4001 4C00- 0x4001 FFFF	Reserved
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	SPI4/I2S4
	0x4001 3000 - 0x4001 33FF	SPI1
	0x4001 2C00 - 0x4001 2FFF	SDIO
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1
	0x4001 1800 - 0x4001 1FFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1
	0x4000 7400 - 0x4000 FFFF	Reserved

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# STM32F401

## Register Boundary Addresses III

Bus	Boundary address	Peripheral
APB1	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6000 - 0x4000 6FFF	Reserved
	0x4000 5C00 - 0x4000 5FFF	I2C3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 4800 - 0x4000 53FF	Reserved
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	I2S2ext
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers
	0x4000 1000 - 0x4000 27FF	Reserved
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
	0x4000 0400 - 0x4000 07FF	TIM3
	0x4000 0000 - 0x4000 03FF	TIM2

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### Part Numbering

Example: STM32 F 401 C E Y 6 TR

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Device subfamily

401 = 401 family

Pin count

C = 48/49 pins  
R = 64 pins  
V = 100 pins

Flash memory size

D = 384 Kbytes of Flash memory  
E = 512 Kbytes of Flash memory

Package

H = UFBGA  
T = LQFP  
U = UQFPN  
Y = WLCSP

Temperature range

6 = Industrial temperature range, -40 to 85 °C

Packing

TR = tape and reel  
No character = tray or tube

### Sample & Buy

Part Number	Order from Distributors	Order from ST	Marketing Status	ECCN (US)	ECCN (EU)	Packing Type	Package	Temperature (°C)	Budgetary Price (US\$/1000)	More Info
STM32F401RET7	Available at 1 distributors	Buy now	ACTIVE	3A991A2	NEC	Tray	LQFP 64 10x10x1.4	-40 105	2.938 / 10k	MORE INFO
STM32F401RET6TR	Available at 1 distributors	Buy now	ACTIVE	3A991A2	NEC	Tape And Reel	LQFP 64 10x10x1.4	-	2.7458 / 10k	MORE INFO
STM32F401RET6	Available at 7 distributors	Buy now	ACTIVE	3A991A2	NEC	Tray	LQFP 64 10x10x1.4	-40 85	2.7458 / 10k	MORE INFO

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