Ahsanullah University of Science & Technology

Department of Computer Science & Engineering

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Introduction:

In this experiment we have made a 4 bit Arithmetic Logic Unit (ALU) with the help of a 4 bit full Adder and othe basic gates. Here S_0, S_1 and S_1 bits are used as Selectors. According to the given table $S_1 = 1$ is specified for arithmetic operations and $S_1 = 0$ is for logical operations and thus depending on the value of S_1, ALU will perform an arithmetic or a logical operation. From the given function table we derived the equation of three inputs and implemented the circuit.

Problem statement:

S_2	S_1	S_0	Output	Function
1	1	1	A_i+1	Increment A
0	1	1	A_i+B_i+1	Add with carry
1	1	0	A_i+B_i	Add
0	1	0	A_i+1+1	Transfer A with Carry
1	0	X	$A_i . B_i$	AND
0	0	X	A_i'	Complement A

Function Generation:

S_2	S_1	S_0	Z	X	Y	Function
1	1	1	1	A_i	0	A_i+1
0	1	1	1	A_i	B_i	A_i+B_i+1
1	1	0	0	A_i	B_i	A_i+B_i
0	1	0	1	A_i	all 1	A_i+1+1
1	0	X	X	A_iB_i	0	$A_i . B_i$
0	0	X	X	A_i'	0	A_i'

Kmap:

For X:

	$S_0'A_i'B_i'$	$S_0'A_i'B_i$	$S_0'A_iB_i$	$S_0'A_iB_i'$	$S_0A_iB_i'$	$S_0A_iB_i$	$S_0A_i'B_i$	$S_0A_i'B_i'$
$S_2'S_1'$	1	1					1	1
$S_2'S_1$			1	1	1	1		
S_2S_1			1	1	1	1		
S_2S_1'			1			1		

For Y:

	$S_0'B_i'$	$S_0'B_i$	S_0B_i	S_0B_i'
$S_2'S_1'$				
$S_2'S_1$	1	1	1	
S_2S_1		1		
S_2S_1'				

For Z:

	$\bar{S}_1\bar{S}_0$	$\bar{S}_1S_0$	S_1S_0	$S_1\bar{S}_0$
$\bar{S}_2$	X	X	1	1
S_2	X	X	1	

From the given table we can determine 3 equations of X, Y and Z Respectively

$$\therefore X = S_1 A_i + S_2 A_i B_i S_1' + S_2' S_1' A_i'$$

$$\therefore Y = S_1 B_i + S_2' S_1 S_0'$$

$$\therefore Z = S_2 S_1 S_0 + S_2' S_1 S_0 + S_2' S_1 S_0'$$

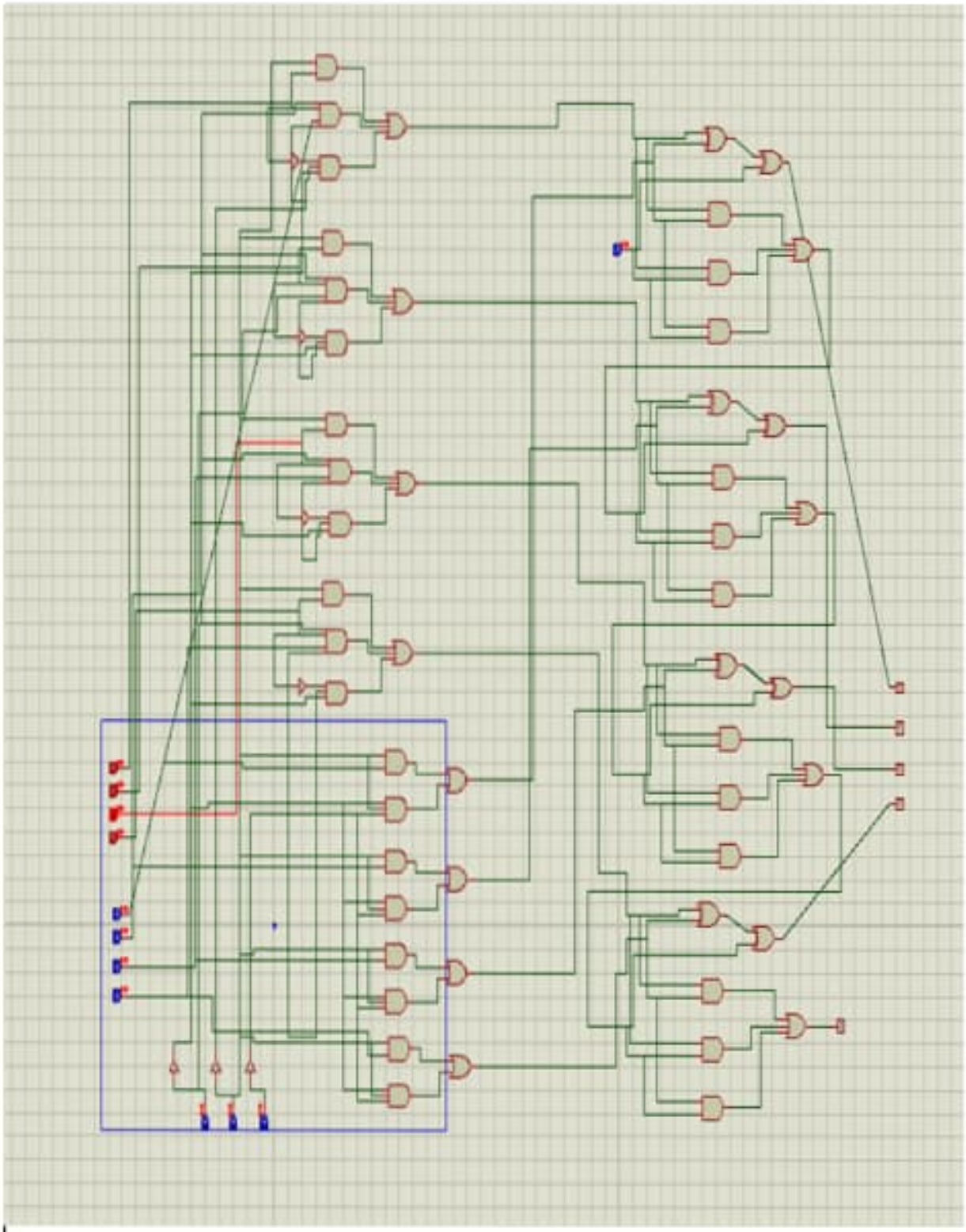
$$= S_1 S_0 (S_2 + S_2') + S_2' S_1 S_0'$$

$$= S_1 S_0 + S_2' S_1 S_0'$$

Equipment and Budget:

Gate Name	IC	Quantity	Price per IC (tk)	Price (tk)
NOT	7404	2	25	50
AND	7408	5	23	115
OR	7432	1	27	27
XOR	7486	2	23	46
3 Input AND	7411	3	25	75
3 Input OR	4075	3	23	69
4 Input AND	7421	2	26	52
		Total Cost = 434 tk		

Simulation:



Result :

Input											Output				
S_2	S_1	S_0	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	Function	Cout	F_3	F_2	F_1	F_0
1	1	1	1	0	0	0	0	0	1	0	Increcement A	0	1	0	0	1
0	1	1	1	0	0	0	0	0	1	0	Add with carrry	0	1	0	1	1
1	1	0	1	0	0	0	0	0	1	0	Add	0	1	0	1	0
0	1	0	1	0	0	0	1	1	1	1	Transfer A with carrry	1	1	0	0	0
1	0	X	1	0	0	0	0	0	1	0	AND	0	0	0	0	0
0	0	X	1	0	0	0	0	0	1	0	Complement A	0	0	1	1	1

Conclusion :

There were some issues when we implemented the circuit for the first time. While working with XOR gate, the proteus software was showing some errors such as (No model specified, Simulation Failed due to partition analysis error). But eventually we solved the problem and took the right approach. But even after fixing these errors the circuit was not showing any output. Then finally our circuit was working perfectly after few tweaking here and there.

We solved these 4-bit ALU functions using K-map. The total cost for performing the simulation was reasonable.