

Ahsanullah University of Science and Technology

Department of Computer Science and Engineering

Course Code: CSE3110 Course Name: Digital System Design Lab

Semester: Fall 2020

Group I

Design the following 4-bit ALU (Arithmetic Logic Unit):

S2	S1	S0	Output	Function
1	1	1	$A_i + 1$	Increment A
0	1	1	$A_i + B_i + 1$	Add with Carry
1	1	0	$A_i + B_i$	Add
0	1	0	$A_i + 1 + 1$	Transfer A with Carry
1	0	X	$A_i \cdot B_i$	AND
0	0	X	A_i'	Complement A

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Group III

Design the following 4-bit ALU (Arithmetic Logic Unit):

S2	S1	S0	Output	Function
1	1	0	$A_i - B_i - 1$	Subtract with Borrow
1	1	1	$A_i + B_i$	Add
0	1	1	$A_i + B_i + 1$	Add with Carry
0	1	0	$A_i + 1$	Increment A
1	0	X	$A_i \text{ I } B_i$	OR
0	0	X	$A_i \text{ xor } B_i$	XOR

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Group II

Design the following 4-bit ALU (Arithmetic Logic Unit):

S2	S1	S0	Output	Function
1	0	0	$A_i - 1$	Decrement A
1	0	1	$A_i + 1 + 1$	Transfer A with Carry
0	0	1	$A_i - B_i$	Subtract
0	0	0	$A_i - B_i - 1$	Subtract with Borrow
0	1	X	A_i'	Complement A
1	1	X	$A_i \cdot B_i$	AND

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Group V

Design the following 4-bit ALU (Arithmetic Logic Unit):

S2	S1	S0	Output	Function
0	0	0	$A_i + 1 + 1$	Transfer A with Carry
0	0	1	$A_i - B_i - 1$	Subtraction with Borrow
1	0	0	$A_i - 1$	Decrement A
1	0	1	$A_i + B_i$	Add
0	1	X	$A_i \text{ xor } B_i$	XOR
1	1	X	$A_i B_i$	OR

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Group VII

Design the following 4-bit ALU (Arithmetic Logic Unit):

S2	S1	S0	Output	Function
0	0	0	$A_i - B_i$	Subtract
0	0	1	A_i	Transfer A
0	1	0	$A_i + 1$	Increment A
0	1	1	$A_i + B_i + 1$	Add with Carry
1	0	X	A_i'	Complement A
1	1	X	$A_i \text{ xor } B_i$	XOR

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Group IV

Design the following 4-bit ALU (Arithmetic Logic Unit):

S2	S1	S0	Output	Function
1	0	0	$A_i - 1$	Decrement A
0	0	1	$A_i + 1 + 1$	Transfer with Carry
1	0	1	$A_i + 1$	Increment A
0	0	0	$A_i - B_i - 1$	Subtract with Borrow
0	1	X	$A_i \cdot B_i$	AND
1	1	X	$A_i \mid B_i$	OR

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Group VI

Design the following 4-bit ALU (Arithmetic Logic Unit):

S2	S1	S0	Output	Function
1	0	0	$A_i + 1$	Increment A
0	0	1	$A_i + B_i + 1$	Add with Carry
1	0	1	$A_i + B_i$	Add
0	0	0	$A_i - B_i$	Subtract
0	1	X	$A_i \mid B_i$	OR
1	1	X	A_i'	Complement A