Ahsanullah University of Science and Technology (AUST)

Department of Computer Science and Engineering

LAB REPORT

Course No. : CSE2210

Course Title: Digital Electronics and Pulse Techniques Lab

Experiment Number: 03

Name of the Experiment: Study of a TTL NAND Gate with totem-pole output.

Submitted By:

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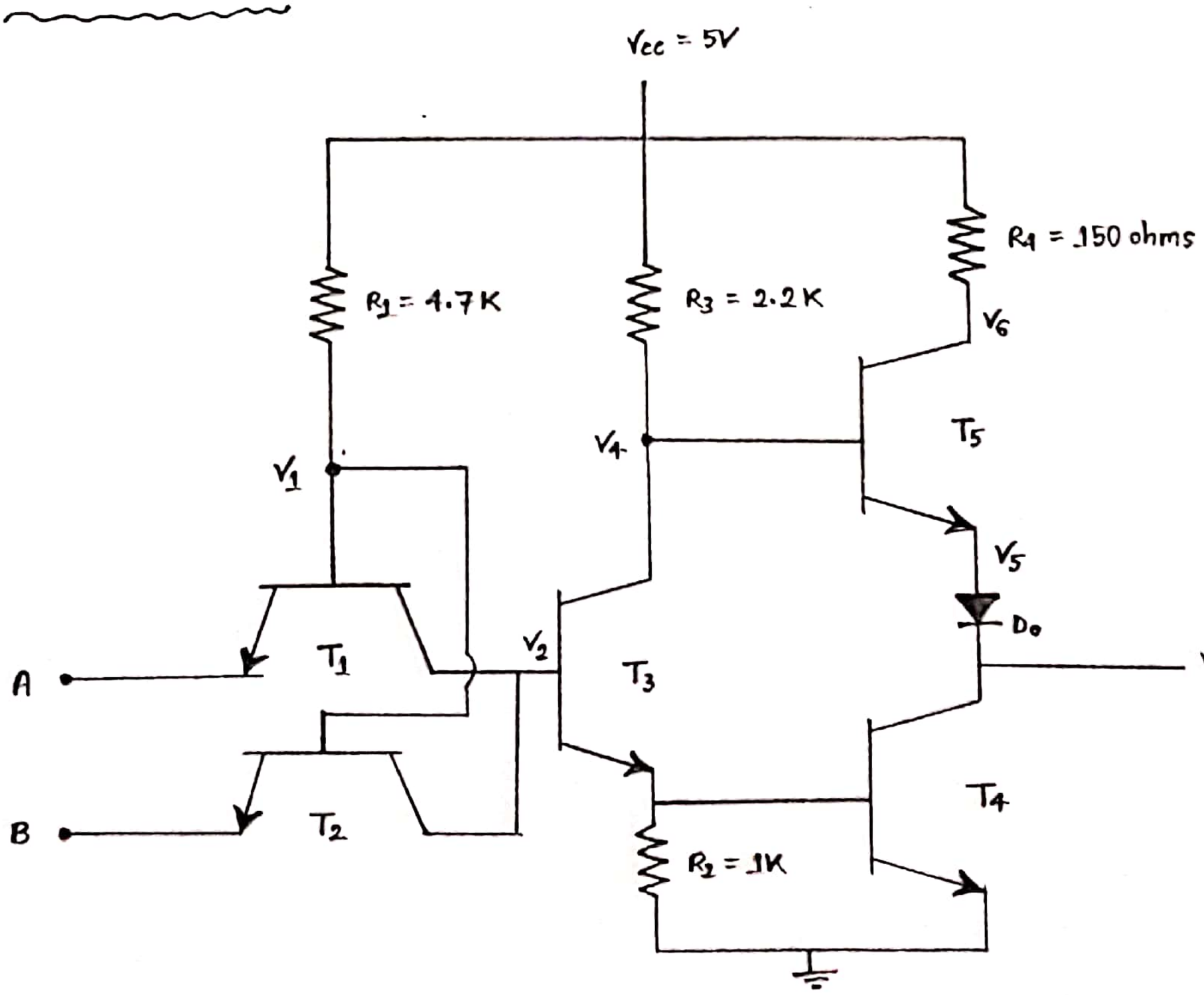
Name of the Experiment :

Study of a TTL NAND gate with totem-pole output.

Objective :

Study of a TTL NAND (Transistor-Transistor Logic) gate with totem-pole output and measure the voltages at various point for all possible input combinations and also find noise margins.

Circuit Diagram :



Answer to the Questions:

① Analyze the operation of TTL NAND gate with the experimental data.

Ans: In this experiment, we have set a circuit where there are two points, A & B. We have used 5 transistors. We have given input voltages to the A & B. We assume ±5 volt is high volt and treated as binary 1 and ±0 volt is low volt and treated as binary 0. After setting up the circuit, for two inputs we may have four possible combinations. The chart is given below -

A	B	V_0 (V)
0	0	4.31
0	1	4.31
1	0	4.31
1	1	0.01

In first three combinations, we can see that there is at least one low volt input. For that we get high volt output. And for the last combination where A & B both are high, we get low volt output. So, by examining the datas we can say that this circuit works like a NAND gate. In fact it is the fastest saturation logic circuit.

(2) What are the differences of transistors T_1 and T_2 with that of a multi-emitter transistor ?

Ans: A multi-emitter transistor is a specialized bipolar transistor mostly used at the input of an IC TTL NAND gate. Input signals are applied to the emitters, collector current stops flowing only if all the emitters are driven by the low voltage (logical).

The differences between T_1 and T_2 in the circuit that we used and a multi-emitter transistor is given below -

① In a multi-emitter transistor there is a connection between every emitter with a diode which acting as an i/p diode. But in T_1 and T_2, there is no connection between emitter and diode.

② In a multi-emitter transistor circuit the collector current stops flowing only if all emitter are driven by the logical low voltage. Whereas in TTL NAND gate circuit collector current depends only with that respective transistor.

③ What is totem-pole stage? Why it is used in place of passive pull-up resistor?

Ans: To solve the problem with the high output resistance of the simple output stage the second schematic is added to this a "Totem-Pole" output. It consists of two n-p-n transistors, the lifting diode and the current limiting resistor.

The totem-pole resistor is used in place of passive pull-up register because in the passive push pull stage, we need two different transistor such as a PNP and a NPN transistor whereas the totem-pole was only uses NPN transistor. This is useful because NPN type transistors are usually easier to make and support higher current for a given size of than PNP type transistors.

In this circuit o/p delay may be reduced by decreasing passive pull-up resistor (R_C) but this will increase the power disipation, when the o/p is in its low state and the voltage accross R_C is $V_{CC} = V_{CE}(sat)$.

To solve this problem totem pole stage is used in the place of passive pull-up resistor.

④ What is the function of T_3 ?

Ans: The transistor T_3 acts as a splitter, since the emitter voltage is out of phase with the collector voltage (for an increase in base current the emitter voltage increases and the collector current decreases). So, the o/p is in the voltage state when T_3 is in saturation.

⑤ Why resistor R_4 is used ?

Ans: In the experimental circuit, we have used T_3 transistor, in the collector of the T_3 transistor, we use R_4 resistor.

If the resistor R_4 is omitted from the circuit that would result a faster change in the o/p from V(0) to V(1). However the R_4 is needed to limit the current supplies during the turn on and turn off transmission. In particular, T_4 doesn't turn off as quiet as T_5 turns on with both totem pole transistor, conducting at the some time. The supply voltage would be short circuited if the R_4 resistor was missing. That's why R_4 resistor is used.

⑥ Why diode D_o is used in the circuit? Can it be placed elsewhere?

Ans: since the base of the transistor T_5 is tied to the collector T_3 when $V_{BN_5} = V_{CN_5} = 1V$. If the o/p diode D_o was missing, the base to emitter voltage of T_5 would be $V_{BE} = V_{BN_5} = V_{CE(sat)} = (1-0.2)V$ $= 0.8V$ which would put T_5 into saturation. So, if we don't use D_o, current would be wasted.

The Diode D_o can be placed from the emitter into the base of T_5. This is also used to establish TTL NAND gates.

⑦ Why two totem-pole gates cannot be wire ANDed?

Ans: It should be said that the wire ANDed connection must not be used with the totem-pole driven circuit, if the o/p from one gate is high while that from a second gate is low and if these two o/p are tied together. We have exactly the situation if the R_4 resistor is not used. That's why two totem pole gates cannot be wire ANDed.

⑧ What are the features and advantages of TTL gates?

Ans: Features:

i) Noise impurity

ii) Noise Margin

iii) Fan in

iv) Fan out

v) Powerz disipation

Advantages :

i) It has strong drive capability.

ii) It has open collector output that is suitable for wired gate.

iii) High availability and compatibility.

iv) Low cost and easy to use.

v) It has power per gate of about 1 - 2.2 mW which is better than emos but not as ECL.

Experimental Data :

A	B	V_0	V_1	V_2	V_3	V_4	V_5	V_6
0	0	4.31	0.53	0.01	0.00	5.00	4.71	5.00
0	1	4.31	0.55	0.03	0.00	5.00	4.71	5.00
1	0	4.31	0.55	0.03	0.00	5.00	4.71	5.00
1	1	0.01	1.66	1.16	0.58	0.61	0.37	5.00

Calculations :

When the i/p of both A & B are high i.e (logically high) 4.31, T_1 and T_2 work as inverse active mode.

The current I is enough for T_3 and T_4 to saturation.

Now, when all inputs are high (1),

$$V_2 + V_3 = (1.16 + 0.58)\,V$$

$$= 1.74\,V$$

$$\therefore NM(0) = -(4.31 - 1.74)\,V$$

$$= -2.57\,V$$

When one input is at V(1) and the others is at V(0), then if V(0) tends to increase we need only (0.5 + 0.5) = 1.0 V at T_3's base to make the path along $T_3 - T_4$ to conduct.

Here, $V_2 = 0.03V$

$\therefore$ NM (1) $= (1 - 0.03)\ V$

$= 0.97\ V$

Discussion of the findings:

In this experiment, we have worked on a TTL NAND Gate with totem pole output. So, when we gave high voltage as both i/p, we get $V_o = 0.01V$ as o/p which is V(0) and for others i/p combinations, we get $V_o = 4.31V$ as o/p which means V(1). From the experimental table's data we can come to a decision that it is a TTL NAND Gate circuit.