AHSANULLAH UNIVERSITY OF SCIENCE & TECHNOLOGY

Department : CSE Program : BSc in CSE

Examination : Lab Final Semester : Fall 2019 Year : 2nd (1st sem.)

Course Number : CSE 2106 Course Name : DLD Lab

Student Name : S. M. TASNIMUL HASAN.

Student ID : 18.02.04.142

Date : 20-09-2020

Ans. to the Q. No. 1

(a) (i) NAND & (iv) NOR

(b) (iv) different.

(c) (i) NAND gates

(d) (iii) 8

(e) (iv) $S=1$, $R=1$

Ans. to the Q.No. 2

Binary Parallel Adders :

Binary Parallel Adders is a combinational circuit consists of various full adders in parallel structure so that when more than 1-bit numbers are to be added, then there can be full adders for every column for the addition.

The numbers of full adders in a binary parallel adders depends on the number of bits present in the numbers for the addition.

Ans. to the Q. No. 3

Shift Registers :

Shift Register is a group of flip flops used to store multiple bits of data. The bits stored in such registers can be made to move within the registers and in/out of the registers by applying clock pulses.

i) The registers which will ~~start~~ shift the bits to left are called "shift left Registers".

ii) The registers which will shift the bits to right are called "shift Right Registers."

Shift registers are basically of 4 types. These are

1. Serial input serial output
2. Serial input parallel output
3. Parallel input serial output
4. Parallel input parallel output.

Ans. to the Q.No. 4

$$F(A,B,C,D) = \Sigma(1,2,5,8,10,13)$$

Truth Table :

Decimal	Input				Output
	A	B	C	D	F
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	1
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	1
9	1	0	0	1	0
10	1	0	1	0	1
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	0
15	1	1	1	1	0

Implementation table :

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{A}$	0	(1)	(2)	3	4	(5)	6	7
A	(8)	9	(10)	11	12	(13)	14	15
	A	$\bar{A}$	1	0	0	1	0	0

Circuit Diagram :