Sec-A

Ahsanullah University of Science and Technology
Department of Computer Science and Engineering

Course Outline

Course No	:	CSE2105
Course Title	:	Digital Logic Design
Credit Hour	:	3.0
Semester (Session)	:	Fall 2019
Student Year & Student Semester:		2nd Year, 1st Semester
Course Teacher(s)	:	Qamrun Nahar Eity, Assistant Professor

Course Objective/Course Outcome (CO):

CO_1: Analyze how a digital computer can perform the complex operations based on simply manipulating bits (zeros and ones).
CO_2: Apply the principles of Boolean algebra to logic functions.
CO_3: Use K-maps to realize two-level minimal/optimal combinational circuits with up to 6 variables, benefits of tabulation method.
CO_4: Understand theory of operation for most of digital electronic devices.
CO_5: Ability to design combinational logic systems.
CO_6: Understand the operation of latches, flip-flops, counters and registers.
CO_7: Analyze and design sequential circuits built with various flip-flops.

Text/ Reference books:

- "Digital Design With An Introduction to the Verilog HDL" By M. Morris Mano, Michael D. Ciletti (5th edition), Prentice Hall, 2012.
- "Digital Fundamentals" By Floyd (11th edition), Pearson Education, 2011.

Topics/Contents	Course Outcome
Introduction to digital logic(analog and digital signal, advantage of digital signal, logic level), Number System, Basic logic operations, truth tables, logic gates, Implementing basic logic operations using NAND and NOR gate, Implementing NOT gate using X-NOR or X-OR gate.	CO_1
BCD/8421 code,Excess-3 code,2-4-2-1 code,8,4,-2,-1code,reflected/ gray code, odd/even parity, Boolean Algebra & logic simplification (commutative, associative, distributive law, rules of Boolean algebra, duality principle, de Morgan's theorems, different examples using the rules of Boolean algebra, simplification using Boolean algebra, Boolean function, implementation of Boolean function with gates).	CO_2
Standard forms of Boolean expressions (SOP,POS),Canonical forms (minterm, maxterm), determining standard expression from a truth table, Conversion between Canonical forms, Quiz#1 (on week 1 to week 2)	CO_2
2,3,4,5,6 variable K Maps, K-Map SOP minimization, K-Map POS minimization, don't care condition, Introduction to combinational logic, design procedure of combinational logic, 3 bit square gate, Code Coverter, Parity Checker and Generator.	CO_3, CO_5
Half adder, full adder, half subtractor, full subtractor, implementation of a full adder using two half adders, binary parallel adder, CLA adder, BCD adder, comparator circuit.	CO_4, CO_5
Multiplexer (2X1, 4X1, 8X1, 16X1 MUX),Design a 16 X1 MUX using two 8X1 MUXs, Boolean function implementation using MUX, Decoder (3X8,4X16 decoder), design a 4X16 decoder using two 3X8 decoders, Boolean function implementation using decoder, Encoder, Priority encoder, Demultiplexer, ALU and Multiplier implementation using Adder,Quiz#2 (on Week 3 to Week 4)	CO_4, CO_5
Design of ROM & PLA, Sequential logic, sequential circuit, asynchronous and synchronous sequential circuits, Flip-flops (Basic flip-flop circuit, SR, D, JK, T flip-flops, triggering of flip-flops, Master slave flip-flop, excitation table,	CO_6, CO_7
Design procedure of sequential circuit, timing diagram, design of counters(Synchronous counter: 2 bit & 3 bit binary counter, binary	CO_6, CO_7

Week	Topics	Course Outcome
10	BCD ripple counter, Ring counter, Johnson ring counter, Mod counter and problem solving regarding counters.	CO_6, CO_7
11	Sequence detectors, Error detection and correction codes (Hamming code)	CO_6, CO_7, CO_1
12	Tabulation Method or Quine-MaCluskey (QM) method, Quiz #4 (on week	CO_3
13	Sequence Detectors	CO_7
14	Review on previous lectures and problem solving.	

Note: *This Lecture Plan is subject to change. Course teacher will slow down or speed up each chapter to meet the needs of students.*

Marks Distribution:

Attendance and Class Performance	10
Class Test	20
Final Exam	70
Total	**100**

FOUR class tests will be taken (as it is a 3-credit course) and best THREE will be considered for "Class Test" marks.