

**DIGITAL CIRCUITS**

Even in a large-scale digital system, such as a computer, or a data-processing, control, or digital-communication system, there are only a few basic operations which must be performed. These operations, to be sure, may be repeated very many times. The four circuits most commonly employed in such systems are known as the OR, AND, NOT, and FLIP-FLOP. These are called *logic* gates, or circuits, because they are used to implement Boolean algebraic equations (as we shall soon demonstrate). This algebra was invented by G. Boole in the middle of the nineteenth century as a system for the mathematical analysis of logic.

This chapter discusses in detail the first three basic logic circuits mentioned above. These basic gates are combined into FLIP-FLOPS and other digital-system building blocks in Chaps. 7, 8, and 9.

**5-1 DIGITAL (BINARY) OPERATION OF A SYSTEM**

A digital system functions in a binary manner. It employs devices which exist only in two possible states. A transistor is allowed to operate at cutoff or in saturation, but not in its active region. A node may be at a high voltage of, say  $4 \pm 1$  V or at a low voltage of, say,  $0.2 \pm 0.2$  V, but no other values are allowed (Fig. 5-1). Various designations are used for these two quantized states, and the most common are 1 or 0, high or low, and true or false. Binary arithmetic and mathematical manipulation of switching or logic functions are best carried out with the classification, which involves two symbols, 0 (zero) and 1 (one).

The binary system of representing numbers will now be explained by making reference to the familiar *decimal system*. In the latter the base is 10 (ten), and ten numerals, 0, 1, 2, 3, . . . , 9, are required to express an arbitrary number. To write numbers larger than 9, we assign a meaning to the *position* of a numeral in an array of numerals. For example, the number 1,264 (one thousand two hundred sixty four) has the meaning

$$1,264 \equiv 1 \times 10^3 + 2 \times 10^2 + 6 \times 10^1 + 4 \times 10^0$$

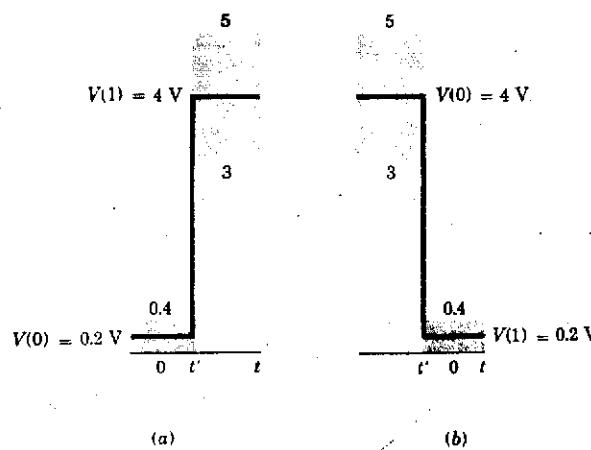


Figure 5-1 Illustrating the definitions of (a) positive and (b) negative logic. A transition from one state to the other occurs at  $t = t'$ .

Thus the individual digits in a number represent the coefficients in an expansion of the number in powers of 10. The digit which is farthest to the right is the coefficient of the zeroth power, the next is the coefficient of the first power, and so on.

In the *binary system* of representation the base is 2, and only the two numerals 0 and 1 are required to represent a number. The numerals 0 and 1 have the same meaning as in the decimal system, but a different interpretation is placed on the position occupied by a digit. In the binary system the individual digits represent the coefficients of powers of two rather than *ten* as in the

Table 5-1 Equivalent numbers in decimal and binary notation

Decimal notation	Binary notation	Decimal notation	Binary notation
0	00000	11	01011
1	00001	12	01100
2	00010	13	01101
3	00011	14	01110
4	00100	15	01111
5	00101	16	10000
6	00110	17	10001
7	00111	18	10010
8	01000	19	10011
9	01001	20	10100
10	01010	21	10101

decimal system. For example, the decimal number 19 is written in the binary representation as 10011 since

$$\begin{aligned}10011 &\equiv 1 \times 2^4 + 0 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 \\&= 16 + 0 + 0 + 2 + 1 = 19\end{aligned}$$

A short list of equivalent numbers in decimal and binary notation is given in Table 5-1.

A binary digit (a 1 or a 0) is called a *bit*. A group of bits having a significance is a *byte*, *word*, or *code*. For example, to represent the 10 numerals (0, 1, 2, ..., 9) and the 26 letters of the English alphabet would require 36 different combinations of 1's and 0's. Since  $2^5 < 36 < 2^6$ , then a minimum of 6 bits per byte are required in order to accommodate all the alphanumeric characters. In this sense a byte is sometimes referred to as a *character*.

### Logic Systems

In a *dc*, or *level-logic*, system a bit is implemented as one of two voltage levels. If, as in Fig. 5-1a, the more positive voltage is the 1 level and the other is the 0 level, the system is said to employ *dc positive logic*. On the other hand, a *dc negative-logic* system, as in Fig. 5-1b, is one which designates the more negative voltage state of the bit as the 1 level and the more positive as the 0 level. It should be emphasized that the absolute values of the two voltages are of no significance in these definitions. In particular, the 0 state need not represent a zero voltage level (although in some systems it might).

The parameters of a physical device (for example,  $V_{CE(sat)}$  of a transistor) are not identical from sample to sample, and they also vary with temperature. Furthermore, ripple or voltage spikes may exist in the power supply or ground leads, and other sources of unwanted signals, called *noise*, may be present in the circuit. For these reasons the digital levels are not specified precisely, but as indicated by the shaded regions in Fig. 5-1, each state is defined by a voltage range about a designated level, such as  $4 \pm 1$  V and  $0.2 \pm 0.2$  V.

In a *dynamic*, or *pulse-logic*, system a bit is recognized by the presence or absence of a pulse. A 1 signifies the existence of a positive pulse in a dynamic positive-logic system; a negative pulse denotes a 1 in a dynamic negative-logic system. In either system a 0 at a particular input (or output) at a given instant of time designates that no pulse is present at that particular moment.

### 5-2 THE OR GATE

An *OR* gate has two or more inputs and a single output, and it operates in accordance with the following definition: *The output of an OR assumes the 1 state if one or more inputs assume the 1 state.* The  $n$  inputs to a logic circuit will be designated by  $A, B, \dots, N$  and the output by  $Y$ . It is to be understood that

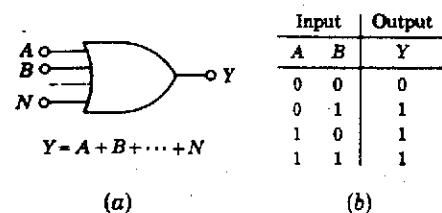


Figure 5-2 (a) The standard symbol for an OR gate and its Boolean expression. (b) The truth table for a two-input OR gate.

each of these symbols may assume one of two possible values, either 0 or 1. A standard symbol for the OR circuit is given in Fig. 5-2a, together with the Boolean expression for this gate. The equation is to be read "Y equals A or B or . . . or N." Instead of defining a logical operation in words, an alternative method is to give a *truth table* which contains a tabulation of all possible input values and their corresponding outputs. It should be clear that the two-input truth table of Fig. 5-2b is equivalent to the above definition of the OR operation.

In a *diode-logic* (DL) system the logical gates are implemented by using diodes. A diode OR for negative logic is shown in Fig. 5-3. The generator source resistance is designated by  $R_s$ . We consider first the case where the supply voltage  $V_R$  has a value equal to the voltage  $V(0)$  of the 0 state for dc logic.

If all inputs are in the 0 state, the voltage across each diode is  $V(0) - V(0) = 0$ . Since, in order for a diode to conduct, it must be forward-biased by at least the cutin voltage  $V_y$  (Fig. 2-7), none of the diodes conducts. Hence the output voltage is  $v_o = V(0)$ , and Y is in the 0 state.

If now input A is changed to the 1 state, which for negative logic is at the potential  $V(1)$ , less positive than the 0 state, then  $D1$  will conduct. The output becomes

$$v_o = V(0) - [V(0) - V(1) - V_y] \frac{R}{R + R_s + R_f} \quad (5-1)$$

where  $R_f$  is the diode forward resistance. Usually  $R$  is chosen much larger than  $R_s + R_f$ . Under this restriction

$$v_o \approx V(1) + V_y \quad (5-2)$$

Hence the output voltage exceeds the more negative level  $V(1)$  by  $V_y$  (approx-

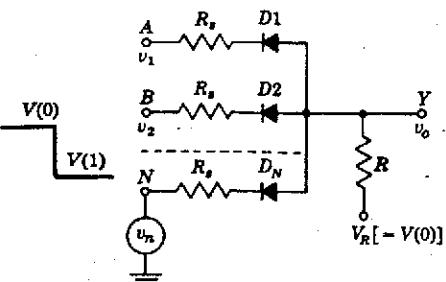


Figure 5-3 A diode OR circuit for negative logic. [It is also possible to choose the supply voltage such that  $V_R > V(0)$ , but that arrangement has the disadvantage of drawing standby current when all inputs are in the 0 state.]

mately 0.6 V for silicon or 0.2 V for germanium). Furthermore, the step in output voltage is *smaller* by  $V_y$  than the change in input voltage.

From now on, unless explicitly stated otherwise, we shall assume  $R \gg R_s$  and ideal diodes with  $R_f = 0$  and  $V_y = 0$ . The output, for input A excited, is then  $v_o = V(1)$ , and the circuit has performed the following logic: if  $A = 1, B = 0, \dots, N = 0$ , then  $Y = 1$ , which is consistent with the OR operation.

For the above excitation, the output is at  $V(1)$ , and each diode, except  $D1$ , is back-biased. Hence the presence of signal sources at  $B, C, \dots, N$  does not result in an additional load on generator A. Since the OR configuration minimizes the interaction of the sources on one another, this gate is sometimes referred to as a *buffer* circuit. Since it allows several independent sources to be applied at a given node, it is also called a (nonlinear) *mixing* gate.

If two or more inputs are in the 1 state, the diodes connected to these inputs conduct and all other diodes remain reverse-biased. The output is  $V(1)$ , and again the OR function is satisfied. If for any reason the level  $V(1)$  is not identical for all inputs, *the most negative value of  $V(1)$  (for negative logic) appears at the output*, and all diodes except one are nonconducting.

A positive-logic OR gate uses the same configuration as that in Fig. 5-3, except that all diodes must be reversed. *The output now is equal to the most positive level  $V(1)$  (or more precisely is smaller than the most positive value of  $V(1)$  by  $V_y$ ).* If a dynamic logic system is under consideration, *the output-pulse magnitude is (approximately) equal to the largest input pulse* (regardless of whether the system uses positive or negative logic).

A second mode of operation of the OR circuit of Fig. 5-3 is possible if  $V_R$  is set equal to a voltage more positive than  $V(0)$  by at least  $V_y$ . For this condition *all diodes conduct in the 0 state, and  $v_o \approx V(0)$  if  $R \gg R_s + R_f$ .* If one or more inputs are excited, then the diode connected to the most negative  $V(1)$  conducts, the output equals this value of  $V(1)$ , and all other diodes are back-biased. Clearly, the OR function has been satisfied.

### Boolean Identities

If it is remembered that  $A, B$ , and  $C$  can take on only the value 0 or 1, the following equations from Boolean algebra pertaining to the OR (+) operation are easily verified:

$$A + B + C = (A + B) + C = A + (B + C) \quad (5-3)$$

$$A + B = B + A \quad (5-4)$$

$$A + A = A \quad (5-5)$$

$$A + 1 = 1 \quad (5-6)$$

$$A + 0 = A \quad (5-7)$$

These equations may be justified by referring to the definition of the OR operation, to a truth table, or to the action of the OR circuits discussed above.

## 5-3 THE AND GATE

An AND gate has two or more inputs and a single output, and it operates in accordance with the following definition: *The output of an AND assumes the 1 state if and only if all the inputs assume the 1 state.* A symbol for the AND circuit is given in Fig. 5-4a, together with the Boolean expression for this gate. The equation is to be read "Y equals A and B and . . . and N." [Sometimes a dot (·) or a cross (×) is placed between symbols to indicate the AND operation.] It may be verified that the two-input truth table of Fig. 5-4b is consistent with the above definition of the AND operation.

A diode-logic (DL) configuration for a negative AND gate is given in Fig. 5-5a. To understand the operation of the circuit, assume initially that all source resistances  $R_s$  are zero and that the diodes are ideal. If *any* input is at the 0 level  $V(0)$ , the diode connected to this input conducts and the output is clamped at the voltage  $V(0)$ , or  $Y = 0$ . However, if *all* inputs are at the 1 level  $V(1)$ , then all diodes are reverse-biased and  $v_o = V(1)$ , or  $Y = 1$ . Clearly, the AND operation has been implemented. The AND gate is also called a *coincidence circuit*.

A positive-logic AND gate uses the same configuration as that in Fig. 5-5a, except that all diodes are reversed. This circuit is indicated in Fig. 5-5b and should be compared with Fig. 5-3. It is to be noted that the symbol  $V(0)$  in Fig. 5-3 designates the same voltage as  $V(1)$  in Fig. 5-5b because each represents the upper binary level. Similarly,  $V(1)$  in Fig. 5-3 equals  $V(0)$  in Fig. 5-5b, since both represent the lower binary level. Hence these two circuits are identical, and we conclude that a *negative OR gate is the same circuit as a positive AND gate*. This result is not restricted to diode logic, and by using Boolean algebra, we show in Sec. 5-7 that it is valid independently of the hardware used to implement the circuit.

In Fig. 5-5b it is possible to choose  $V_R$  to be more positive than  $V(1)$ . If this condition is met, all diodes will conduct upon a coincidence (all inputs in the 1 state) and the output will be clamped to  $V(1)$ . The output impedance is low in this mode of operation, being equal to  $(R_s + R_f)/n$  in parallel with  $R$ . On the other hand, if  $V_R = V(1)$ , then all diodes are cut off at a coincidence, and the output impedance is high (equal to  $R$ ). If for any reason not all inputs have the same upper level  $V(1)$ , then the output of the positive AND gate of Fig. 5-5b will equal  $V(1)_{\min}$ , the *least* positive value of  $V(1)$ . Note that the diode connected to

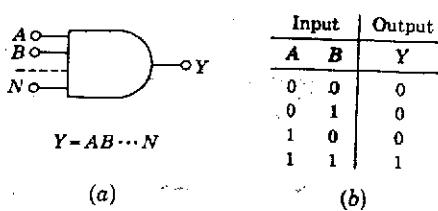


Figure 5-4 (a) The standard symbol for an AND gate and its Boolean expression; (b) The truth table for a two-input AND gate.

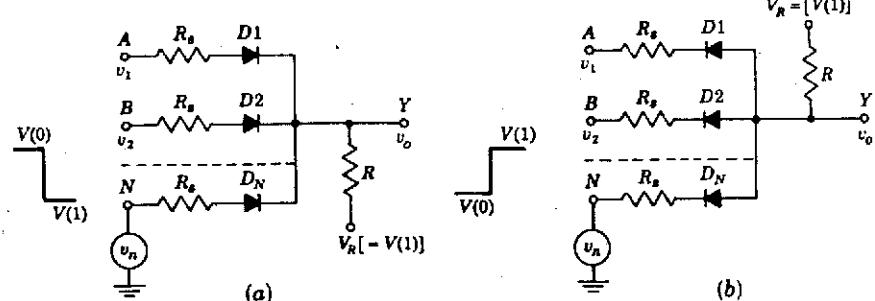


Figure 5-5 A diode-logic AND circuit for (a) negative logic and (b) positive logic.

$V(1)_{\min}$  conducts, clamping the output to this minimum value of  $V(1)$  and maintaining all other diodes in the reverse-biased condition. If, on the other hand,  $V_R$  is smaller than all inputs  $V(1)$ , then all diodes will be cut off upon coincidence and the output will rise to the voltage  $V_R$ . Similarly, if the inputs are pulses, then the *output pulse will have an amplitude equal to the smallest input amplitude* [provided that  $V_R$  is greater than  $V(1)_{\min}$ ].

## Boolean Identities

Since  $A$ ,  $B$ , and  $C$  can have only the value 0 or 1, the following expressions involving the AND operation may be verified:

$$ABC = (AB)C = A(BC) \quad (5-8)$$

$$AB = BA \quad (5-9)$$

$$AA = A \quad (5-10)$$

$$A1 = A \quad (5-11)$$

$$A0 = 0 \quad (5-12)$$

$$A(B + C) = AB + AC \quad (5-13)$$

These equations may be proved by reference to the definition of the AND operation, to a truth table, or to the behavior of the AND circuits discussed above. Also, by using Eqs. (5-11), (5-13), and (5-6), it can be shown that

$$A + AB = A \quad (5-14)$$

Similarly, it follows from Eqs. (5-13), (5-10), and (5-6) that

$$A + BC = (A + B)(A + C) \quad (5-15)$$

We shall have occasion to refer to the last two equations later.

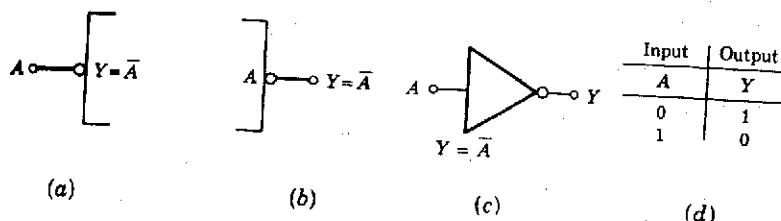


Figure 5-6 Logic negation at (a) the input and (b) the output of a logic block. (c) A symbol often used for a NOT gate and the Boolean equation. (d) The truth table.

#### 5-4 THE NOT (INVERTER) CIRCUIT

The NOT circuit has a single input and a single output and performs the operation of *logic negation* in accordance with the following definition: *The output of a NOT circuit takes on the 1 state if and only if the input does not take on the 1 state.* The standard to indicate a *logic negation* is a small circle drawn at the point where a signal line joins a logic symbol. Negation at the input of a logic block is indicated in Fig. 5-6a and at the output in Fig. 5-6b. The symbol for a NOT gate and the Boolean expression for negation are given in Fig. 5-6c. The equation is to be read "Y equals NOT A" or "Y is the complement of A." [Sometimes a prime (') is used instead of the bar (−) to indicate the NOT operation.] The truth table is given in Fig. 5-6d.

A circuit which accomplishes a logic negation is called a NOT circuit, or, since it inverts the sense of the output with respect to the input, it is also known as an *inverter*. In a truly binary system only two levels  $V(0)$  and  $V(1)$  are recognized, and the output, as well as the input, of an inverter must operate between these two voltages. When the input is at  $V(0)$ , the output must be at  $V(1)$ , and vice versa. Ideally, then, a NOT circuit inverts a signal while preserving its shape and the binary levels between which the signal operates.

The transistor circuit of Fig. 5-7 implements an inverter for positive logic having a 0 state of  $V(0) = V_{CE(sat)} = 0.2$  V and a 1 state of  $V(1) = 12$  V. If the input is low,  $v_i = V(0)$ , then the parameters are chosen so that the  $Q$  is OFF, and hence  $v_o = V_{CC} = V(1)$ . On the other hand, if the input is high,  $v_i = V(1)$ , then

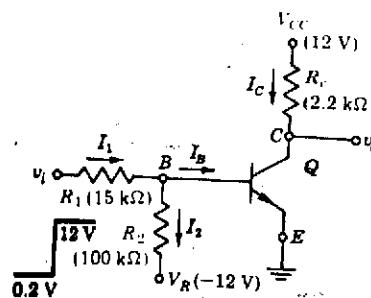


Figure 5-7 An INVERTER for positive logic. A similar circuit using a *p-n-p* transistor is used for a negative-logic NOT circuit.

the circuit parameters are picked so that  $Q$  is in saturation and then  $v_o = V_{CE(sat)} = V(0)$ . A detailed calculation of quiescent conditions is made in the following example.

**Example 5-1** If the silicon transistor in Fig. 5-7 has a minimum value of  $h_{FE}$  of 30, find the output levels for input levels of 0.2 V and 12 V, obtained from a preceding gate.

**SOLUTION** For  $v_i = V(0) = 0.2$  V the open-circuited base voltage  $V_B$  is, using superposition,

$$V_B = -12 \times \frac{15}{100 + 15} + 0.2 \times \frac{100}{100 + 15} = -1.391 \text{ V}$$

Since a bias of about 0 V is adequate to cut off a silicon emitter junction (Table 3-1, page 79), then  $Q$  is indeed cut off. Hence  $v_o = 12$  V for  $v_i = 0$ .

For  $v_i = V(1) = 12$  V let us verify the assumption that  $Q$  is in saturation. The minimum base current required for saturation is

$$I_{B(\min)} = \frac{I_C}{h_{FE}}$$

It is usually sufficiently accurate to use the approximate values for the saturation junction voltages given in Table 3-1, which for silicon are  $V_{BE(sat)} = 0.8$  V and  $V_{CE(sat)} = 0.2$  V. With these values

$$I_C = \frac{12 - 0.2}{2.2} = 5.364 \text{ mA} \quad I_{B(\min)} = \frac{5.36}{30} = 0.179 \text{ mA}$$

$$I_1 = \frac{12 - 0.8}{15} = 0.747 \text{ mA} \quad I_2 = \frac{0.8 - (-12)}{100} = 0.128 \text{ mA}$$

and

$$I_B = I_1 - I_2 = 0.747 - 0.128 = 0.619 \text{ mA}$$

Since this value exceeds  $I_{B(\min)}$ ,  $Q$  is indeed in saturation and the drop across the transistor is  $V_{CE(sat)}$ . Hence  $v_o = 0.2$  V for  $v_i = 12$  V, and the circuit has performed the NOT operation.

#### Transistor Limitations

There are certain transistor characteristics as well as certain circuit features which must particularly be taken into account in designing transistor inverters.

1. *The back-bias emitter-junction voltage  $V_{EB}$ .* This voltage must not exceed the emitter-to-base breakdown voltage  $BV_{EBO}$  specified by the manufacturer. For the type 2N2222A,  $BV_{EBO} = 6$  V.
2. *The dc current gain  $h_{FE}$ .* Since  $h_{FE}$  decreases with decreasing temperature, the circuit must be designed so that at the lowest expected temperature the

transistor will remain in saturation. The maximum value of  $R_t$  is determined principally by this condition.

3. The reverse collector saturation current  $I_{CBO}$ . Since  $|I_{CBO}|$  increases about 7 percent/ $^{\circ}\text{C}$  (doubles every  $10^{\circ}\text{C}$ ), we cannot continue to neglect the effect of  $I_{CBO}$  at high temperatures. At cutoff the emitter current is zero and the base current is  $I_{CBO}$  (in a direction opposite to that indicated as  $I_B$  in Fig. 5-7). Let us calculate the value of  $I_{CBO}$  which just brings the transistor to the point of cutoff. If we assume, as in Table 3-1, that at cutoff,  $V_{BE} = 0$  V, then

$$I_t = 0.2/15 = 0.0133 \text{ mA}$$

The drop across the 100-k $\Omega$  resistor is  $100 I_t = 12$  V and

$$I_{CBO} = I_2 - I_t = 0.12 - 0.013 = 0.107 \text{ mA}$$

The ambient temperature at which  $I_{CBO} = 0.107$  mA =  $107 \mu\text{A}$  is the maximum temperature at which the inverter will operate satisfactorily. A silicon transistor can be operated at temperatures in excess of  $185^{\circ}\text{C}$ .

### Boolean Identities

From the basic definitions of the NOT, AND, and OR connectives we can verify the following Boolean identities:

$$\bar{\bar{A}} = A \quad (5-16)$$

$$\bar{A} + A = 1 \quad (5-17)$$

$$\bar{A}A = 0 \quad (5-18)$$

$$A + \bar{A}B = A + B \quad (5-19)$$

**Example 5-2** Verify Eq. (5-19).

**SOLUTION** Since  $B + \bar{B} = 1$  and  $A\bar{B} = \bar{A}$ , then

$$A + \bar{A}B = A(B + \bar{B}) + \bar{A}B = AB + A + \bar{A}B = (A + \bar{A})B + A = B + A$$

where use is made of Eq. (5-17).

### 5-5 THE INHIBIT (ENABLE) OPERATION

A NOT circuit preceding one terminal ( $S$ ) of an AND gate acts as an *inhibitor*. This modified AND circuit implements the logical statement: *If  $A = 1, B = 1, \dots, M = 1$ , then  $Y = 1$  provided that  $S = 0$ . However, if  $S = 1$ , then the coincidence of  $A, B, \dots, M$  is inhibited (disabled), and  $Y = 0$ .* Such a configuration is also called an *anticoincidence* circuit. The logical block symbol is drawn in Fig. 5-8a, together with its Boolean equation. The equation is to be read "Y

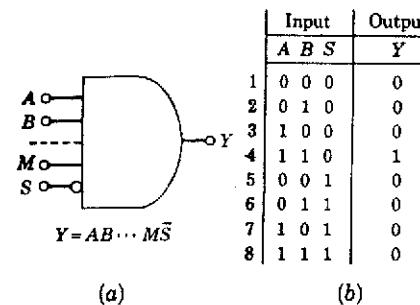


Figure 5-8 (a) The logic block and Boolean expression for an AND with an enable terminal  $S$ . (b) The truth table for  $Y = ABS$ . The column on the left numbers the eight possible input combinations.

equals  $A$  and  $B$  and  $\dots$  and  $M$  and not  $S$ ." The truth table for a three-input AND gate with one inhibitor terminal ( $S$ ) is given in Fig. 5-8b.

The terminal  $S$  is also called a *strobe* or an *enable input*. The enabling bit  $S = 0$  allows the gate to perform its AND logic, whereas the inhibiting bit  $S = 1$  causes the output to remain at  $Y = 0$ , independently of the values of the input bits.

It is possible to have a two-input AND, one terminal of which is inhibiting. This circuit satisfies the logic: "The output is true (1) if input  $A$  is true (1) provided that  $B$  is not true (0) [or equivalently, provided that  $B$  is false (0)]." Another possible configuration is an AND with more than one inhibit terminal.

### 5-6 THE EXCLUSIVE OR CIRCUIT

An EXCLUSIVE OR gate obeys the definition: *The output of a two-input EXCLUSIVE OR assumes the 1 state if one and only one input assumes the 1 state.* The standard symbol for an EXCLUSIVE OR is given in Fig. 5-9a and the truth table in Fig. 5-9b. The circuit of Sec. 5-2 is referred to as an INCLUSIVE OR if it is desired to distinguish it from the EXCLUSIVE OR.

The above definition is equivalent to the statement: "If  $A = 1$  or  $B = 1$  but not simultaneously, then  $Y = 1$ ." In Boolean notation,

$$Y = (A + B)(\bar{A}\bar{B}) \quad (5-20)$$

This function is implemented in logic diagram form in Fig. 5-10a.

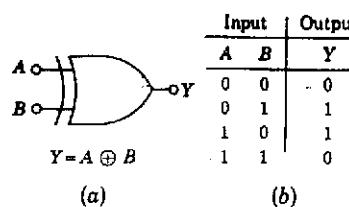


Figure 5-9 (a) The standard symbol for an EXCLUSIVE OR gate and its Boolean expression. (b) The truth table.

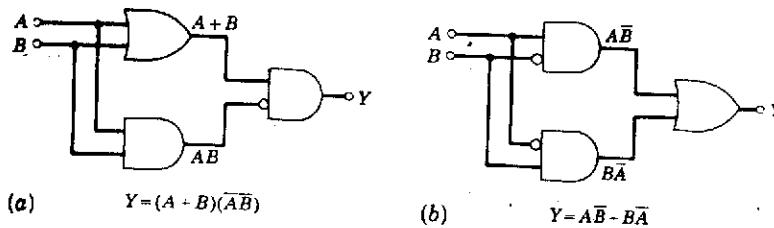


Figure 5-10 Two logic block diagrams for the EXCLUSIVE OR gate.

A second logic statement equivalent to the definition of the EXCLUSIVE OR is the following: "If  $A = 1$  and  $B = 0$ , or if  $B = 1$  and  $A = 0$ , then  $Y = 1$ ." The Boolean expression is

$$Y = A\bar{B} + B\bar{A} \quad (5-21)$$

The block diagram which satisfies this logic is indicated in Fig. 5-10b.

An EXCLUSIVE OR is employed within the arithmetic section of a computer. Another application is as an *inequality comparator, matching circuit, or detector* because, as can be seen from the truth table,  $Y = 1$  only if  $A \neq B$ . This property is used to check for the inequality of two bits. If bit  $A$  is not identical with bit  $B$ , then an output is obtained. Equivalently, "If  $A$  and  $B$  are both 1 or if  $A$  and  $B$  are both 0, then no output is obtained, and  $Y = 0$ ." This latter statement may be put into Boolean form as

$$Y = AB + A\bar{B} \quad (5-22)$$

This equation leads to a third implementation for the EXCLUSIVE OR block, which is indicated by the logic diagram of Fig. 5-11a. An *equality detector* gives an output  $Z = 1$  if  $A$  and  $B$  are both 1 or if  $A$  and  $B$  are both 0, and hence

$$Z = \bar{Y} = AB + A\bar{B} \quad (5-23)$$

where use was made of Eq. (5-16). If the output  $Z$  is desired, the negation in Fig. 5-11a may be omitted or an additional inverter may be cascaded with the output of the EXCLUSIVE OR.

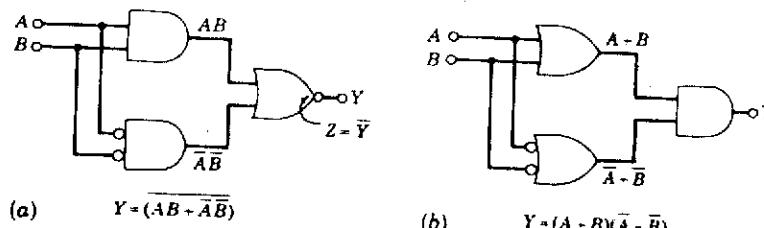


Figure 5-11 Two additional logic block diagrams for the EXCLUSIVE OR gate.

A fourth possibility for this gate is

$$Y = (A + B)(\bar{A} + \bar{B}) \quad (5-24)$$

which may be verified from the definition or from the truth table. This logic is depicted in Fig. 5-11b.

It should be noted that a two-input EXCLUSIVE-OR behaves as a *controlled inverter* or an inverter with a strobe input. Thus, if  $A$  is the input and  $B = S$  is the strobe, then from the truth table of Fig. 5-9 it follows that  $Y = A$  if  $S = 1$ , whereas  $Y = A$  if  $S = 0$ .

We have demonstrated that there often are several ways to implement a logical circuit. In practice one of these may be realized more advantageously than the others. Boolean algebra is sometimes employed for manipulating a logic equation so as to transform it into a form which is better from the point of view of implementation in hardware. In the next section we shall verify through the use of Boolean algebra that the four expressions given above for the EXCLUSIVE OR are equivalent.

### Two-Level Logic

Digital design often calls for several gates (AND, OR, or combinations of those) feeding into an OR (or AND) gate. Such a combination is known as *two-level (or two-wide) logic*. The EXCLUSIVE OR circuits of Figs. 5-10 and 5-11 are examples of two-level logic. In the discussion of combinational systems in Chap. 6 it is found that the most useful logic array consists of several ANDS which feed an OR which is followed by a NOT gate. This cascade of gates (for example, Fig. 5-11b) is called an AND-OR-INVERT (AOI) configuration. The detailed circuit topology for an AOI is given in Fig. 6-1.

### 5-7 DE MORGAN'S LAWS

The following two binary equations are known as De Morgan's theorems:

$$\overline{ABC \dots} = \bar{A} + \bar{B} + \bar{C} + \dots \quad (5-25)$$

$$\overline{A + B + C + \dots} = \bar{A}\bar{B}\bar{C} \dots \quad (5-26)$$

To verify Eq. (5-25) note that if all inputs are 1, then each side of the equation equals 0. On the other hand, if one (or more than one) input is 0, then each side of Eq. (5-25) equals 1. Hence, for all possible inputs the right-hand side of the equation equals the left-hand side. Equation (5-26) is verified in a similar manner. De Morgan's laws complete the list of basic Boolean identities. For each future reference, all these relationships are summarized in Table 5-2.

With the aid of Boolean algebra we shall now demonstrate the equivalence of the four EXCLUSIVE OR circuits of the preceding section. Using Eq. (5-25), it is immediately clear that Eq. (5-20) is equivalent to Eq. (5-24). Now the latter

Table 5-2 Summary of basic Boolean identities

Fundamental laws		
OR	AND	NOT
$A + 0 = A$	$A0 = 0$	$A + \bar{A} = 1$
$A + 1 = 1$	$A1 = A$	$A\bar{A} = 0$
$A + A = A$	$AA = A$	$\bar{\bar{A}} = A$
$A + \bar{A} = 1$	$A\bar{A} = 0$	
Associative laws		
$(A + B) + C = A + (B + C)$	$(AB)C = A(BC)$	
Commutative laws		
$A + B = B + A$	$AB = BA$	
Distributive law		
$A(B + C) = AB + AC$		
De Morgan's laws		
$\overline{AB} = \bar{A} + \bar{B}$		
$A + B + \dots = \bar{A}\bar{B} + \dots$		
Auxiliary identities		
$A + AB = A$	$A + \bar{A}B = A + B$	
$(A + B)(A + C) = A + BC$		

equation can be expanded with the aid of Table 5-2 as follows:

$$(A + B)(\bar{A} + \bar{B}) = A\bar{A} + B\bar{A} + A\bar{B} + B\bar{B} = B\bar{A} + A\bar{B} \quad (5-27)$$

This result shows that the EXCLUSIVE OR of Eq. (5-21) is equivalent to that of Eq. (5-24).

It follows from De Morgan's laws that *to find the complement of a Boolean function change all OR to AND operations, all AND to OR operations, and negate each binary symbol*. If this procedure is applied to Eq. (5-22), the result is Eq. (5-24), if use is made of the identity  $\bar{\bar{A}} = A$ .

With the aid of De Morgan's law we can show that *an AND circuit for positive logic also operates as an OR gate for negative logic*. Let  $Y$  be the output and  $A, B, \dots, N$  be the inputs to a positive AND so that

$$Y = AB \dots N \quad (5-28)$$

Then, by Eq. (5-25),

$$\bar{Y} = \bar{A} + \bar{B} + \dots + \bar{N} \quad (5-29)$$

If the output and all inputs of a circuit are complemented so that a 1 becomes a 0 and vice versa, then positive logic is changed to negative logic (refer to Fig. 5-1). Since  $Y$  and  $\bar{Y}$  represent the same output terminal,  $A$  and  $\bar{A}$  the same input terminal, etc., the circuit which performs the positive AND logic in Eq. (5-28) also operates as the negative OR gate of Eq. (5-29). Similar reasoning is used to verify that the same circuit is either a negative AND or a positive OR, depending upon

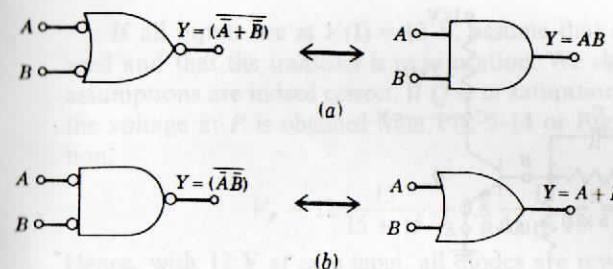


Figure 5-12 (a) An OR is converted into an AND by inverting all inputs and also the output. (b) An AND becomes an OR if all inputs and the output are complemented.

how the binary levels are defined. We verified this result for diode logic in Sec. 5-3, but the present proof is independent of how the circuit is implemented.

It should now be clear that it is really not necessary to use all three connectives OR, AND, and NOT. The OR and the NOT are sufficient because, from the De Morgan law of Eq. (5-25), the AND can be obtained from the OR and the NOT, as is indicated in Fig. 5-12a. Similarly, the AND and the NOT may be chosen as the basic logic circuits, and from the De Morgan law of Eq. (5-26), the OR may be constructed as shown in Fig. 5-12b. This figure makes clear once again that an OR (AND) circuit negated at input and output performs the AND (OR) logic.

## 5-8 THE NAND AND NOR DIODE-TRANSISTOR LOGIC (DTL) GATES

In Fig. 5-10a the negation before the second AND could equally well be put at the output of the first AND without changing the logic. Such an AND-NOT sequence is also present in Fig. 5-12b and in many other logic operations. This negated AND is called a NOT-AND, or a NAND, gate. The logic symbol, Boolean expression, and truth table for the NAND are given in Fig. 5-13. The NAND may be implemented by placing a transistor NOT circuit after a diode AND as in Fig. 5-14. Circuits involving diodes and transistors as in Fig. 5-14 are called diode-transistor logic (DTL) gates.

Input	Output	
	A	B
0 0	1	
0 1	1	
1 0	1	
1 1	0	

(a) (b)

Figure 5-13 (a) The logic symbol and Boolean expression for a two-input NAND gate. (b) The truth table.

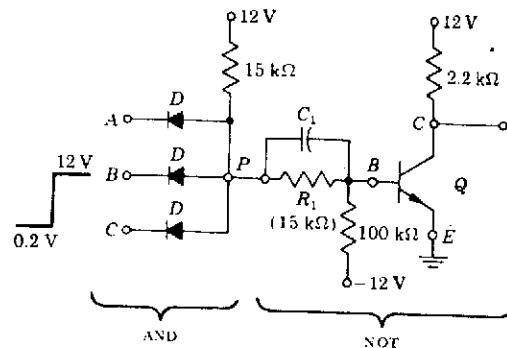


Figure 5-14 A three-input positive NAND (or negative NOR) gate.

The capacitor  $C_1$  across  $R_1$  in Fig. 5-14 is added to improve the transient response of the inverter. This capacitor aids in the removal of the minority-carrier saturation charge stored in the base when the signal changes abruptly between logic states. A transistor cannot come out of saturation until this charge is taken from the base region. The interval required to remove the saturation charge is called the *storage time*  $t_s$ . A discussion of this phenomenon is given in Sec. 3-14.

**Example 5-3** Verify that the circuit of Fig. 5-14 is a positive NAND if the inputs are obtained from the outputs of similar NAND gates. Silicon transistors and diodes are used. Assume that the drop across a conducting diode is 0.7 V. Find the minimum value of  $h_{FE}$  for proper operation of the gate.

**SOLUTION** Consider that at least one input is low. We must verify that the output is high. The low input now comes from a transistor in saturation, and  $V_{CE(sat)} \approx 0.2$  V. The open-circuit voltage at the base of  $Q$  is, from Fig. 5-15a, using superposition,

$$V_B = -12 \frac{15}{100 + 15} + 0.9 \frac{100}{100 + 15} = -0.782 \text{ V}$$

which cuts off  $Q$  and  $Y = 1$ , as it should.

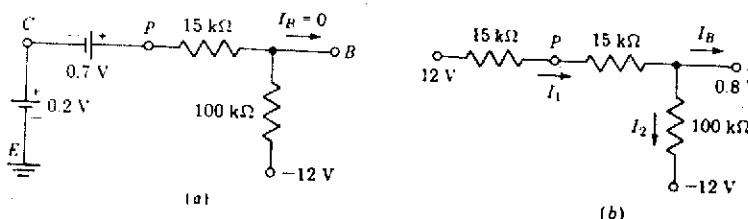


Figure 5-15 Relating to calculations in the circuit of Fig. 5-14. (a) At least one input is low. (b) All inputs are high.

If all inputs are at  $V(1) = 12$  V, assume that all diodes are reverse-biased and that the transistor is in saturation. We shall now verify that these assumptions are indeed correct. If  $Q$  is in saturation, then with  $V_{BE} = 0.8$  V, the voltage at  $P$  is obtained from Fig. 5-14 or Fig. 5-15b. Using superposition,

$$V_P = 12 \frac{15}{15 + 15} + 0.8 \frac{15}{15 + 15} = 6.40 \text{ V}$$

Hence, with 12 V at each input, all diodes are reverse-biased by  $12 - 6.40 = 5.60$  V. From Fig. 5-15b and Fig. 5-14,

$$I_1 = \frac{12 - 0.8}{15 + 15} = 0.373 \text{ mA} \quad I_2 = \frac{0.8 + 12}{100} = 0.128 \text{ mA}$$

$$I_B = 0.373 - 0.128 = 0.245 \text{ mA} \quad I_C = \frac{12 - 0.2}{2.2} = 5.364 \text{ mA}$$

$$h_{FE(\min)} = \frac{I_C}{I_B} = \frac{5.364}{0.245} = 21.9$$

If  $h_{FE} \geq 21.9$ , then  $Q$  will indeed be in saturation and the output is  $V_{CE(sat)} = 0.2$  V =  $V(0)$ , as it should be if all the inputs are high.

### A NOR Gate

A negation following an OR is called a NOT-OR, or a NOR gate. The logic symbol, Boolean expression, and truth table for the NOR are given in Fig. 5-16. A positive NOR circuit is implemented by a cascade of a diode OR and a transistor INVERTER.

The circuit of Fig. 5-14 employs *diode-transistor logic* (DTL). The NAND and NOR may also be implemented in other configurations, as is indicated in Secs. 5-9 through 5-14. With the aid of De Morgan's laws, it can be shown that, regardless of the hardware involved, a positive NAND is also a negative NOR, whereas a negative NAND may equally well be considered a positive NOR.

It is clear that a single input NAND is a NOT. Also, a NAND followed by a NOT is an AND. In Sec. 5-7 it is pointed out that all logic can be performed by using only the two connectives AND and NOT. Therefore we now conclude that, by repeated use of the NAND circuit alone, any logical function can be carried out. A similar argument leads equally well to the result that all logic can be performed by using only the NOR circuit.

Input	Output	
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

$Y = \overline{A+B}$

(a) (b)

Figure 5-16 (a) The logic symbol and Boolean expression for a two-input NOR gate. (b) The truth table.

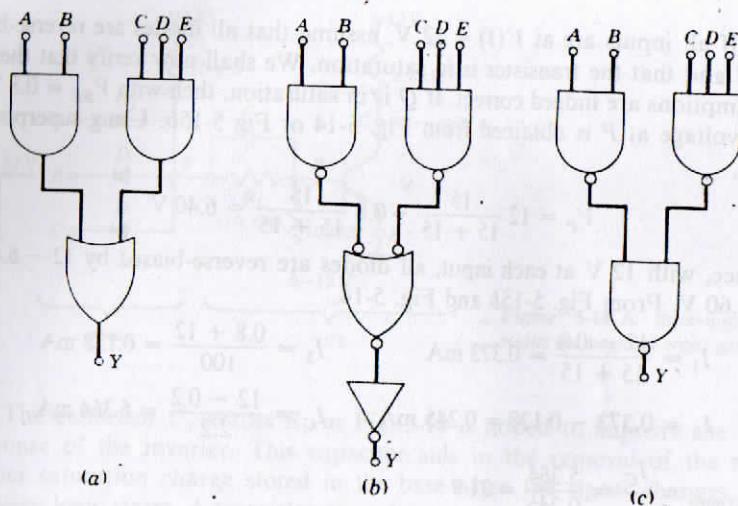


Figure 5-17 A two-level AND-OR is equivalent to a NAND-NAND configuration.

**Example 5-4** Verify that two-level AND-OR topology is equivalent to a NAND-NAND system.

**SOLUTION** The AND-OR logic is indicated in Fig. 5-17a. Since  $X = \bar{X}$ , then inverting the output of an AND and simultaneously negating the input to the following OR does not change the logic. These modifications are made in Fig. 5-17b. We have also negated the output of the OR gate and, at the same time, have added an INVERTER to Fig. 5-17b, so that once again the logic is unaffected. An OR gate negated at each terminal is an AND circuit (Fig. 5-12a). Since an AND followed by an INVERTER is a NAND then Fig. 5-17c is equivalent to Fig. 5-17b. Hence, the NAND-NAND of Fig. 5-17c is equivalent to the AND-OR of Fig. 5-17a.

If any of the inputs in Fig. 5-17 are obtained from the output of another gate then the resultant topology is referred to as *three-level logic*.

## 5-9 MODIFIED (INTEGRATED-CIRCUIT) DTL GATES<sup>1,2</sup>

Most logic gates are fabricated as an *integrated circuit* (IC). This process is described in Chap. 4, where it is found that large values of resistance (above  $30\text{ k}\Omega$ ) and of capacitance (above  $100\text{ pF}$ ) cannot be fabricated economically. On the other hand, transistors and diodes may be constructed very inexpensively. In view of these facts, the NAND gate of Fig. 5-14 is modified for integrated-circuit implementation by eliminating the capacitor  $C_1$ , reducing the resistance values

drastically, and using diodes or transistors to replace resistors wherever possible. At the same time the power-supply requirements are simplified so that only a single 5-V supply is used. The resulting circuit is indicated in Fig. 5-18.

The operation of this positive NAND gate is easily understood qualitatively. If at least one of the inputs is low (the 0 state), the diode  $D$  connected to this input conducts and the voltage  $V_P$  at point  $P$  is low. Hence diodes  $D_1$  and  $D_2$  are nonconducting,  $I_B = 0$ , and the transistor is OFF. Therefore the output of  $Q$  is high and  $Y$  is in the 1 state. This logic satisfies the first three rows of the truth table in Fig. 5-13. Consider now the case where all inputs are high (1) so that all input diodes  $D$  are cut off. Then  $V_P$  tries to rise toward  $V_{CC}$ , and a base current  $I_B$  results. If  $I_B$  is sufficiently large,  $Q$  is driven into saturation and the output  $Y$  falls to its low (0) state, thus satisfying the fourth row of the truth table.

This NAND gate is considered quantitatively in the following illustrative example. The necessity for using two diodes  $D_1$  and  $D_2$  in series is explained. False logic can be caused by switching transients, power-supply noise spikes, coupling between leads, etc. The noise voltage at the input which will cause the circuit to malfunction when the output is in the 0(1) state is called the *noise-margins*  $NM(0)$  [ $NM(1)$ ]. These noise margins are calculated below.

**Example 5-5** (a) For the transistor in Fig. 5-18 assume (Table 3-1) that  $V_{BE(sat)} = 0.8\text{ V}$ ,  $V_Y = 0.5\text{ V}$ , and  $V_{CE(sat)} = 0.2\text{ V}$ . The drop across a conducting diode is  $0.7\text{ V}$  and  $V_{(diode)} = 0.6\text{ V}$ . The inputs of this switch are obtained from the outputs of similar gates. Verify that the circuit functions as a positive NAND and calculate  $h_{FE(\min)}$ . (b) Will the circuit operate properly if  $D_2$  is not used? (c) Calculate  $NM(0)$ . (d) Calculate  $NM(1)$ . Assume, for the moment, that  $Q$  is not loaded by a following stage.

**SOLUTION** (a) The logic levels are  $V_{CE(sat)} = 0.2\text{ V}$  for the 0 state and  $V_{CC} = 5\text{ V}$  for the 1 state. If at least one input is in the 0 state, its diode conducts and  $V_P = 0.2 + 0.7 = 0.9\text{ V}$ . Since, in order for  $D_1$  and  $D_2$  to be

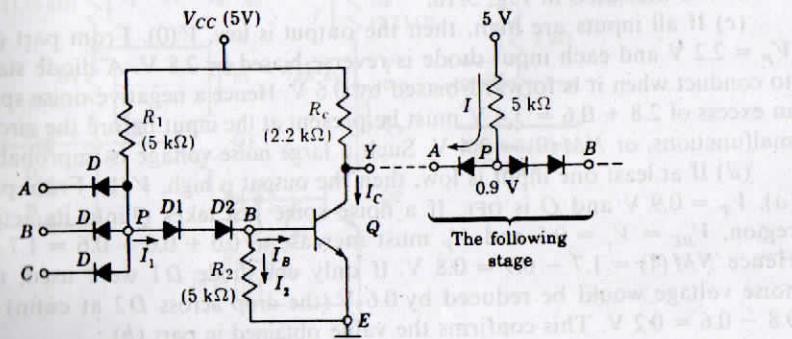


Figure 5-18 An integrated positive DTL NAND gate.

conducting, a voltage of  $(2)(0.7) = 1.4$  V is required, these diodes are cut off and  $V_{BE} = 0$ . Since the cutin voltage of  $Q$  is  $V_y = 0.5$  V, then  $Q$  is OFF, the output rises to 5 V, and  $Y = 1$ . This confirms the first three rows of the NAND truth table.

If all inputs are at  $V(1) = 5$  V, then we shall assume that all input diodes are OFF, that  $D_1$  and  $D_2$  conduct, and that  $Q$  is in saturation. If these conditions are true, the voltage at  $P$  is the sum of two diode drops plus  $V_{BE(sat)}$  or  $V_P = 0.7 + 0.7 + 0.8 = 2.2$  V. The voltage across each input diode is  $5 - 2.2 = 2.8$  V in the reverse direction, thus justifying the assumption that  $D$  is OFF. We now find  $h_{FE(\min)}$  to put  $Q$  into saturation.

$$I_1 = \frac{V_{CC} - V_P}{R_1} = \frac{5 - 2.2}{5} = 0.560 \text{ mA}$$

$$I_2 = \frac{V_{BE(sat)}}{R_s} = \frac{0.8}{5} = 0.160 \text{ mA}$$

$$I_B = I_1 - I_2 = 0.560 - 0.160 = 0.400 \text{ mA}$$

$$I_C = \frac{V_{CC} - V_{CE(\text{sat})}}{R_s} = \frac{5 - 0.2}{22} = 2.182 \text{ mA}$$

$$\text{and } h_{FE(\min)} = \frac{I_C}{I_B} = \frac{2.182}{0.400} = 5.46$$

If  $h_{FE} > h_{FE(\min)}$ , then  $Y = V(0)$  for all inputs at  $V(1)$ , thus verifying the last line in the truth table in Fig. 5.13.

(b) If at least one input is at  $V(0)$ , then  $V_P = 0.2 + 0.7 = 0.9$  V. Hence if only one diode  $D1$  is used between  $P$  and  $B$ , then  $V_{BE} = 0.9 - 0.6 = 0.3$  V, where 0.6 V represents the diode cutin voltage. Since the cutin base voltage is  $V_y = 0.5$  V, then theoretically  $Q$  is cut off. However, this is not a very conservative design because a small ( $> 0.2$  V) spike of noise will turn  $Q$  ON. An even more conservative design uses three diodes in series, instead of the two indicated in Fig. 5-18.

(c) If all inputs are high, then the output is low,  $V(0)$ . From part (a)  $V_p = 2.2$  V and each input diode is reverse-biased by 2.8 V. A diode starts to conduct when it is forward-biased by 0.6 V. Hence a negative noise spike in excess of  $2.8 + 0.6 = 3.4$  V must be present at the input before the circuit malfunctions, or  $NM(0) = 3.4$  V. Such a large noise spike is unlikely.

(d) If at least one input is low, then the output is high,  $V(1)$ . From part (a),  $V_P = 0.9$  V and  $Q$  is OFF. If a noise spike just takes  $Q$  into its active region,  $V_{BE} = V_y = 0.5$  and  $V_P$  must increase to  $0.5 + 0.6 + 0.6 = 1.7$  V. Hence  $NM(1) = 1.7 - 0.9 = 0.8$  V. If only one diode  $D1$  were used, the noise voltage would be reduced by 0.6 V (the drop across  $D2$  at cutin) to  $0.8 - 0.6 = 0.2$  V. This confirms the value obtained in part (b).

### Fan-out

In the foregoing discussion we have unrealistically assumed that the NAND gate is unloaded. If it drives  $N$  similar gates, we say that the *fan-out* is  $N$ . The output transistor now acts as a *sink* for the current in the input to the gates it drives. In other words, when  $Q$  is in saturation ( $Y = 0$ ), the input current  $I$  in Fig. 5-18 of a following stage adds to the collector current of  $Q$ . Assume that all the input diodes to a following stage (which is now considered to be a *current source*) are high except the one driven by  $Q$ . Then the current in this diode is  $I = (5 - 0.9)/5 = 0.820$  mA. This current is called a *standard load*. The total collector current of  $Q$  is now  $I_C = 0.820N + 2.182$  mA, where 2.182 mA is the unloaded collector current found in part *a* of the preceding example. Since the base current is almost independent of loading,  $I_B$  remains at its previous value of 0.400 mA. If we assume a reasonable value for  $h_{FE(\min)}$  of 30, the fan-out is given by  $I_C = h_{FE}I_B$ , or

$$I_s \equiv 0.820N + 2.182 = (30)(0.400) = 12.00 \text{ mA} \quad (5-30)$$

and  $N = 11.97$ . Since  $N$  must be an integer, a conservative choice is  $N = 11$ . Of course, the current rating of  $O$  must not be exceeded.

The fan-out may be increased considerably by replacing  $D1$  by a transistor  $Q1$ , as indicated in Fig. 5-19. When  $Q1$  is conducting, it is in its active region and not in saturation. This statement follows from the fact that the current in the  $2-k\Omega$  resistance is in the direction to reverse-bias the collector junction of the  $n-p-n$  transistor  $Q1$ . Since the emitter current of  $Q1$  supplies the base current of  $Q2$ , then  $Q2$  is driven by a much higher base current than is  $Q$  in Fig. 5-18. For the same  $h_{FE(\min)}$  of the output transistors in Figs. 5-18 and 5-19, it is clear that the latter circuit has the larger collector current, and hence the larger fan-out.

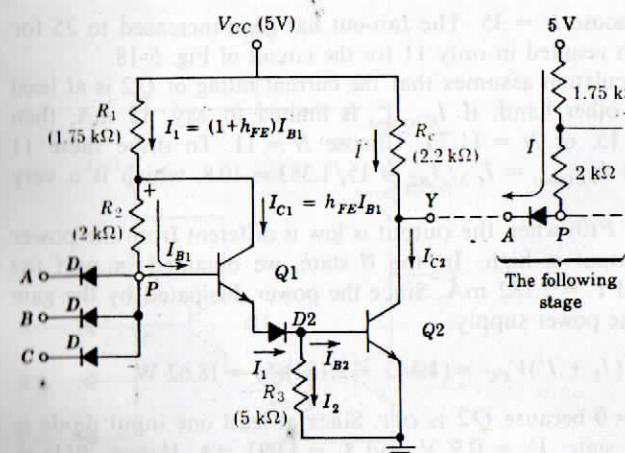


Figure 5-19 A modified integrated positive DTL NAND gate with increased fan-out.

**Example 5-6** If  $h_{FE(\min)} = 30$ , calculate the fan-out  $N$  for the NAND gate of Fig. 5-19. From Table 3-1,  $V_{BE(\text{active})} = 0.7$  V. (b) Calculate the average power  $P$  dissipated by the gate.

**SOLUTION** (a) As with the circuit of Fig. 5-18, if any input is low, then  $V_P = 0.9$  V, and both  $Q1$  and  $D2$  are OFF. Hence  $V_{BE2} = 0$ ,  $Q2$  is OFF, and  $Y = 1$ . If, however, all inputs are high, the input diodes are OFF,  $Q2$  goes into saturation, and

$$V_P = V_{BE(\text{active})} + V_{D2} + V_{BE2(\text{sat})} = 0.7 + 0.7 + 0.8 = 2.2 \text{ V}$$

Since  $Q1$  is in its active region,  $I_{C1} = h_{FE}I_{B1}$ . As indicated in Fig. 5-19, the current in  $R_2$  is  $I_{B1}$  (remember that each  $D$  is cut off), and the current in  $R_1$  is  $I_1 = I_{B1} + I_{C1} = (1 + h_{FE})I_{B1}$ . Applying KVL between  $V_{CC}$  and  $V_P$ , we have, for  $h_{FE} = 30$ ,

$$5 - 2.2 = (1.75)(31)I_{B1} + 2I_{B1} \quad (5-31)$$

or

$$I_{B1} = 0.0498 \text{ mA} \quad I_1 = (31)(0.0498) = 1.543 \text{ mA}$$

$$I_2 = 0.8/5 = 0.160 \text{ mA} \quad I_{B2} = 1.543 - 0.160 = 1.383 \text{ mA}$$

The unloaded collector current of  $Q2$  is  $I' = (5 - 0.2)/2.2 = 2.182 \text{ mA}$ . For each gate which it drives,  $Q2$  must sink a standard load of

$$I = \frac{5 - 0.7 - 0.2}{1.75 + 2} = 1.093 \text{ mA}$$

Since the maximum collector current is  $h_{FE}I_{B2}$ , and  $I_{C2} = IN + I'$ , then

$$I_{C2} = (30)(1.383) = 1.093N + 2.182 = 41.49 \text{ mA} \quad (5-32)$$

and  $N = 35.96$ . Choose  $N = 35$ . The fan-out has been increased to 35 for the same  $h_{FE}$  which resulted in only 11 for the circuit of Fig. 5-18.

The above calculation assumes that the current rating of  $Q2$  is at least 41.5 mA. On the other hand, if  $I_{C2(\max)}$  is limited to, say, 15 mA, then  $1.093N + 2.182 = 15$ , or  $N = 11.73$ . Choose  $N = 11$ . To drive these 11 gates requires that  $h_{FE(\min)} = I_{C2}/I_{B2} = 15/1.383 = 10.8$ , which is a very small number.

(b) The power  $P(0)$  when the output is low is different from the power  $P(1)$  when the output is high. In the 0 state, we obtained in part (a)  $I_1 = 1.543 \text{ mA}$  and  $I' = 2.182 \text{ mA}$ . Since the power dissipated by the gate must come from the power supply,

$$P(0) = (I_1 + I')V_{CC} = (1.543 + 2.182)(5) = 18.62 \text{ W}$$

In the 1 state,  $I' = 0$  because  $Q2$  is OFF. Since at least one input diode is conducting in this state,  $V_P = 0.9 \text{ V}$  and  $I_1 = 1.093 \text{ mA}$ . Hence,  $P(1) = (1.093)(5) = 5.47 \text{ W}$ .

If we assume that in a particular system this gate is equally likely to be in either state, then the average power is

$$P_{av} = \frac{P(0) + P(1)}{2} = \frac{18.62 + 5.47}{2} = 12.04 \text{ W}$$

Note that the output voltages are almost independent of the fan-out. The low-level  $V(0) = V_{CE(\text{sat})}$  does not vary appreciably with  $I_{C2}$  (and hence  $N$ ). The high-level  $V(1) = V_{CC} - I''R_c$  where  $I''$  is the reverse saturation current of the fan-out diodes (which are reverse-biased in the 1 state). At room temperature,  $I''R_c \ll V_{CC}$  and  $V(1) \approx V_{CC}$ , independent of the fan-out. However, at highly elevated temperatures and large values of  $N$ , the high-level  $V(0)$  may fall appreciably below  $V_{CC}$  (Prob. 5-42).

The fan-in  $M$  of a logic gate gives the number of inputs to the switch. For example, in Fig. 5-19,  $M = 3$ .

## 5-10 HIGH-THRESHOLD-LOGIC (HTL) GATE<sup>2</sup>

In an industrial environment the noise level is quite high because of the presence of motors, high-voltage switches, on-off control circuits, etc. By using a higher supply voltage (15 V instead of 5 V) and a 6.9-V Zener diode in place of  $D2$  in the DTL gate of Fig. 5-19, this circuit is converted into the high-noise-immunity gate of Fig. 5-20. The resistances are increased in Fig. 5-20 with respect to those in Fig. 5-19, so that approximately the same currents are obtained in both circuits. The noise margin obtained with this circuit is typically 7 V (Prob. 5-46).

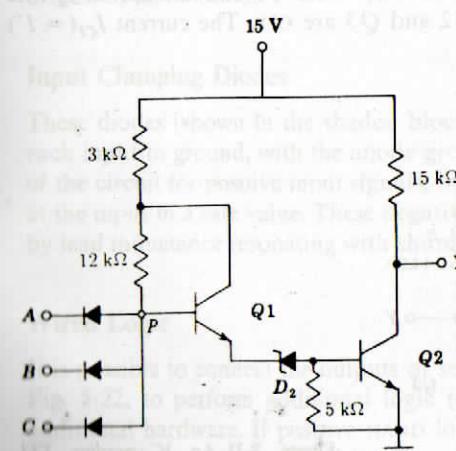


Figure 5-20 A high-threshold-logic NAND gate.

## 5-11 TRANSISTOR-TRANSISTOR-LOGIC (TTL) GATE<sup>1,3</sup>

The fastest-saturating logic circuit is the transistor-transistor-logic gate (TTL, or  $T^2L$ ), shown in Fig. 5-21. This switch uses a multiple-emitter transistor which is easily and economically fabricated using integrated-circuit techniques (Sec. 4-7). The TTL circuit has the topology of the DTL circuit of Fig. 5-18, with the emitter junctions of  $Q1$  acting as the input diodes  $D$  of the DTL gate and the collector junction of  $Q1$  replacing the diode  $D1$  of Fig. 5-18. The base-to-emitter diode of  $Q2$  is used in place of the diode  $D2$  of the DTL gate, and both circuits have an output transistor ( $Q3$  or  $Q$ ).

The explanation of the operation of the TTL gate parallels that of the DTL switch. Thus, if at least one input is at  $V(0) = 0.2$  V, then

$$V_P = 0.2 + 0.7 = 0.9 \text{ V}$$

For the collector junction of  $Q1$  to be forward-biased and for  $Q2$  and  $Q3$  to be ON requires about  $0.7 + 0.7 + 0.7 = 2.1$  V. Hence these are OFF; the output rises to  $V_{CC} = 5$  V, and  $Y = V(1)$ . On the other hand, if all inputs are high (at 5 V), the input diodes (the emitter junctions) are reverse-biased and  $V_P$  rises toward  $V_{CC}$  and drives  $Q2$  and  $Q3$  into saturation. Then the output is  $V_{CE(sat)} = 0.2$  V, and  $Y = V(0)$  (and  $V_P$  is clamped at about 2.3 V).

### Input Transistor Action

The explanation given in the preceding paragraph assumes that  $Q1$  acts like isolated back-to-back diodes and not as a transistor. The above conclusions are also reached if the transistor behavior of  $Q1$  is taken into consideration.

**Condition I.** At least one input is low.  $v_i = 0.2$  V. The emitter of  $Q1$  is forward-biased and we assume that  $Q2$  and  $Q3$  are OFF. The current  $I_{CI} (= I')$

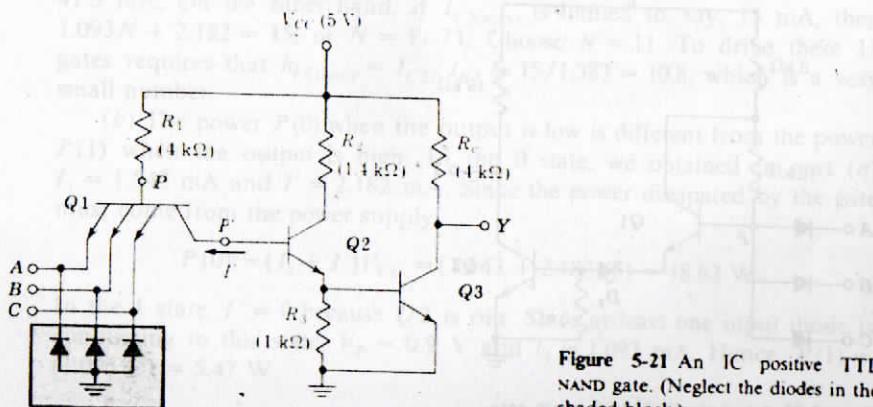


Figure 5-21 An IC positive TTL NAND gate. (Neglect the diodes in the shaded block.)

into the collector  $P'$  must be the current from emitter to base of  $Q2$ . Hence,  $I_{CI}$  equals the reverse saturation current of the emitter-junction diode of  $Q2$ . Since this current is very small (a few nanoamperes),  $I_{BI} \gg I_{CI}/h_{FE}$  and  $Q1$  is in saturation. The voltage at  $P'$  equals  $V_{CE(sat)} + v_i = 0.2 + 0.2 = 0.4$  V. This voltage is too small to put  $Q2$  and  $Q3$  ON. This argument justifies our assumptions that  $Q2$  and  $Q3$  are OFF and, therefore,  $Y = V(1) = V_{CC}$ .

**Condition II: All inputs are high.** The emitters of  $Q1$  are reverse-biased, whereas the collector is forward-biased, because the  $p$ -type base is connected to the positive 5-V supply (through the 4-kΩ resistor). Hence,  $Q1$  is operating in the inverted mode (Sec. 3-11). The inverted-current gain  $h_{FE}$  for an IC transistor is very small ( $< 1$ ). The input current (now the collector current of the inverted transistor) is  $h_{FE}I_{BI}$ . The current  $I'$  (now the emitter current of the inverted transistor) is  $-(1 + h_{FE})I_{BI}$ . This large current saturates  $Q2$  and  $Q3$  and  $Y = V(0)$ . This concludes the argument that Fig. 5-21 obeys NAND logic.

### Low Storage Time

We now show that, because of the transistor behavior of  $Q1$  during turnoff, the storage time  $t_s$  (Sec. 3-14) is reduced considerably. Note that the base voltage of  $Q2$ , which equals the collector voltage of  $Q1$ , is at  $0.8 + 0.8 = 1.6$  V during saturation of  $Q2$  and  $Q3$ . If now any input drops to 0.2 V, then  $V_P = 0.9$  V, and hence the base of  $Q1$  is at 0.9 V. At this time the collector junction is reverse-biased by  $1.6 - 0.9 = 0.7$  V, the emitter junction is forward-biased, and  $Q1$  is in its active region. The large collector current  $I'$  of  $Q1$  now quickly removes the stored charge in  $Q2$  and  $Q3$ . It is this transistor action which gives TTL the highest speed of any saturated logic. It is not until all the charge is removed from  $Q3$  and  $Q2$  (so that these transistors go OFF) that  $Q1$  saturates, as discussed in Condition I.

### Input Clamping Diodes

These diodes (shown in the shaded block in Fig. 5-21) are often included from each input to ground, with the anode grounded. These diodes are effectively out of the circuit for positive input signals, but they limit negative voltage excursions at the input to a safe value. These negative signals may arise from ringing caused by lead inductance resonating with shunt capacitance.

### Wired Logic

It is possible to connect the outputs of several TTL or DTL gates together, as in Fig. 5-22, to perform additional logic (called *wired* or *collector logic*) without additional hardware. If positive NAND logic is under consideration, this connection is called a *wired-AND*, *phantom-AND*, *dotted-AND*, or *implied-AND*. Thus, if both  $Y_1 = 1$  and  $Y_2 = 1$ , then  $Y = 1$ , whereas if  $Y_1 = 0$  and/or  $Y_2 = 0$ , then  $Y = 0$ .

Sec. 5-12

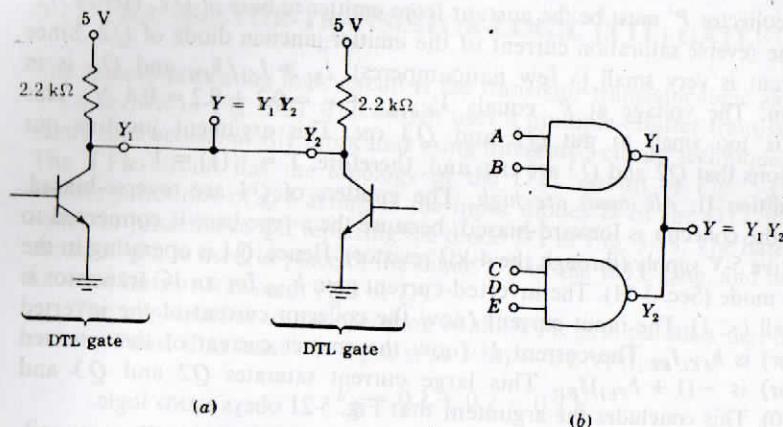


Figure 5-22 (a) Wired-AND logic is obtained by connecting the outputs of positive NAND gates together. (b) A two-input and a three-input NAND gate wired-AND together to perform the logic in Eq. (5-33).

The circuit of Fig. 5-21 also represents a negative NOR gate; and connecting two outputs together as in Fig. 5-22 now represents negative wired-OR logic. If  $Y_1$  and/or  $Y_2$  is in the low state (which is now the 1 state), then  $Y$  is also in the low state ( $Y = 1$ ), whereas if  $Y_1$  and  $Y_2$  are both high (the 0 state), then  $Y$  is also high ( $Y = 0$ ).

Consider two positive NAND gates wired-AND together as in Fig. 5-22b. Then  $Y_1 = \overline{AB}$  and  $Y_2 = \overline{CDE}$ . Hence

$$Y = Y_1 Y_2 = (\overline{AB})(\overline{CDE}) = \overline{AB + CDE} \quad \text{mod 16} \quad (5.33)$$

where use is made of De Morgan's law. Note that the wired-AND has led to an implementation of the AOI two-level logic (Sec. 5-6). Because of the + sign in Eq. (5-33), the connection in Fig. 5-22 is often incorrectly referred to as a positive wired-OR.

Note that the wired-AND connection places the collector resistors in Fig. 5-22a in parallel. This reduction in resistance increases the power dissipation in the ON state. In order to avoid this condition *open-collector* gates ( $R_c$  omitted from Fig. 5-21) are available specifically for wired-AND applications. Of course, after the open-collector outputs of several gates are tied together, a passive pullup resistor  $R_c$  must be added externally.

## 5-12 OUTPUT STAGES

In the discussion of fan-out (Sec. 5-9), two dc (static) conditions are taken into account; namely, the output transistor must saturate when loaded by  $N$  gates.

Sec. 5-12

and the current rating of this sink transistor must not be exceeded. Another (dynamic) condition is now considered.

At the output terminal of the DTL or TTL gate there is a capacitive load  $C_L$ , consisting of the capacitances of the reverse-biased diodes of the fan-out gates and any stray wiring capacitance. If the collector-circuit resistor of the inverter is  $R_c$  (called a *passive pull-up*), then, when the output changes from the low to the high state, the output transistor is cut off and the capacitance charges exponentially from  $V_{CE(sat)}$  to  $V_{CC}$ . The time constant  $R_c C_L$  of this waveform may introduce a prohibitively long delay time into the operation of these gates.

The output delay may be reduced by decreasing  $R_c$ , but this will increase the power dissipation when the output is in its low state and the voltage across  $R_c$  is  $V_{CC} - V_{CE(sat)}$ . A better solution to this problem is indicated in Fig. 5-23, where a transistor acts as an *active pull-up* circuit, replacing the passive pull-up resistance  $R_c$ . This output configuration is called a *totem-pole* amplifier because the transistor  $Q4$  "sits" upon  $Q3$ . It is also referred to as a power-driver, or power-buffer, output stage.

The transistor  $Q2$  acts as a *phase splitter*, since the emitter voltage is out of phase with the collector voltage (for an increase in base current, the emitter voltage increases and the collector voltage decreases). We now explain the operation of this driver circuit in detail, with reference to the TTL gate of Fig. 5-23.

The output is in the low-voltage state when  $Q2$  and  $Q3$  are driven into saturation. For this state we should like  $Q4$  to be OFF. Is it? Note that the collector voltage  $V_{CO}$  of  $Q2$  with respect to ground  $N$  is given by

$$V_{CN2} \equiv V_{CE2(\text{cap})} + V_{BE2(\text{cap})} = 0.2 + 0.8 = 1.0 \text{ V} \quad (5-34)$$

Since the base of  $Q4$  is tied to the collector of  $Q2$ , then  $V_{BN4} = V_{CN2} = 1.0$  V. If the output diode  $DO$  were missing, the base-to-emitter voltage of  $Q4$

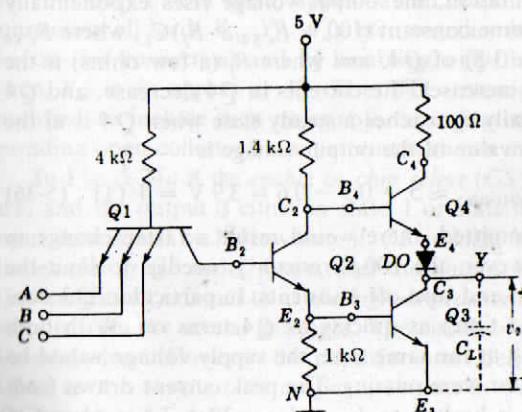


Figure 5-23 A TTL gate with a totem-pole output driver. This same active pullup circuit ( $Q4$ ,  $DO$ , and  $100\ \Omega$ ) may be used in place of  $R_C$  in the DTL gate of Fig. 5-19, if  $D2$  is replaced by transistor  $Q2$ .

would be

$$V_{BE4} = V_{BN4} - V_{CE3(\text{sat})} = 1.0 - 0.2 = 0.8 \text{ V}$$

which would put  $Q4$  into saturation. Under these circumstances the steady current through  $Q4$  would be

$$\frac{V_{CC} - V_{CE4(\text{sat})} - V_{CE3(\text{sat})}}{100} = \frac{5 - 0.2 - 0.2}{100} \text{ A} = 46 \text{ mA} \quad (5-35)$$

which is excessive and wasted current. The necessity for adding  $DO$  is now clear. With it in place, the sum of  $V_{BE4}$  and  $V_{DO}$  is 0.8 V. Hence both  $Q4$  and  $DO$  are at cutoff. In summary, if  $C_L$  is at the high voltage  $V(1)$  and the gate is excited,  $Q4$  and  $DO$  go OFF, and  $Q3$  conducts. Because of its large active-region current,  $Q3$  quickly discharges  $C_L$ , and as  $v_o$  approaches  $V(0)$ ,  $Q3$  enters saturation. The bottom transistor  $Q3$  of the totem pole is referred to as a *current sink*, which discharges  $C_L$ .

Assume now that with the output at  $V(0)$ , there is a change of state, because one of the inputs drops to its low state. Then  $Q2$  is turned OFF, which causes  $Q3$  to go to cutoff because  $V_{BE3}$  drops to zero. The output  $v_o$  remains momentarily at 0.2 V because the voltage across  $C_L$  cannot change instantaneously. Now  $Q4$  goes into saturation and  $DO$  conducts, as we can verify:

$$V_{BN4} = V_{BE4(\text{sat})} + V_{DO} + v_o = 0.8 + 0.7 + 0.2 = 1.7 \text{ V}$$

and the base and collector currents of  $Q4$  are

$$I_{B4} = \frac{V_{CC} - V_{BN4}}{1.4} = \frac{5 - 1.7}{1.4} = 2.36 \text{ mA}$$

$$I_{C4} = \frac{V_{CC} - V_{CE4(\text{sat})} - V_{DO} - v_o}{0.1} = \frac{5 - 0.2 - 0.7 - 0.2}{0.1} = 39.0 \text{ mA}$$

Hence, if  $h_{FE}$  exceeds  $h_{FE(\text{min})} = I_{C4}/I_{B4} = 39.0/2.36 = 16.5$ , then  $Q4$  is in saturation. The transistor  $Q4$  is referred to as a *source*, supplying current to  $C_L$ . As long as  $Q4$  remains in saturation, the output voltage rises exponentially toward  $V_{CC}$  with the very small time constant  $(100 + R_{CS4} + R_f)C_L$ , where  $R_{CS4}$  is the saturation resistance (Sec. 3-8) of  $Q4$ , and where  $R_f$  (a few ohms) is the diode forward resistance. As  $v_o$  increases, the currents in  $Q4$  decrease, and  $Q4$  comes out of saturation and finally  $v_o$  reaches a steady state when  $Q4$  is at the cutin condition. Hence the final value of the output voltage is

$$v_o = V_{CC} - V_{BE4(\text{cutin})} - V_{DO(\text{cutin})} \approx 5 - 0.5 - 0.6 = 3.9 \text{ V} = V(1) \quad (5-36)$$

If the 100- $\Omega$  resistor were omitted, there would result a faster change in output from  $V(0)$  to  $V(1)$ . However, the 100- $\Omega$  resistor is needed to limit the current spikes during the turn-on and turn-off transients. In particular,  $Q3$  does not turn off (because of storage time) as quickly as  $Q4$  turns on. With both totem-pole transistors conducting at the same time, the supply voltage would be short-circuited if the 100- $\Omega$  resistor were missing. The peak current drawn from the supply during the transient is limited to  $I_{C4} + I_{B4} = 39 + 2.4 \approx 41 \text{ mA}$  if

the 100- $\Omega$  resistor is used. These current spikes generate noise in the power-supply distribution system, and also result in increased power consumption at high frequencies.

### Alternative Output Stages

From the foregoing discussion it should be clear that the diode  $DO$  can be moved from the emitter into the base lead of  $Q4$ . This configuration is used by some manufacturers.

The diode in the base of  $Q4$  referred to in the preceding paragraph may be the base-to-emitter diode of an additional transistor, such as  $Q5$  in Prob. 5-51.

The manufacturer's specification sheet for the TTL gate is given in Appendix B-6.

### Wired Logic

It should be emphasized that the wired-AND connection must *not* be used with the totem-pole driver circuit. If the output from one gate is high while that from a second gate is low, and if these two outputs are tied together, we have exactly the situation just discussed in connection with transient current spikes. Hence, if the wired-AND were used, the power supply would deliver a *steady* current of 41 mA under these circumstances.

### Three-State Output<sup>4</sup>

It is often necessary to expand the capability of a digital system by combining a number of identical packages (Fig. 6-27). Consider such a design where the  $n$ th output  $Y_n$  corresponds to  $Y_{n1}$  from chip 1, to  $Y_{n2}$  from chip 2, to  $Y_{n3}$  from chip 3, etc. Depending upon the specified logic, it is required that either  $Y_{n1}$ ,  $Y_{n2}$ , or  $Y_{n3}$ , etc. (but only one of these) appear at an output  $Y_n$ . This result is obtained by connecting all leads  $Y_{n1}$ ,  $Y_{n2}$ ,  $Y_{n3}$ , etc., together (referred to as *wire OR-ing* or as the *OR-tied connection*) and by enabling only the  $i$ th chip during the interval when  $Y_{ni}$  is to appear at  $Y_n$ . The TTL totem-pole output stage (Fig. 5-23), modified to include such an enable, is indicated in Fig. 5-24a and the corresponding open-collector output circuit is shown in Fig. 5-24b.

In Fig. 5-24a if the *enable* or *chip select* ( $CS$ ) signal is low,  $D1$  and  $D2$  are OFF, and the output is either in state 1 or state 0, depending upon whether the input data are 0 or 1. However, if  $CS$  is high, then  $D1$  and  $D2$  are ON, these diodes clamp  $Q3$  and  $Q4$  OFF, and the output  $Y$  is effectively an open-circuit. This condition, referred to as the *high-impedance third state*, allows OR-ing of the outputs from the several packages. The circuit of Fig. 5-24b operates in a similar 3-state fashion. However, the manufacturers designate the configuration in Fig. 5-24a as the *tristate (TS) output* and that in Fig. 5-24b as the *open-collector (OC) output*.

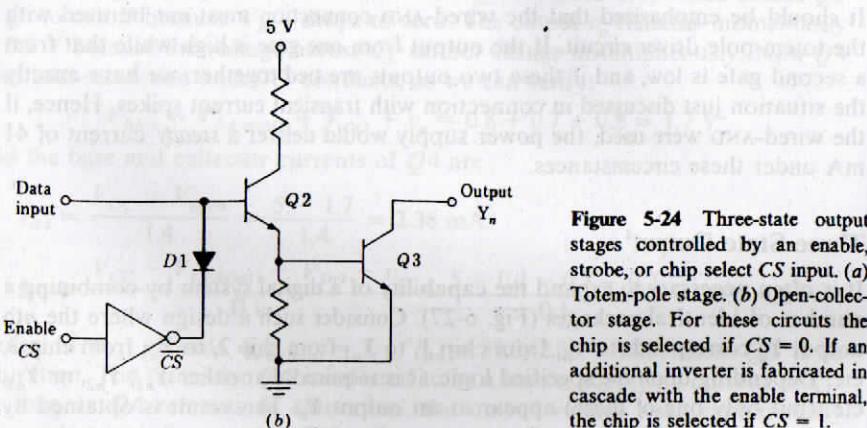
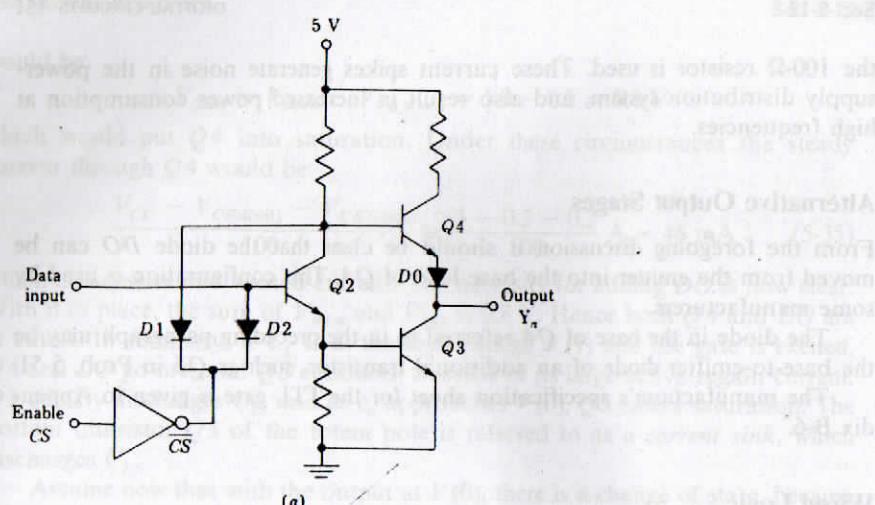


Figure 5-24 Three-state output stages controlled by an enable, strobe, or chip select CS input. (a) Totem-pole stage. (b) Open-collector stage. For these circuits the chip is selected if  $CS = 0$ . If an additional inverter is fabricated in cascade with the enable terminal, the chip is selected if  $CS = 1$ .

### 5-13 RESISTOR-TRANSISTOR LOGIC (RTL)<sup>1,2</sup> AND DIRECT-COUPLED TRANSISTOR LOGIC (DCTL)<sup>1,5</sup>

There are commercially available several other logic families, two of which are discussed in this section. The configuration for a *resistor-transistor logic* gate is indicated in Fig. 5-25a, which represents a three-input positive NOR gate with a fan-out of 5. If any input is high, the corresponding transistor is driven into saturation and the output is low,  $v_o = V_{CE(sat)} \approx 0.2 \text{ V} = V(0)$ . However, if all inputs are low, then all input transistors are cut off by  $V_y - V(0) = 0.5 - 0.2 = 0.3 \text{ V}$  and the output  $v_o$  is high. (Note the low noise margin.) The preceding two statements confirm that the gate performs positive NOR (or negative NAND) logic.

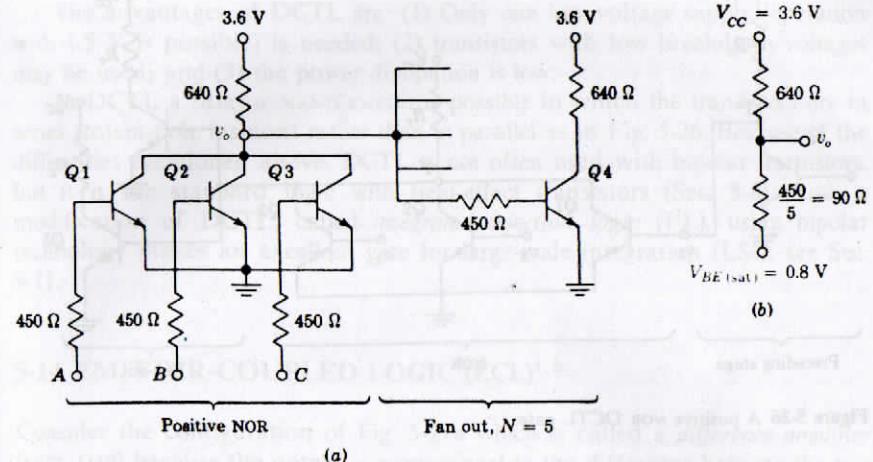


Figure 5-25 (a) An RTL positive NOR gate with a fan-in of 3 and a fan-out of 5. (b) The equivalent circuit from which to calculate  $v_o$  in the high state.

The value of  $v_o$  depends upon the fan-out. For example, if  $N = 5$ , then the output of the NOR gate is loaded by five  $450\text{-}\Omega$  resistors in parallel (or  $90\text{ }\Omega$ ), which is tied to  $V_{BE(sat)} \approx 0.8 \text{ V}$ , as shown in Fig. 5-25b. Under these circumstances (using superposition),

$$v_o = \frac{3.6 \times 90}{90 + 640} + \frac{0.8 \times 640}{90 + 640} = 1.14 \text{ V} \quad (5-37)$$

This voltage must be large enough so that the base current can drive each of the five transistors into saturation. Since

$$I_B = \frac{1.14 - 0.8}{0.45} = 0.755 \text{ mA} \quad I_C = \frac{3.6 - 0.2}{0.64} = 5.31 \text{ mA}$$

then the circuit will operate properly if  $h_{FE} > h_{FE(\min)} = 5.31/0.76 = 7.0$ .

### Direct-coupled Transistor Logic (DCTL)

This configuration is the same as RTL, except that the base resistors are omitted. In Fig. 5-26 the fan-in is 3 and the fan-out is 2.

To verify that the circuit implements positive NOR logic, consider first that all inputs are in the 0 state. Because this low voltage to an input (say, to  $Q1$ ) comes from a saturated transistor ( $Q'$ ) of a preceding state,

$$v_1 = V_{CE(sat)} = V(0)$$

Since this voltage is 0.2 V for a saturated silicon transistor, and since the cutin voltage  $V_y \approx 0.5 \text{ V}$ ,  $Q1$  will conduct very little (although the noise margin is only  $0.5 - 0.2 = 0.3 \text{ V}$  as it is with RTL logic). Since the current in  $Q1$  is almost

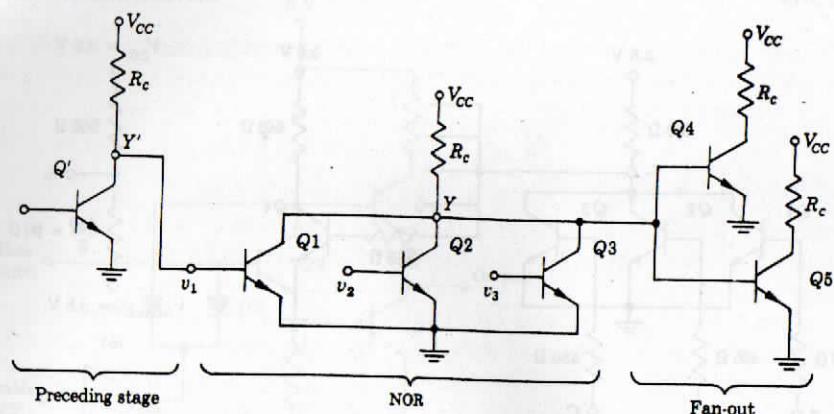


Figure 5-26 A positive NOR DCTL gate.

zero, the output  $Y$  tries to rise to  $V_{CC}$  and  $Q4$  and  $Q5$  go into saturation. Hence the output  $Y$  is clamped at

$$V_{BE(sat)} = V(1) \approx 0.8 \text{ V}$$

for silicon. Thus, with all inputs in the low state, the output is in the high state. Note that the high state is only 0.8 V, independent of  $V_{CC}$ .

Consider now that at least one input  $v_1$  is in the high state. Since  $Q1$  is fed from  $Q'$ ,  $Q'$  is cut off and  $Q1$  is driven into saturation. Under these circumstances the output  $Y$  is  $V_{CE(sat)} = V(0)$ . If more than one input is excited, the output will certainly be low. Hence we have confirmed that the NOR function is satisfied.

There are a number of difficulties with DCTL: (1) The reverse saturation current for all fan-in transistors adds in the common collector-circuit resistor  $R_c$ . At high enough temperatures the total  $I_{CBO}R_c$  drop may be large enough so that the output  $Y$  is too low to drive the fan-out transistors into saturation. (2) Because of the direct connection, the base current is almost equal to the collector current (for  $V_{CC} \gg V_{CE(sat)}$  and  $V_{CC} \gg V_{BE(sat)}$ ). With a transistor so heavily driven into saturation, very large stored base charge will result, with a corresponding detrimental effect on the switching speed. (3) Since the voltage levels are so low—the total output-voltage step is only of the order of 0.6 V for silicon—then spurious (noise) spikes can be troublesome. (4) The bases of the fan-out transistors are connected together. Since the input characteristics can never be identical, let us assume that  $Q4$  has a much lower  $V_{BE}$  for a given  $I_B$  than does  $Q5$ . Under these circumstances,  $Q4$  will “hog” most of the base current, and it is possible that  $Q5$  may not even be driven into saturation. Hence transistors suitable for DCTL must have very close control on uniformity of input characteristics, very low values of  $I_{CBO}$ , as large a differential as possible between  $V_{BE(sat)}$  and  $V_{CE(sat)}$ , a large  $h_{FE}$ , and a small storage time.

The advantages of DCTL are: (1) Only one low-voltage supply (operation with 1.5 V is possible) is needed; (2) transistors with low breakdown voltages may be used; and (3) the power dissipation is low.

In DCTL a NOR or NAND circuit is possible in which the transistors are in series (totem-pole fashion) rather than in parallel as in Fig. 5-26. Because of the difficulties mentioned above, DCTL is not often used with bipolar transistors, but it is the standard logic with field-effect transistors (Sec. 8-8). Also, a modification of DCTL, called *integrated injection logic* ( $I^2L$ ), using bipolar technology makes an excellent gate for large-scale integration (LSI); see Sec. 9-11.

### 5-14 Emitter-Coupled Logic (ECL)

Consider the configuration of Fig. 5-27a which is called a *difference amplifier* (DIFF AMP) because the output is proportional to the difference between the two input voltages  $v_1$  and  $v_2$ . This circuit is discussed in detail in Chap. 15 where its analog behavior is studied. This same configuration exhibits digital properties, and a logic family based upon this building block is called *emitter-coupled logic* (ECL) or *current-mode logic* (CML).

If  $v_1 = v_2$  then, from symmetry, the transistor currents are equal. However if  $v_1$  exceeds  $v_2$  by about 0.1 V, then it can be shown (Sec. 15-4) that  $Q1$  is ON and  $Q2$  is OFF. Conversely, if  $v_1$  is less than  $v_2$  by approximately 0.1 V, then  $Q1$  is OFF and  $Q2$  is ON. The transfer characteristic is indicated in Fig. 5-27b. We find the emitter current remains essentially constant and that this current is switched from transistor  $Q1$  to the other  $Q2$  as  $v_1$  varies from 0.1 V above

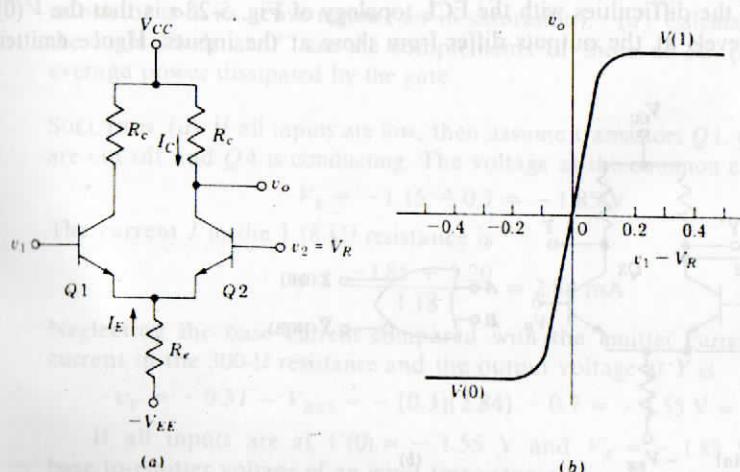


Figure 5-27 (a) A difference amplifier. (b) The transfer characteristic.

$v_2 = V_R$  = reference voltage to 0.1 V below  $V_R$ . Except for a very narrow range of input voltage  $v_1$ , the output  $v_o$  takes on only one of two possible values and, hence, behaves as a digital circuit. The two logic levels are easily found. If  $Q2$  is OFF,  $v_o = V_{CC} = V(1)$ . When  $Q2$  is ON, then the parameter values are chosen so that  $Q2$  remains in its active region. Then  $v_o = V_{CC} - I_C R_c = V(0)$ . If we neglect the base current then from Fig. 5-27a,

$$I_C = -I_E = \frac{V_R - V_{BE(\text{active})} + V_{EE}}{R_e} \quad (5-38)$$

(Transistor  $Q2$  will be in its active region if the collector junction  $V_{CB}$  is reverse-biased.) Since in the DIFF AMP neither transistor is allowed to go into saturation, then storage time is eliminated and, hence, the ECL is the fastest of all logic families (Table 5-3); a propagation delay (Sec. 5-15) as low as 0.5 ns per gate is possible.

A two-input OR (and also NOR) gate is drawn in Fig. 5-28a. This circuit is obtained from Fig. 5-27 by using two transistors in parallel at the input. Consider positive logic. If both  $A$  and  $B$  are low, then neither  $Q1$  nor  $Q2$  conducts whereas  $Q3$  is in its active region. Under these circumstances  $Y$  is low and  $Y'$  is high. If either  $A$  or  $B$  is high, then the emitter current switches to the input transistor the base of which is high, and the collector current of  $Q3$  drops approximately to zero. Hence  $Y$  goes high and  $Y'$  drops in voltage. Note that OR logic is performed at the output  $Y$  and NOR logic at  $Y'$ , so that  $Y' = \bar{Y}$ . The logic symbol for such an OR gate with both true and false outputs is indicated in Fig. 5-28b. The availability of complementary outputs is clearly an advantage to the logic design engineer since it avoids the necessity of adding gates simply as inverters. The basic Motorola ECL (MECL II) three-input gate is shown in Fig. 5-29.

One of the difficulties with the ECL topology of Fig. 5-28a is that the  $V(0)$  and  $V(1)$  levels at the outputs differ from those at the inputs. Hence emitter

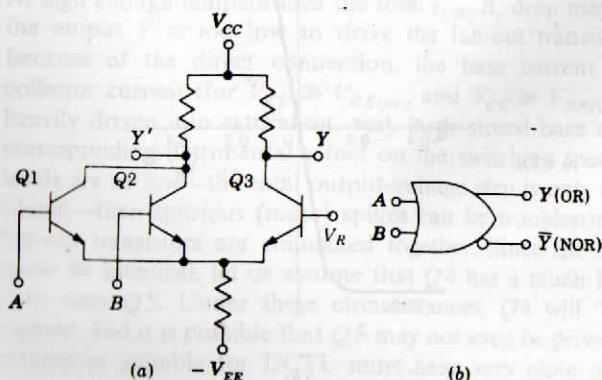


Figure 5-28 (a) DIFF AMP converted into a two-input emitter-coupled logic circuit. (b) The symbol for a two-input OR/NOR gate.

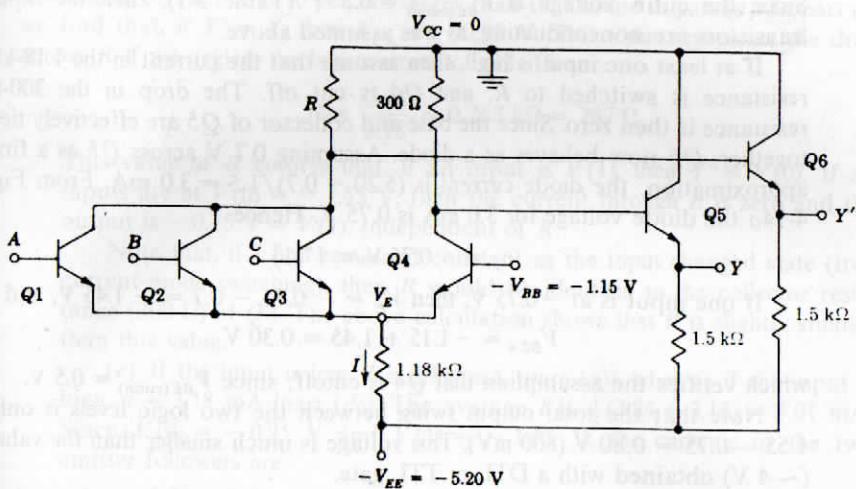


Figure 5-29 A three-input ECL OR/NOR gate, with no dc-level shift between input and output voltages.

followers  $Q5$  and  $Q6$  are used at the outputs to provide the proper dc-level shifts, as shown in Fig. 5-29. The reference voltage  $V_R = -V_{BB}$  is obtained from a temperature-compensated network (not indicated). The quantitative operation of the gate is given in the following illustrative problem.

**Example 5-7** (a) What are the logic levels at output  $Y$  of the ECL gate of Fig. 5-29? Assume a drop of 0.7 V between base and emitter of a conducting transistor. (b) Calculate the noise margins. (c) Verify that a conducting transistor is in its active region (not in saturation). (d) Calculate  $R$  so that the logic levels at  $Y'$  are the complements of those at  $Y$ . (e) Find the average power dissipated by the gate.

**SOLUTION** (a) If all inputs are low, then assume transistors  $Q1$ ,  $Q2$ , and  $Q3$  are cut off and  $Q4$  is conducting. The voltage at the common emitter is

$$V_E = -1.15 - 0.7 = -1.85 \text{ V}$$

The current  $I$  in the 1.18-kΩ resistance is

$$I = \frac{-1.85 + 5.20}{1.18} = 2.84 \text{ mA}$$

Neglecting the base current compared with the emitter current,  $I$  is the current in the 300-Ω resistance and the output voltage at  $Y$  is

$$v_Y = -0.31 - V_{BE5} = -(0.3)(2.84) - 0.7 = -1.55 \text{ V} = V(0)$$

If all inputs are at  $V(0) = -1.55 \text{ V}$  and  $V_E = -1.85 \text{ V}$ , then the base-to-emitter voltage of an input transistor is

$$V_{BE} = -1.55 + 1.85 = 0.30 \text{ V}$$

Since the cutin voltage is  $V_{BE(\text{cutin})} = 0.5$  V (Table 3-1), then the input transistors are nonconducting, as was assumed above.

If at least one input is high, then assume that the current in the 1.18-k $\Omega$  resistance is switched to  $R$ , and  $Q4$  is cut off. The drop in the 300- $\Omega$  resistance is then zero. Since the base and collector of  $Q5$  are effectively tied together,  $Q5$  now behaves as a diode. Assuming 0.7 V across  $Q5$  as a first approximation, the diode current is  $(5.20 - 0.7)/1.5 = 3.0$  mA. From Fig. 4-14a the diode voltage for 3.0 mA is 0.75 V. Hence

$$v_Y = -0.75 \text{ V} = V(1)$$

If one input is at -0.75 V, then  $V_E = -0.75 - 0.7 = -1.45$  V, and

$$V_{BE4} = -1.15 + 1.45 = 0.30 \text{ V}$$

which verifies the assumption that  $Q4$  is cutoff; since  $V_{BE(\text{cutin})} = 0.5$  V.

Note that the total output swing between the two logic levels is only  $1.55 - 0.75 = 0.80$  V (800 mV). This voltage is much smaller than the value ( $\sim 4$  V) obtained with a DTL or TTL gate.

(b) If all inputs are at  $V(0)$ , then the calculation in part (a) shows that an input transistor is within  $0.50 - 0.30 = 0.20$  V of cutin. Hence a positive noise spike of 0.20 V will cause the gate to malfunction.

If one input is at  $V(1)$ , then we find in part (a) that  $V_{BE4} = 0.30$  V. Hence a negative noise spike at the input of 0.20 V drops  $V_E$  by the same amount and brings  $V_{BE4}$  to 0.5 V, or to the edge of conduction. Note that the noise margins are quite small ( $\pm 200$  mV) and are equal in magnitude.

(c) From part (a) we have that, when  $Q4$  is conducting, its collector voltage with respect to ground is the drop in the 300- $\Omega$  resistance, or  $V_{C4} = -(0.3)(2.84) = -0.85$  V. Hence the collector junction voltage is

$$V_{CB4} = V_{C4} - V_{B4} = -0.85 + 1.15 = +0.30 \text{ V}$$

For an  $n-p-n$  transistor this represents a reverse bias, and  $Q4$  must be in its active region.

If any input, say  $A$ , is at  $V(1) = -0.75 \text{ V} = V_{B1}$ , then  $Q1$  is conducting and the output  $Y' = \bar{Y} = V(0) = -1.55$  V. The collector of  $Q1$  is more positive than  $V(0)$  by  $V_{BE6}$ , or

$$V_{C1} = -1.55 + 0.7 = -0.85 \text{ V}$$

and

$$V_{CB1} = V_{C1} - V_{B1} = -0.85 + 0.75 = -0.10 \text{ V}$$

For an  $n-p-n$  transistor this represents a forward bias, but one whose magnitude is less than the cutin voltage of 0.5 V. Therefore  $Q1$  is not in saturation; it is in its active region.

(d) If input  $A$  is at  $V(1)$ , then  $Q1$  conducts and  $Q4$  is OFF. Then

$$V_E = V(1) - V_{BE1} = -0.75 - 0.7 = -1.45 \text{ V}$$

$$I = \frac{V_E + V_{EE}}{1.18} = \frac{-1.45 + 5.20}{1.18} = 3.18 \text{ mA}$$

This value of  $I$  is about 10 percent larger than that found in part (a). In part (c) we find that, if  $Y' = \bar{Y}$ , then  $V_{C1} = -0.85$  V. This value represents the drop across  $R$  if we neglect the base current of  $Q1$ . Hence

$$R = \frac{0.85}{3.18} = 0.267 \text{ k}\Omega = 267 \Omega$$

This value of  $R$  ensures that, if an input is  $V(1)$ , then  $Y' = V(0)$ . If all inputs are at  $V(0) = -1.55$  V, then the current through  $R$  is zero and the output is  $-0.75 \text{ V} = V(1)$ , independent of  $R$ .

Note that, if  $I$  had remained constant as the input changed state (true current-mode switching), then  $R$  would be identical to the collector resistance (300  $\Omega$ ) of  $Q4$ . The above calculation shows that  $R$  is slightly smaller than this value.

(e) If the input is low,  $I = 2.84$  mA [part (a)], whereas if the input is high,  $I = 3.18$  mA [part (d)]. The average  $I$  is  $\frac{1}{2}(2.84 + 3.18) = 3.01$  mA. Since  $V(0) = -0.75$  V and  $V(1) = -1.55$  V, the currents in the two emitter followers are

$$\frac{5.20 - 0.75}{1.50} = 2.97 \text{ mA} \quad \text{and} \quad \frac{5.20 - 1.55}{1.50} = 2.43 \text{ mA}$$

The total power supply current drain is  $3.01 + 2.97 + 2.43 = 8.41$  mA and the power dissipation is  $(5.20)(8.41) = 43.7$  mW.

Since the current drain from the power supply varies very little as the input switches from one state to the other, power line spikes (of the type discussed in Sec. 5-11 for TTL gates) are virtually nonexistent.

### Fan-out

The input resistance can be considered infinite if all inputs are low so that all input transistors are cut off. If an input is high, then  $Q4$  is OFF, and the input resistance corresponds to a transistor with an emitter resistor  $R_e = 1.18$  k $\Omega$ , and from Eq. (11-45) a reasonable estimate is  $R_i \approx 100$  k $\Omega$ . The output resistance is that of an emitter follower (or a diode) and a reasonable value is  $R_o \approx 15$   $\Omega$ . Since the input resistance is very high and the output resistance is very low, a large fan-out is possible at low frequencies.

Because ECL gates are intended for high-speed operation, the dc fan-out is not important. Rather the fan-out is determined by the fact that capacitive loading slows down the gate operation. If  $C$  is the input capacitance per gate and  $N$  is the fan-out, then the total capacitance shunting the emitter-follower driver  $Q5$  is  $NC$ . This capacitance is charged rapidly through the low output resistance when  $Q5$  is ON. However, consider the situation where  $v_o = V(1)$  and the input to the emitter follower falls. Since the voltage across a capacitor cannot change instantaneously,  $Q5$  is cut off. Hence  $v_o$  falls toward  $-V_{EE}$  with a time constant  $1.5 \times 10^{-3} NC$  and  $N$  is determined by the maximum allowable transition time between states.

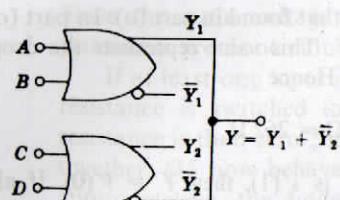


Figure 5-30 An implied-OR connection at the output of two ECL gates.

If the outputs of two or more ECL gates are tied together as in Fig. 5-30 then wired-OR logic (Sec. 5-11) is obtained (Prob. 5-57). Open-emitter gates are available for use in this application.

### Summary

The principal characteristics of the ECL gate are summarized below:

#### Advantages

1. Since the transistors do not saturate, then the highest speed of any logic family is available.
2. Complementary outputs are available.
3. Current switching spikes are not present in the power supply leads.
4. Outputs can be tied together to give the implied-OR function.
5. There is little degradation of parameters with variations in temperature.
6. The number of functions available is high.
7. Data transmission over long distances by means of balanced twisted-pair 50- $\Omega$  lines is possible.<sup>6</sup>

#### Disadvantages

1. A small voltage difference (800 mV) exists between the two logic levels and the noise margins are only  $\pm 200$  mV.
2. The power dissipation is high relative to the other logic families.
3. Level shifters are required for interfacing with other families.
4. Capacitive loading limits the fan-out.

## 5-15 COMPARISON OF LOGIC FAMILIES

An exhaustive comparison of each logic configuration is extremely difficult because we must take into account all the following characteristics: (1) Speed (propagation time delay); (2) noise immunity; (3) fan-in and fan-out capabilities; (4) power supply requirements; (5) power dissipation per gate; (6) operating temperature range; (7) number of functions available; and (8) cost. Items 1 and 7 require some explanation: all others have already been defined or are self-evident.

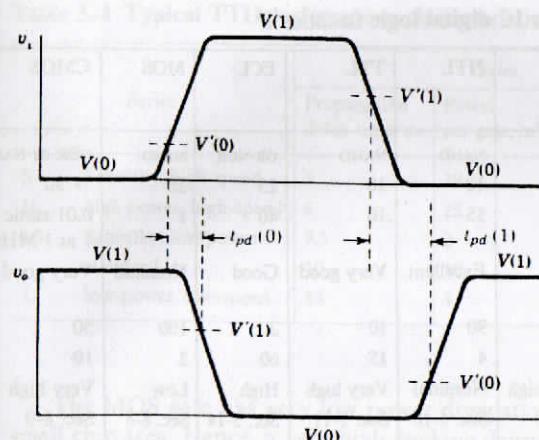


Figure 5-31 Pertaining to the definitions of the propagation delay times.

### Propagation Delay

As the input voltage to a positive NAND gate rises from  $V(0)$  toward  $V(1)$ , then at some *switching threshold voltage*  $V'(0)$  (Fig. 5-31), conditions within the gate are modified, so that a change of state of the output from  $V(1)$  to  $V(0)$  is initiated. Similarly, as the input falls from  $V(1)$  toward  $V(0)$ , then at some other *switching threshold voltage*  $V'(1)$ , the initiation of the change of state from  $V(0)$  to  $V(1)$  takes place. We now define (as in Fig. 5-31) the propagation delay on time  $t_{pd}(0)$  as the interval between the time when the input  $v_i$  reaches  $V(0)$  and the output falls to  $V'(1)$ . Also, the propagation delay off time  $t_{pd}(1)$  is defined as the interval between the time when the input equals  $V'(1)$  and the output rises to  $V(0)$ . Because of minority-carrier storage time,  $t_{pd}(1) > t_{pd}(0)$ . Hence the *propagation delay time*  $t_{pd}$  is usually defined as the average of these two times, or

$$t_{pd} = \frac{1}{2} [t_{pd}(0) + t_{pd}(1)] \quad (5-39)$$

In passing, we note that some authors arbitrarily assume the two threshold voltages to be equal:  $V'(0) = V'(1) = \frac{1}{2}[V(0) + V(1)]$ .

A reduction in propagation delay time usually means the use of smaller circuit resistances and, hence, an increase in power dissipation. Hence, a figure of merit often used in the comparison of logic gate is the product  $t_{pd} P_{av}$ , which is called the *delay-power* or *speed-power* product.

### Functions

The basic AND, OR, NAND, and NOR gates are combined in one integrated chip in various combinations to perform specific functions. The *building blocks* in Table 5-3 are used in the following chapters in connection with digital systems, which include binary adders, decoders, counters, shift registers, FLIP-FLOPS, etc.

Table 5-3 Comparison of the major IC digital logic families<sup>1,6</sup>

Parameter \ Logic	RTL	DTL	HTL	TTL	ECL	MOS	CMOS
Basic gate*	NOR	NAND	NAND	NAND	OR-NOR	NAND	NOR or NAND
Fan-out†	5	8	10	10	25	20	> 50
Power dissipated‡ per gate, mW	12	8	55	10	40	1	0.01 static
Noise immunity	Nominal	Good	Excellent	Very good	Good	Nominal	1 at 1 MHz
Propagation delay§ per gate, ns	12	30	90	10	2	100	Very good
Clock rate,¶ MHz	8	12	4	15	60	2	50
Number of functions	High	Fairly high	Nominal	Very high	High	Low	10
Reference	Sec. 5-13	Sec. 5-8	Sec. 5-10	Sec. 5-11	Sec. 5-14	Sec. 8-8	Sec. 8-9

\* Positive logic.

† Worst-case number of inputs that the gate can drive.

‡ Typical; affected by temperature and frequency of operation.

§ Typical for a nominal fan-out.

¶ Maximum frequency at which FLIP-FLOPS operate. The actual clock rate is from one-half to one-tenth the frequency listed.

### Logic Family Characteristics

A comparison of standard IC digital logic families is made in Table 5-3. In addition to the five types already discussed, *metal-oxide-semiconductor* (MOS) logic is included. Since MOS logic uses the field-effect transistor (FET), the discussion of these gates is postponed until Chap. 8, where the MOSFET is introduced.

The most popular family (the industry standard) is TTL. The voltage levels of DTL and TTL are compatible and, hence, these two gates may be intermixed in a logic system. However, TTL is rapidly replacing DTL because the former has better noise immunity, a smaller propagation delay, and more functions (different IC chips) are available than for the latter.

The RTL gate (the first logic family manufactured) is no longer used in new systems because its fan-out is low, the output depends upon the fan-out, the noise margins are small, and the output swing is low (not compatible with TTL). The brief discussion of RTL in Sec. 5-13 is included for historical reasons and because it leads to a convenient introduction of DCTL, which is used in MOS and CMOS (complementary MOS) logic. The overwhelming choice for lowest power is the CMOS family.

The ECL gate (which is nonsaturating) is the fastest logic gate, with a propagation delay of only about a nanosecond. However, the power dissipation is highest of all the other families (except for HTL), and the voltage swing is low (less than 1 V).

Table 5-4 Typical TTL performance characteristics<sup>7</sup>

Series	Gates			FLIP-FLOPS Clock-input frequency, MHz
	Propagation delay time, ns	Power per gate, mW	Delay-power product, pJ	
S Schottky, high-speed	3	19	57	dc to 125
H high-power, high-speed	6	22	132	dc to 50
LS Schottky, low-power	9.5	2	19	dc to 45
- standard	10	10	100	dc to 35
L low-power, low-speed	33	1	33	dc to 3

The MOS gate has very low power dissipation and it occupies an extremely small chip area. Hence, a very high packing density is possible, and MOS is used principally for very long shift registers and for large memories (Chap. 9). However, these devices have long propagation delays and, hence, are limited to systems operating at frequencies under 1 MHz.

The TTL entries in Table 5-3 are for the standard gate. The TTL family is also available in four other series emphasizing either high speed, low power, or both, as indicated in Table 5-4. These gates differ from one another in the numerical values for the resistances in Fig. 5-23 and in that some use *Schottky transistors* to increase speed by preventing saturation (Sec. 3-14 and Sec. 4-8).

From Texas Instruments, Inc., there is available the 74 series which may be used at temperatures between 0 and 70°C, and the 54 series which is valid over the military range from -55 to 125°C. A designation used with a TTL package could be TI-74LS10, which means that the IC may be operated only in the range 0 to 70°C, and that it is a low-power Schottky chip. The number ten identifies the function (a triple three-input NAND gate). In this book we shall abbreviate this designation to TI-10; it being understood that it may be of the 74 or 54 type and may belong to any one of the five series listed in Table 5-4. It should also be noted that many IC's are available with either totem-pole (Fig. 5-23), tristate, or open-collector outputs (Fig. 5-24).

The LS family has become the industry's favorite TTL. The LS has virtually replaced the L, and the S has replaced the H family. The highest speed is obtained with ECL and the lowest power with CMOS.

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## REVIEW QUESTIONS

- 5-1 Express the following decimal numbers in binary form: (a) 26; (b) 100; (c) 1024.
- 5-2 Define (a) *positive logic*; (b) *negative logic*.
- 5-3 Define an OR gate and give its truth table.
- 5-4 Draw a positive-diode OR gate and explain its operation.
- 5-5 Evaluate the following expressions: (a)  $A + 1$ ; (b)  $A + A$ ; (c)  $A + 0$ .
- 5-6 Define an AND gate and give its truth table.
- 5-7 Draw a positive-diode AND gate and explain its operation.
- 5-8 Evaluate the following: (a)  $A1$ ; (b)  $AA$ ; (c)  $A0$ ; (d)  $A + AB$ .
- 5-9 Define a NOT gate and give its truth table.
- 5-10 Draw a positive-logic NOT gate and explain its operation.
- 5-11 Evaluate the following expressions: (a)  $\bar{A}$ ; (b)  $\bar{A}\bar{A}$ ; (c)  $\bar{A} + A$ .
- 5-12 Define an INHIBITOR and give the truth table for  $AB\bar{S}$ .
- 5-13 Define an EXCLUSIVE OR and give its truth table.
- 5-14 Show two logic block diagrams for an EXCLUSIVE OR.
- 5-15 Verify that the following Boolean expressions represent an EXCLUSIVE OR: (a)  $AB + \bar{A}\bar{B}$ ; (b)  $(A + B)(\bar{A} + \bar{B})$ .
- 5-16 State the two forms of De Morgan's laws.
- 5-17 Show how to implement an AND with OR and NOT gates.
- 5-18 Show how to implement an OR with AND and NOT gates.
- 5-19 Define a NAND gate and give its truth table.
- 5-20 Draw a positive NAND gate with diodes and a transistor (DTL) and explain its operation.
- 5-21 Define a NOR gate and give its truth table.
- 5-22 Repeat Rev. 5-20 for a positive NOR gate.
- 5-23 Draw the circuit of an IC DTL gate and explain its operation.
- 5-24 Define (a) *fan-out*; (b) *fan-in*; (c) *standard load*; (d) *current sink*; (e) *current source*.
- 5-25 What logic is performed if the outputs of two DTL gates are connected together? Explain.
- 5-26 How does high-threshold logic (HTL) differ from DTL?
- 5-27 Draw the circuit of a TTL gate and explain its operation.

- 5-28 Draw a totem-pole output buffer with a TTL gate. Explain its operation.
- 5-29 Explain the function of a 3-state TTL gate.
- 5-30 Draw the circuit of an RTL gate and explain its operation for positive logic.
- 5-31 Repeat Rev. 5-30 for negative logic.
- 5-32 Draw a DCTL circuit and explain its operation.
- 5-33 List three advantages and three disadvantages of DCTL gates.
- 5-34 (a) Sketch a two-input OR (and also NOR) ECL gate.  
(b) What parameters determine the noise margin?  
(c) Why are the two collector resistors unequal?  
(d) Explain why power line spikes are virtually nonexistent.
- 5-35 List and discuss at least four advantages and four disadvantages of the ECL gate.
- 5-36 Define (a) *two threshold voltages*; (b) *propagation delay ON time*; (c) *propagation delay OFF time*; (d) *propagation delay time*.