CHAPTER
NINE

LARGE-SCALE INTEGRATION SYSTEMS

A chip containing over 1,000 components is referred to as an LSI and one with over 10,000 elements as a VLSI (very large-scale integration) system or a VHSIC (very high-speed integrated circuit) . There are reasonable expectations that in the 1990s chips with over one million gates will be available commercially! This chapter describes large-system chips which are primarily "memories" of various types. The commercial importance of these microelectronic chips is evident from the fact that the estimated world-wide semiconductor memory consumption in 1978 exceeded 900 million dollars.†

Included are discussions of very long (over 1,000 bits) MOS shift-register serial memories, mask-programmable MOS read-only memories (ROMs with over 65,000 bits), erasable-programmable read-only memories (EPROMs with over 16,000 bits), programmable logic arrays, read/write memories (RAMs with over 65,000 bits), charge-coupled devices (CCDs with over a 65,000-bit memory), microcomputers, and integrated injection logic (I^2L).

9-1 DYNAMIC MOS SHIFT REGISTERS[1-3]

Very long shift registers (involving hundreds of bits) are impractical if built from FLIP-FLOPS as discussed in Sec. 7-4. Too much power is wasted and they are uneconomical because an excessive area of silicon is required. An alternative approach is to construct an LSI shift-register stage by cascading two dynamic

† Source: DATAQUIST, Inc.

MOS† inverters. A bit is stored temporarily by charging the parasitic capacitance between gate and substrate of a MOSFET. A dynamic NOT circuit is first described and then two such gates will be expanded into a 1-bit dynamic storage cell.

A Dynamic MOS Inverter

The circuit of Fig. 9-1 shows a dynamic MOS inverter which requires a clock waveform ϕ for proper operation. Positive logic using n-channel enhancement MOSFETs is assumed with a 0 state of 0 V and a 1 state of $V_{DD} = 10$ V. The capacitor C represents the parasitic capacitance (~ 0.5 pF) between the gate and substrate of the following MOS, fed by V_o.

When $\phi = 0$ V, then the gates of $Q2$ and $Q3$ are at 0 V and both these enhancement NMOS are OFF. The supply voltage is disconnected from the circuit and delivers essentially no power. When the clock is at 10 V, both $Q2$ and $Q3$ are ON and inversion of V_i takes place. For example, if $V_i = 0$ V, $Q1$ is OFF, C charges to V_{DD}‡ through $Q2$ in series with $Q3$, and $V_o = 10$ V. If, however, $V_i = 10$ V, $Q1$ is ON, C discharges to ground through $Q3$ and $Q1$, and $V_o = 0$ V. Note that $Q3$ is a bidirectional switch: Terminal 2 acts as the source when C charges to the supply voltage, whereas terminal 1 becomes the source when C discharges to ground.

The important features of MOSFETs for this dynamic inverter (and also for the shift register) are:

1. The MOS is a bidirectional switch.
2. The very high input resistance permits temporary data storage on the small gate-to-substrate capacitance of a MOS device.
3. The load FET may be turned off by a clock pulse to reduce power dissipation.

The inverter discussed above is called a *ratioed inverter*. The name derives from the fact that when the input is high and the clock is high, transistors $Q1$ and $Q2$ form a voltage divider between V_{DD} and ground. Therefore the output voltage V_o depends on the ratio of the ON resistance of $Q1$ and the effective load resistance of $Q2$ (typically, $< 1 : 5$). This ratio is related to the physical size of $Q1$ and $Q2$ and is often referred to as the *aspect ratio*.

Two-Phase Ratioed Memory Cell

Cascading two of the dynamic inverters of Fig. 9-1 allows each bit of information which is stored on the capacitance C of the first NOT gate to be transferred to the following inverter by applying a second clock pulse out of phase with the

† The following terms are used synonomously in this chapter: MOSFET, MOS, FET, MOST, NMOS, and transistor.

‡ It is assumed throughout this chapter that the threshold voltage V_T is much smaller than the supply voltage V_{DD} and that $V_{os} = 0$ (Sec. 8-7).

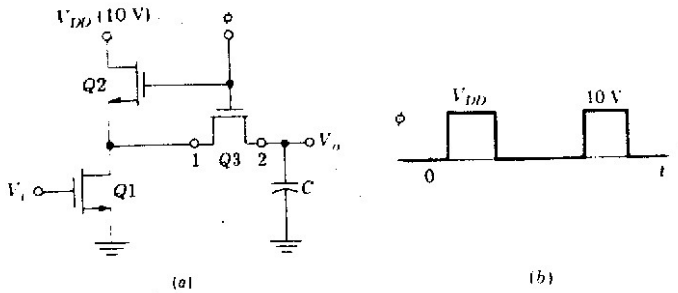

Figure 9-1 (*a*) Dynamic NMOS inverter. (*b*) Clock waveform ϕ.

first waveform. A typical MOS dynamic-shift-register stage is shown in Fig. 9-2*a* and the required two-phase clock waveforms are indicated in Fig. 9-2*b*. Each stage of the register requires six MOSFETs. The input V_i is the voltage on the gate capacitance C_1 of $Q1$, applied there by the previous stage (or by the input signal if this is the first stage of the shift register). When at $t = t_1$ the clock ϕ_1 goes positive (for NMOS devices), transistors $Q1$ and $Q2$ form an inverter and the bidirectional switch $Q3$ conducts. Hence, the complement of the level of C_1 is transferred to C_2. When ϕ_1 drops to 0 (at $t = t_2 +$), $Q2$ and $Q3$ are OFF and C_2 retains its charge as long as ϕ_1 remains at 0 V. However, at $t = t_3 +$, when $\phi_2 = V_{DD}$, then $Q4$ and $Q5$ act as an inverter and the switch $Q6$ is closed. Hence, the data stored on C_2 are inverted and deposited on C_3. The bit (a 1 or a 0) transferred to the output V_o is identical with that which was at the input V_i but delayed by an amount determined by the clock period. In other words the register stage in Fig. 9-2*a* is a 1-bit delay line. The combination $Q1Q2Q3$ can be called the *master inverter*, and $Q4Q5Q6$ the *slave section*. To retain data

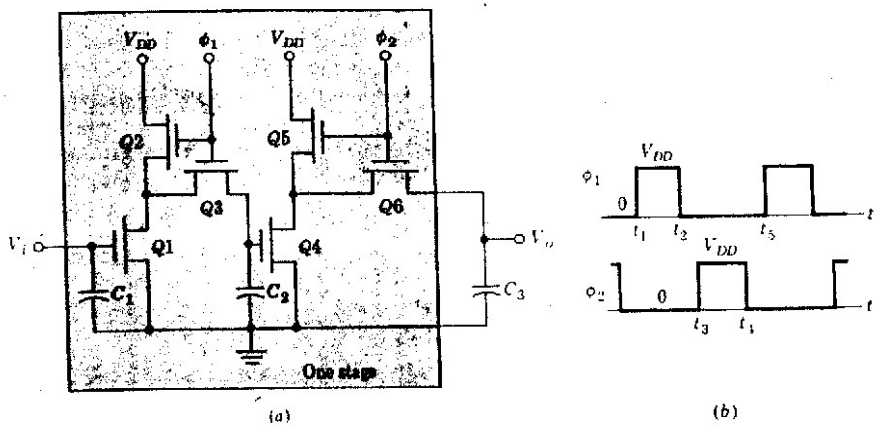

Figure 9-2 (*a*) A two-phase ratioed dynamic NMOS shift-register stage (six MOSFETs). (*b*) The two-phase clock waveforms ϕ_1 and ϕ_2.

stored in the register, the rate at which the data are clocked through the circuit must not fall below some minimum value. If the clock period is too long, the charge will leak of the parasitic capacitors and the data will be lost.

The load FETs in Fig. 9-2*a* are clocked because the gates are controlled by the clock waveform. Unclocked loads (the gates tied to fixed voltages) may also be used, but such circuits dissipate more power.

The Intel 2401 is a dual 1,024-bit dynamic shift register fabricated with NMOS. It uses a single 5-V supply and is TTL compatible. It operates at minimum data rate of 25 kHz and a maximum rate of 1 MHz, with power dissipation of 0.12 mW/bit at 1 MHz. It is interesting to note that this chip contains $2 \times 1{,}024 \times 6 = 12{,}288$ MOSFETs, exclusive of the control circuitry needed to convert it into a recirculating memory (Fig. 9-3).

Applications

Typical applications for MOS shift registers are as serial memories for calculators, cathode-ray tube displays, or communication equipment, as refresh or buffer memories, and as delay lines. A serial dynamic circulating shift-register memory is drawn in Fig. 9-3. The output of the register is returned to its input through an AND-OR combination as indicated. If the *write but not read* mode $W/\bar{R}$ is in the 1 state, the digital data at the *input* terminal are fed into the register. After a *clock* pulse cycle each bit is shifted to the right into the following stage, as explained in connection with Fig. 9-2. When the desired number of bits are entered sequentially into the register, the *recirculating* mode is commenced by changing $W/\bar{R}$ to the 0 state. In this mode further data are inhibited from entering the register and the bits stored in the memory are recirculated from the output back into the input of the shift register in synchronism with the clock waveform. Nondestructive reading of the data train is obtained at the output if the *read* input is excited by a logic 1.

If the register contains 1,024 stages, then this recirculating memory may store one 1,024-bit serial word. Consider now that four systems, S_0, S_1, S_2, and S_3, such as shown in Fig. 9-3, are used with *independent* data inputs and outputs. The $W/\bar{R}$ terminals are tied together as well as all the read terminals and the

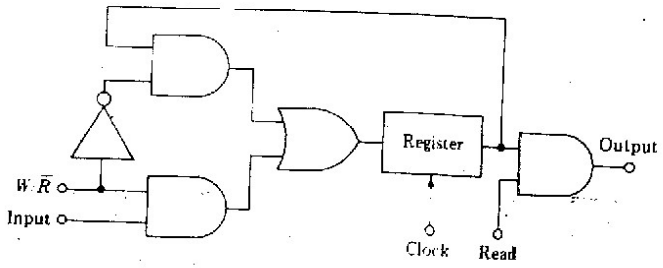

Figure 9-3 A recirculating shift register. ($W/\bar{R}$ is an abbreviation for *write but do not recirculate*). The AND, OR, and NOT gates are fabricated on the same chip with the register stages.

same clock synchronizes all systems. The resulting configuration is a serial memory which could be considered as storing 1,024 words, each containing 4 bits. All 4 bits in a particular word appear simultaneously: the LSB at the output of S_0 and the MSB at the output of S_3. One clock period later another 4-bit word can be read. To expand the system to n-bit words, it is necessary to use n-recirculating shift registers. If more words are required, then longer shift registers must be used.

If the desired use has been made of the data circulating in the memory of Fig. 9-3, then the $W/\bar{R}$ input is changed to a logic 1. This inhibits the bits from the last stage of the shift register from entering the first stage. In other words, the content of the memory is *erased* and new data may be simultaneously entered into the register.

Static MOS Shift Register

A "static" shift register is dc stable and can operate without a minimum clock rate. That is, it can store data indefinitely provided that power is supplied to the circuit. However, static shift-register cells are larger than the dynamic cells and consume more power. Consequently they are seldom used.

9-2 RATIOLESS SHIFT-REGISTER STAGES

It is pointed out in Sec. 9-1 that the load FET $Q2$ in Fig. 9-2 must have a much higher resistance than the driver $Q1$ in order for the low-state voltage V_{ON} to be close to zero. In Sec. 8-7 we emphasize that the FET resistance is proportional to L/w. Hence, $Q2$ must have a much larger channel length L and smaller width w than $Q1$. Consequently the inverter occupies more than the minimum possible area. Also, since the parasitic storage capacitance is charged through the load $Q2$ during a portion of the cycle, the high resistance of $Q2$ limits the speed of operation of the register. Both of these difficulties may be avoided by using a dynamic *ratioless* inverter, as indicated in Fig. 9-4*a* (where $Q1$ and $Q2$ may have identical geometries). Note that no power supply (dc) voltage is used in this inverter. The clock pulse ϕ (Fig. 9-1*b* for NMOS devices) must supply the required energy to this circuit and the power dissipation is proportional to the clocking frequency.

To understand the operation of the ratioless inverter consider first the case where $V_i = 0$. Then during the pulse the situation is as pictured in Fig. 9-4*b*. Since the gate voltage of $Q1$ is 0 and that of $Q2$ is V_{DD}, then (for NMOS enhancement devices) $Q1$ is OFF and $Q2$ is ON. Therefore C charges through $Q2$ to V_{DD}. At the end of the pulse ϕ falls to 0 and both MOSFETs remain OFF. Hence, with $V_i = 0$ (logic 0), the output $V_o = V_{DD}$ (logic 1) and an inversion has taken place.

Consider now that $V_i = V_{DD}$ and that $\phi = V_{DD}$ as shown in Fig. 9-4*c*. Both MOSFETs are ON and deliver current to C as indicated. Hence C is quickly

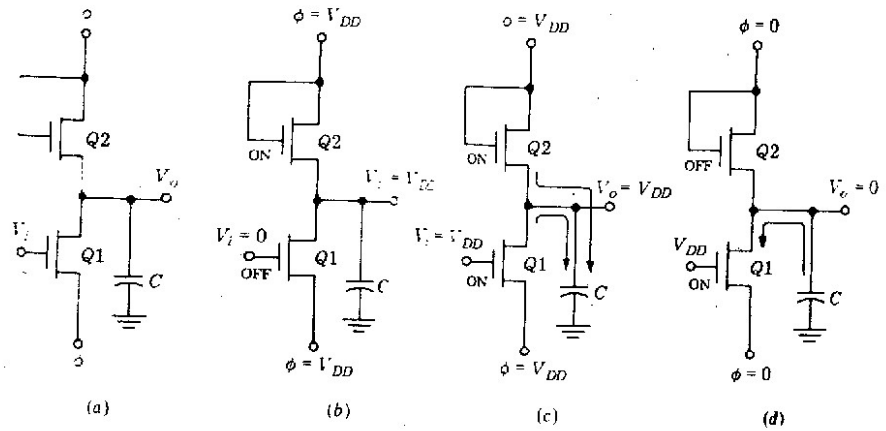

Figure 9-4 (*a*) A ratioless dynamic inverter using NMOS. (*b*) Input = logic 0 and $\phi = V_{DD}$. (*c*) Input = logic 1 and $\phi = V_{DD}$ (during pulse). (*d*) Input remains at logic 1 and $\phi = 0$ (after the pulse terminates).

charged to V_{DD}. Since $V_o = V_i = V_{DD}$, there is no inversion during the pulse. However, at the termination of the pulse when the clock voltage returns to 0, we have the situation depicted in Fig. 9-4*d*. Now the gate G_2 of $Q2$ is at 0 and $Q2$ is OFF, whereas G_1 of $Q1$ is at V_{DD} and $Q1$ is ON. Consequently C discharges to 0 V through $Q1$. Hence, shortly after the pulse ends, $V_o = 0$ while $V_i = V_{DD}$ indicating that a logical inversion has taken place.

Two-Phase Ratioless Dynamic Register Cell

If we cascade two inverters of the type shown in Fig. 9-4*a* through bidirectional transmission gates, the ratioless shift-register stage of Fig. 9-5 is obtained. The first inverter is powered by phase ϕ_1 and the second by phase ϕ_2, where these clock waveforms are drawn in Fig. 9-5*b*. At the beginning ($t = t_1 +$) of pulse ϕ_1 the switch $Q0$ closes and the voltage across C_0 (the input voltage to $Q1$) equals the input level V_i. By the inverter action described in connection with Fig. 9-4, the voltage across C_1 after the end of the pulse ϕ_1 (at $t = t_2 +$) corresponds to the complementary logic state of V_i. Since ϕ_1 is now at its low level, $Q0$ opens and V_i is retained on C_0 until the end of the period of ϕ_1 (at $t = t_5$).

At $t = t_3 +$ the second waveform ϕ_2 goes to its high level V_{DD} allowing transmission through $Q3$ and effectively placing C_1 and C_2 in parallel. If at $t = t_3 -$ the voltage on $C_1(C_2)$ is $V_1(V_2)$, then at $t = t_3 +$ the voltage V on C_2 (which must be the same as that on C_1) is found in Prob. 9-5 to be

$$V = \frac{C_1V_1 + C_2V_2}{C_1 + C_2} \qquad (9\text{-}1)$$

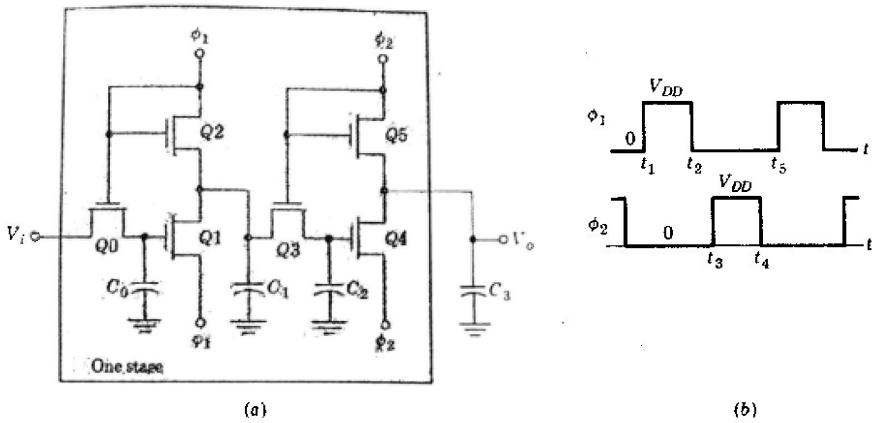

Figure 9-5 (*a*) A two-phase ratioless dynamic NMOS shift-register stage (six MOSFETs). (*b*) The two-phase clock waveforms ϕ_1 and ϕ_2.

If $C_1 \gg C_2$, note from Eq. (9-1) that $V \approx V_1$. In other words, pulse ϕ_2 causes the output voltage (across C_1) of the first inverter to appear at the input (across C_2) of the second NOT gate. Finally, by the inverter action described above, at the end of the pulse ϕ_2 (at $t = t_4 +$ and until $t = t_5$) the logic level V_o across C_3 is the complement of that across C_2, which, in turn, is the complement of that across C_0. Clearly, in one period of the clock the input level V_i has shifted through the stage to the output V_o, as it should in a 1-bit delay line or 1-bit shift register.

No dc power supply is used in Fig. 9-5, but the clocking waveforms must be capable of furnishing the heavy capacitive currents. Also in order to ensure that C_1 be much larger than C_2, additional area must be added to the chip for C_1. We can reduce the loading on the clock drivers by adding another transistor to each inverter as in Prob. 9-6. This modification results in an eight-MOSFET stage. A number of four-phase ratioless shift registers capable of operation at high speed are described in the literature.[1-3] Because of the large amount of chip area required for two-phase ratioless shift registers and the additional complications of four-phase clock drivers these systems are seldom used.

A Dynamic CMOS Shift-Register Stage

The static CMOS inverter indicated in Fig. 8-26 is discussed in Sec. 8-9. The CMOS transmission gate is shown in Fig. 8-28 and its operation is also explained in Sec. 8-9. We find in the foregoing discussion that interposing bidirectional transmission gates between inverters results in a dynamic shift register. Such a configuration using CMOS is indicated in Fig. 9-6. The transmission gates are labeled $T1$ and $T2$ and are controlled by complementary

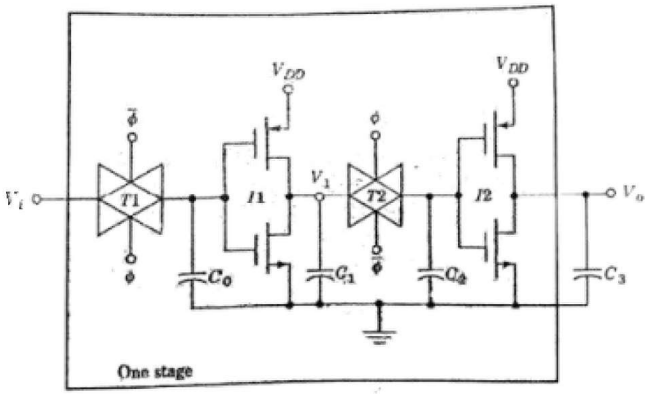

Figure 9-6 A dynamic CMOS shift-register cell.

clocks ϕ and $\bar{\phi}$. When $\phi = V_{DD}$ (corresponding to $C = V(1)$ in Fig. 8-28), $T1$ conducts whereas $T2$ acts as an open circuit. The CMOS inverters are marked $I1$ and $I2$.

The explanation of the operation of the register stage of Fig. 9-6 closely parallels that given in connection with Fig. 9-5. When $\phi = V_{DD}$ (logic 1), then $T1$ transmits and the input V_i appears across C_0. Because of the inverter action of $I1$, the complement of V_i appears across C_1 ($V_1 = \overline{V_i}$). On the next half cycle $\phi = 0$, $T1$ opens, C_0 retains the voltage V_i, and V_1 remains at the $\overline{V_i}$. Also when $\phi = 0$, $T2$ closes, putting C_2 in parallel with C_1, and $I2$ causes the voltage across C_3 to be the complement of that across C_2. Consequently at the end of a complete cycle $V_o = \overline{V_1} = V_i$ and we have demonstrated that this cell behaves as a 1-bit delay line or register.

The CMOS stage consists of eight MOSFETs (or four complementary pairs). The power dissipation is very low since there are no dc current paths; power is used only for the transient charging of capacitors. From the explanation of the circuit given in the foregoing, it should be clear that the output voltage does not depend on the ratio of the resistances of any of the devices and, hence, ratioless operation is involved.

Another type of shift register (the charge-coupled device, CCD) is discussed in Sec. 9-8.