CSE2209: Digital Electronics and Pulse Techniques

Course Conducted By:

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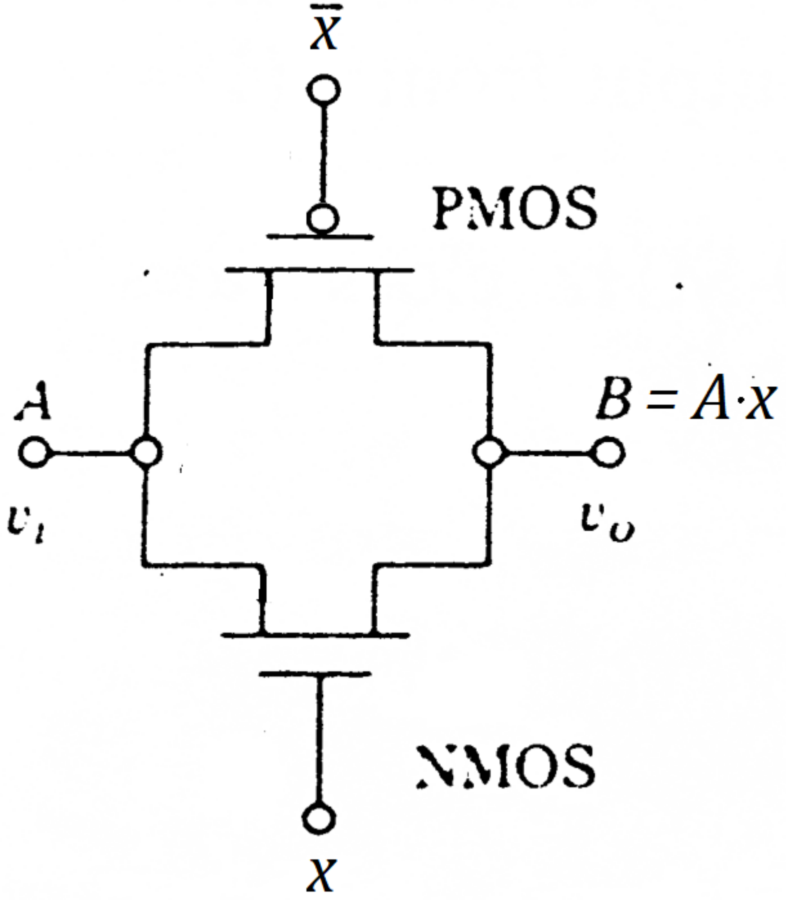
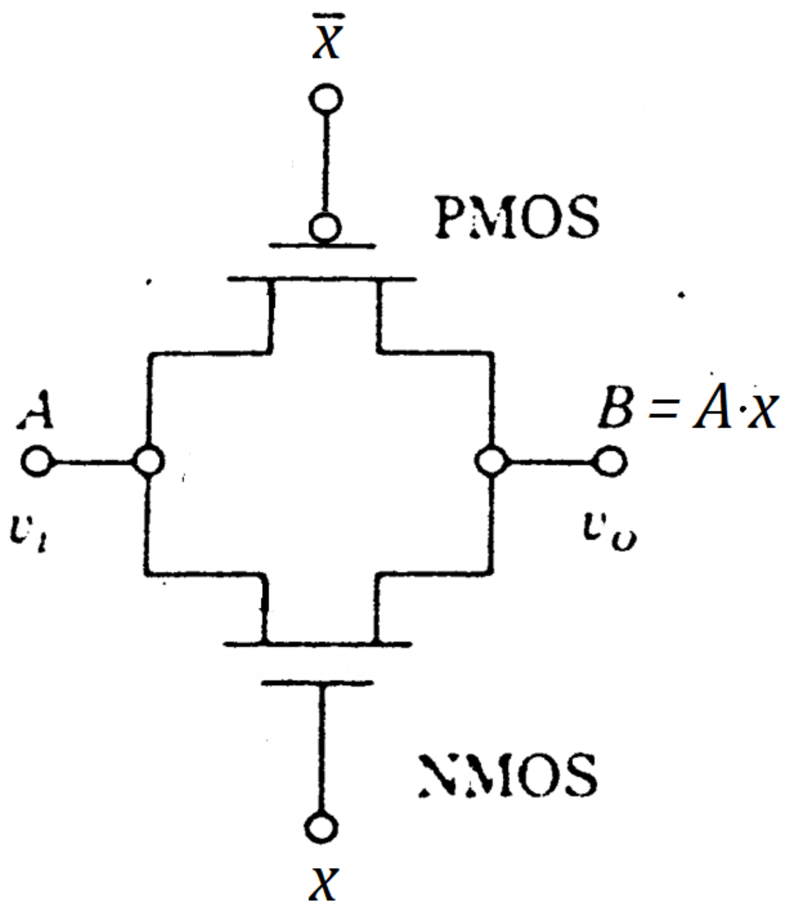
Transmission Gate

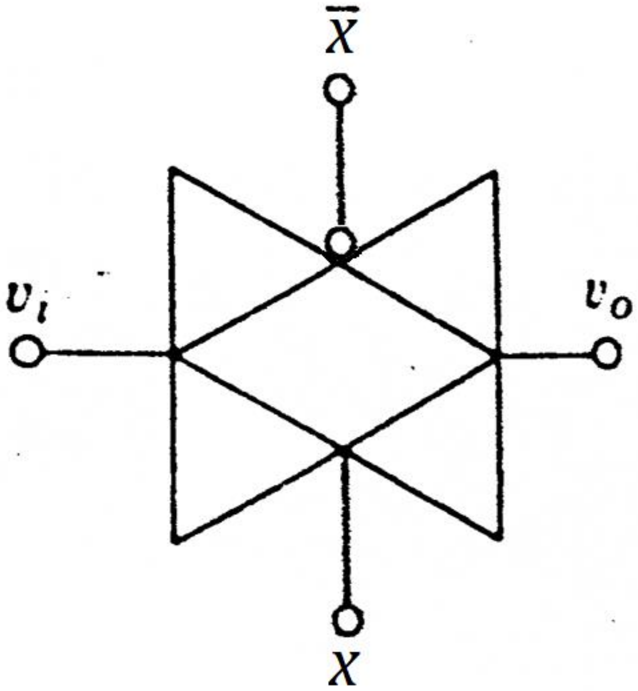
The structure of a CMOS transmission gate is shown in the figure. It consists of an NMOS in parallel with a PMOS such that the gates are controlled by the complementary voltages x applied to the NMOS, and $\bar{x}$ applied to the PMOS. The TG is designed to act as a voltage-controlled switch.

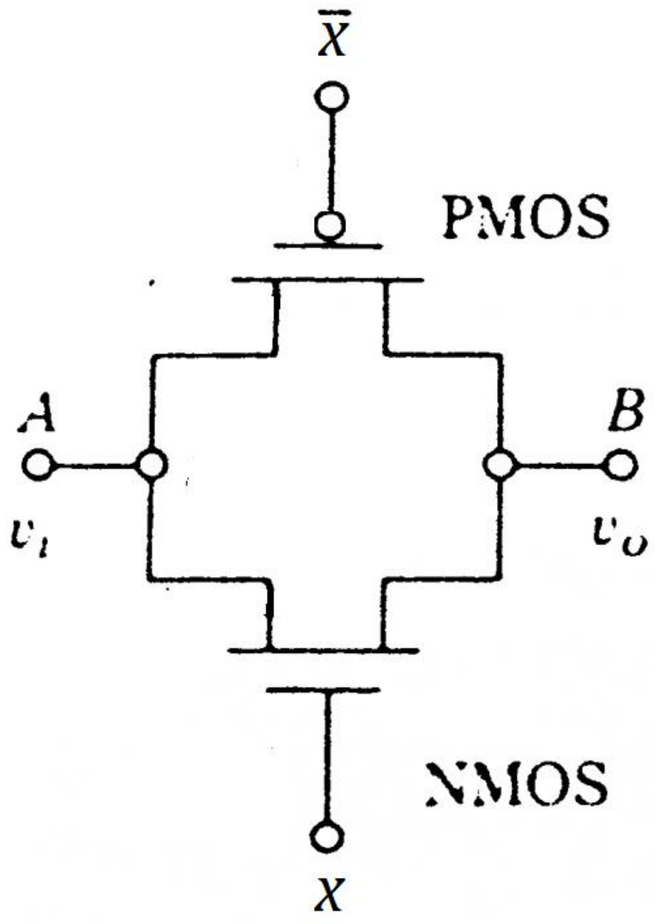


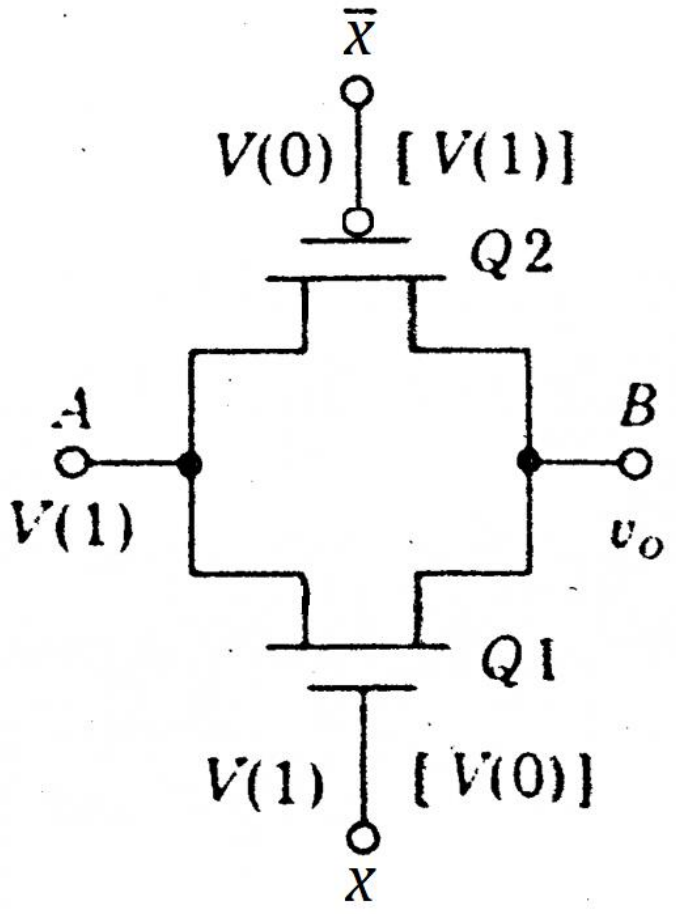
Transmission Gate

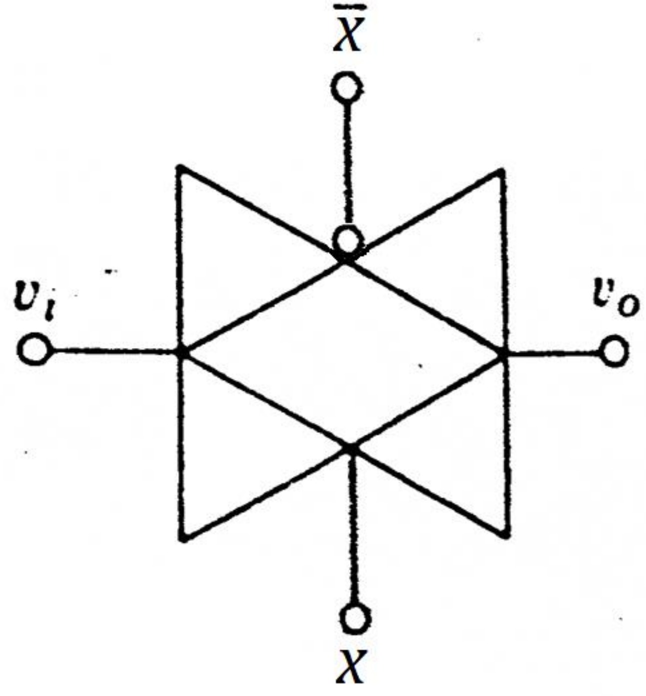
X	A	B (output)
1	0	0
1	1	1
0	0	H.I
0	1	H.I



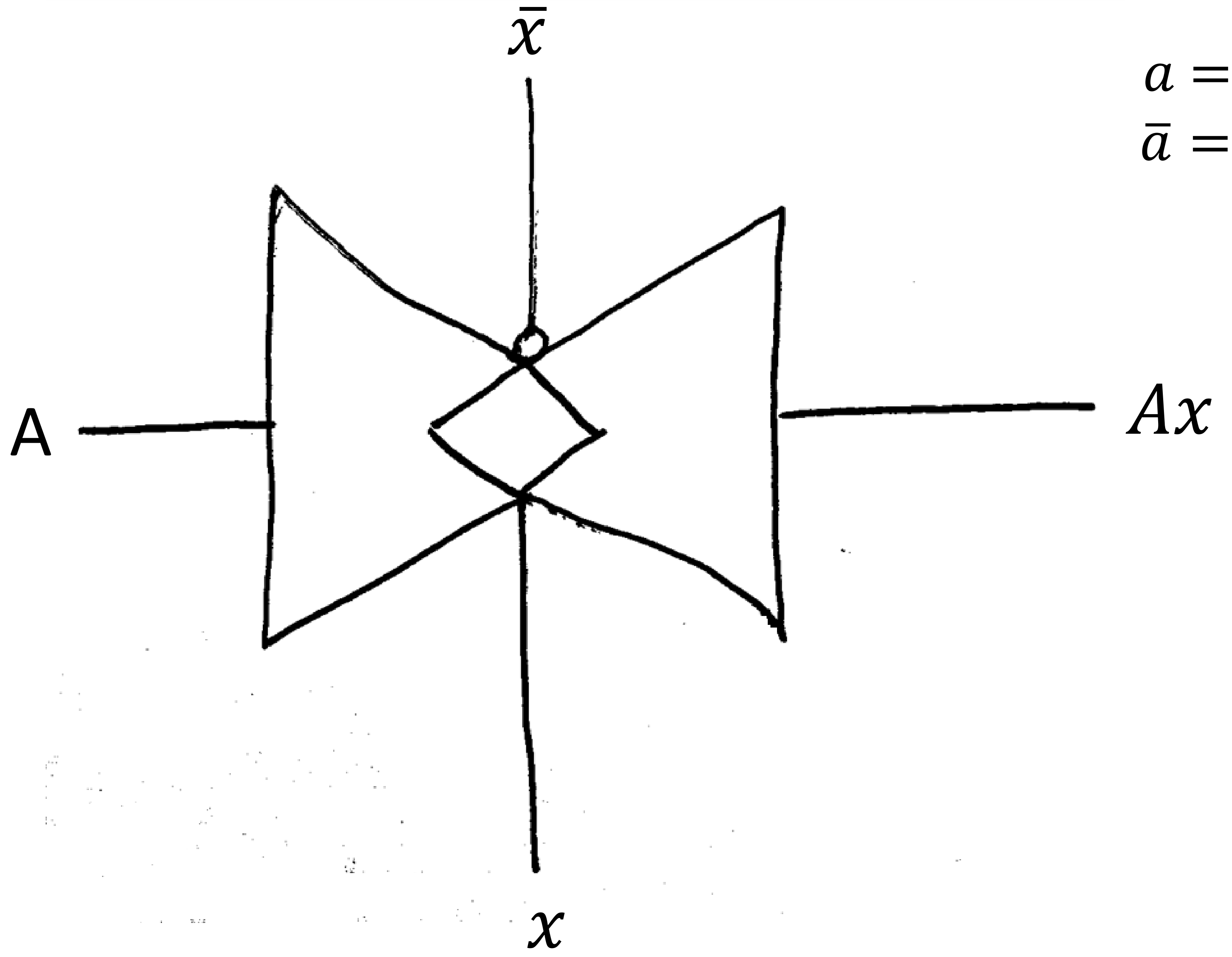



$\overline{X}$
PMOS
A
v_i
B
v_o
NMOS
X


$\overline{X}$
V(0)
[V(1)]
Q2
A
V(1)
B
v_o
Q1
V(1)
[V(0)]
X


$\overline{X}$
v_i
v_o
X

$a = 1$
$\bar{a} = 0$



OR using transmission gate

x	y	f
0	0	0
0	1	1
1	0	1
1	1	1

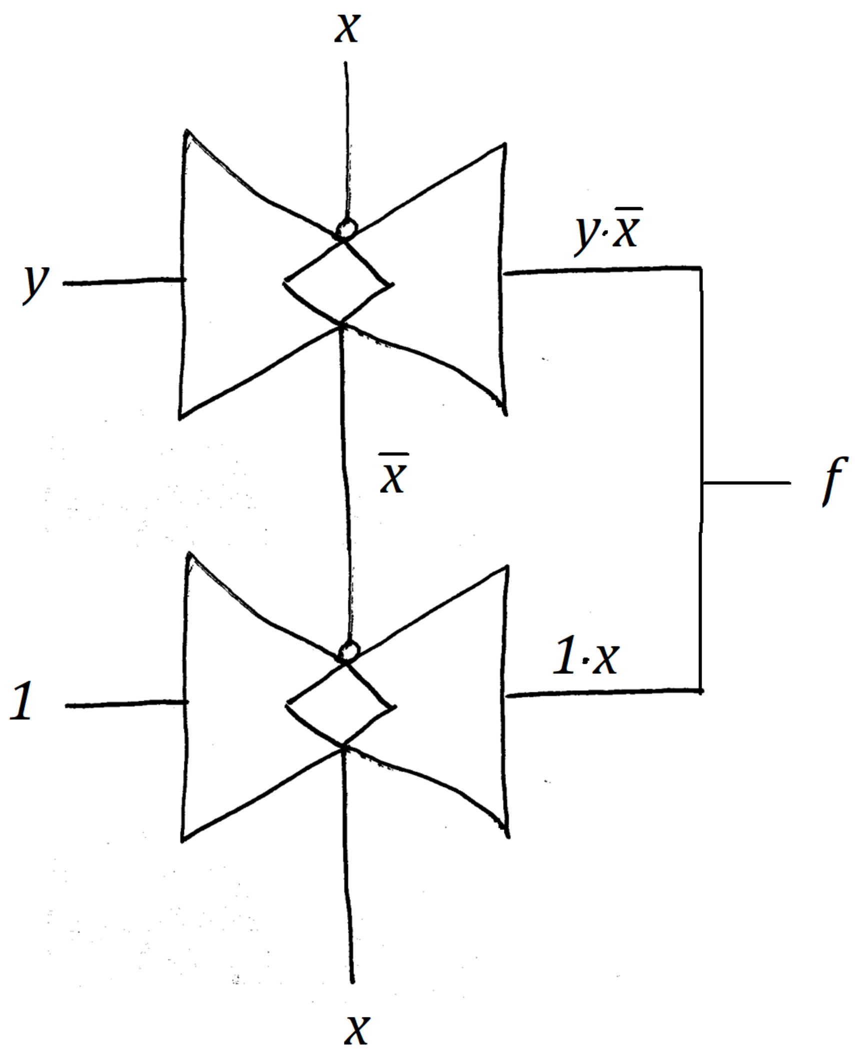
Let **x** be the control signal

f(x, y) = x+y

$= \bar{x}y + x\bar{y} + xy$

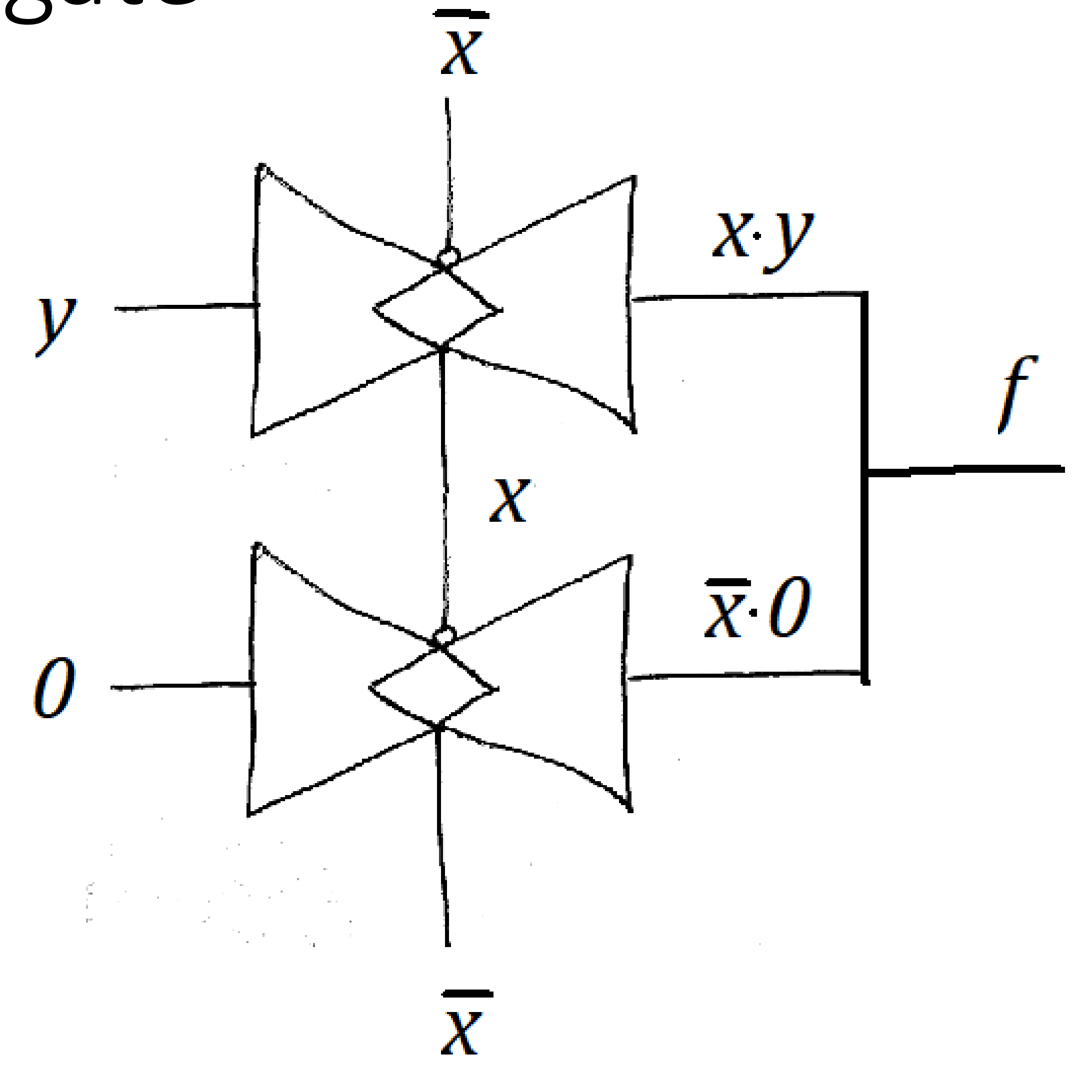
$= \bar{x}y +$ x$(y + \bar{y})$

$= \bar{x}y + x \cdot 1$ [inverse law]



AND using transmission gate

x	y	f
0	0	0
0	1	0
1	0	0
1	1	$\boxed{1}$

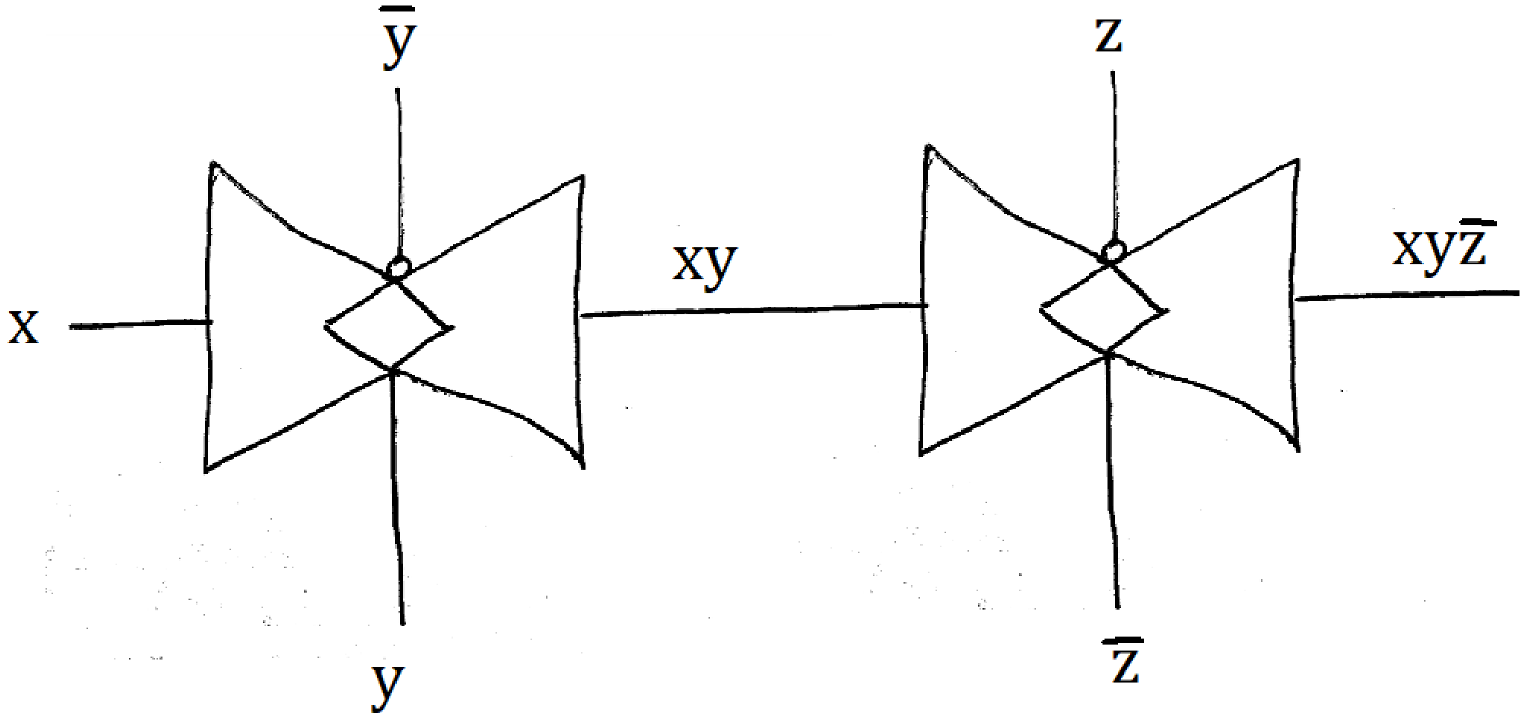


Let **x** be the control signal

$$f(x, y) = xy$$
$$= xy + \bar{x} \cdot 0 \text{ [null law]}$$

Implementing with Transmission Gate

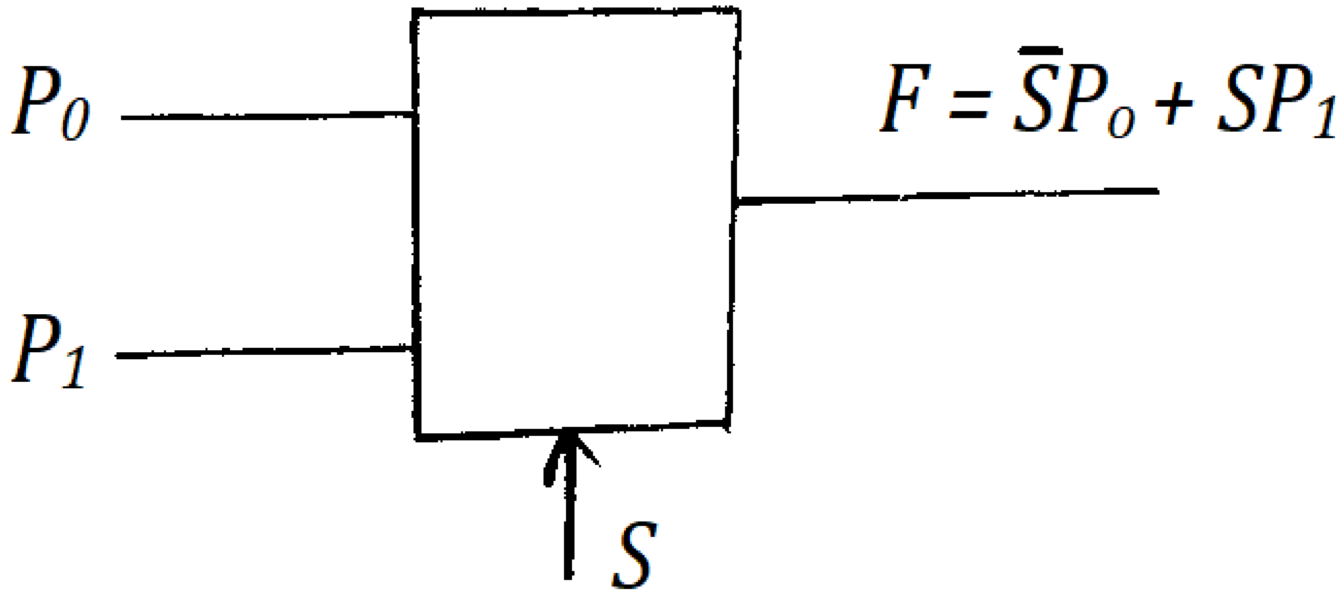
$$f = xy\bar{z}$$

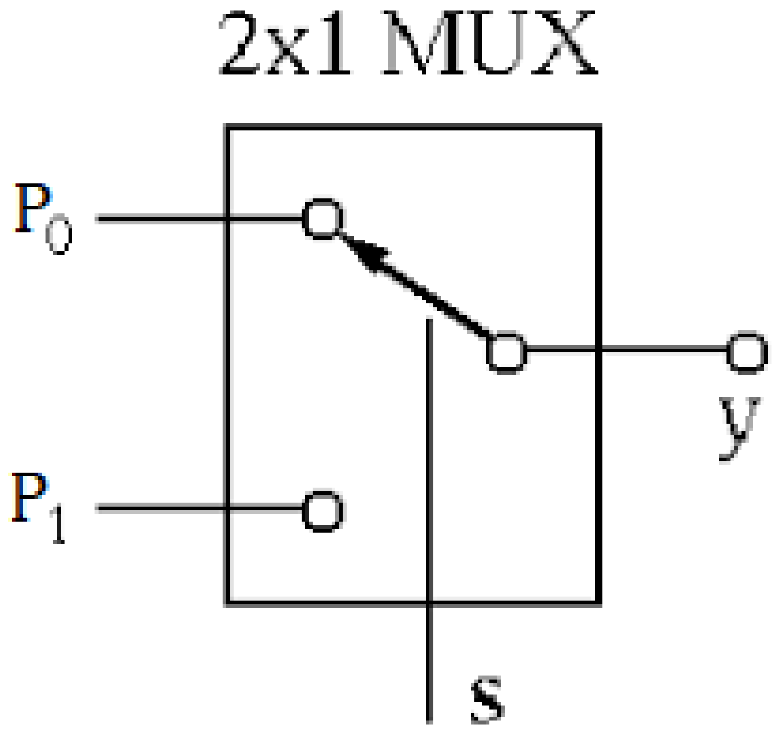


MUX Design Based on CMOS Transmission Gate

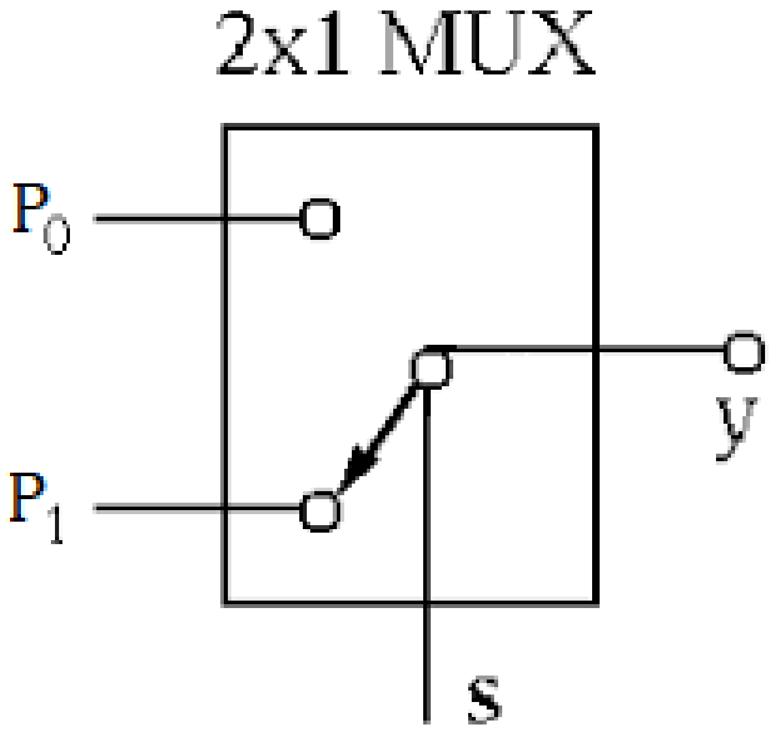
2 x 1 MUX

P_0 active, when S= 0
P_1 active, when S= 1





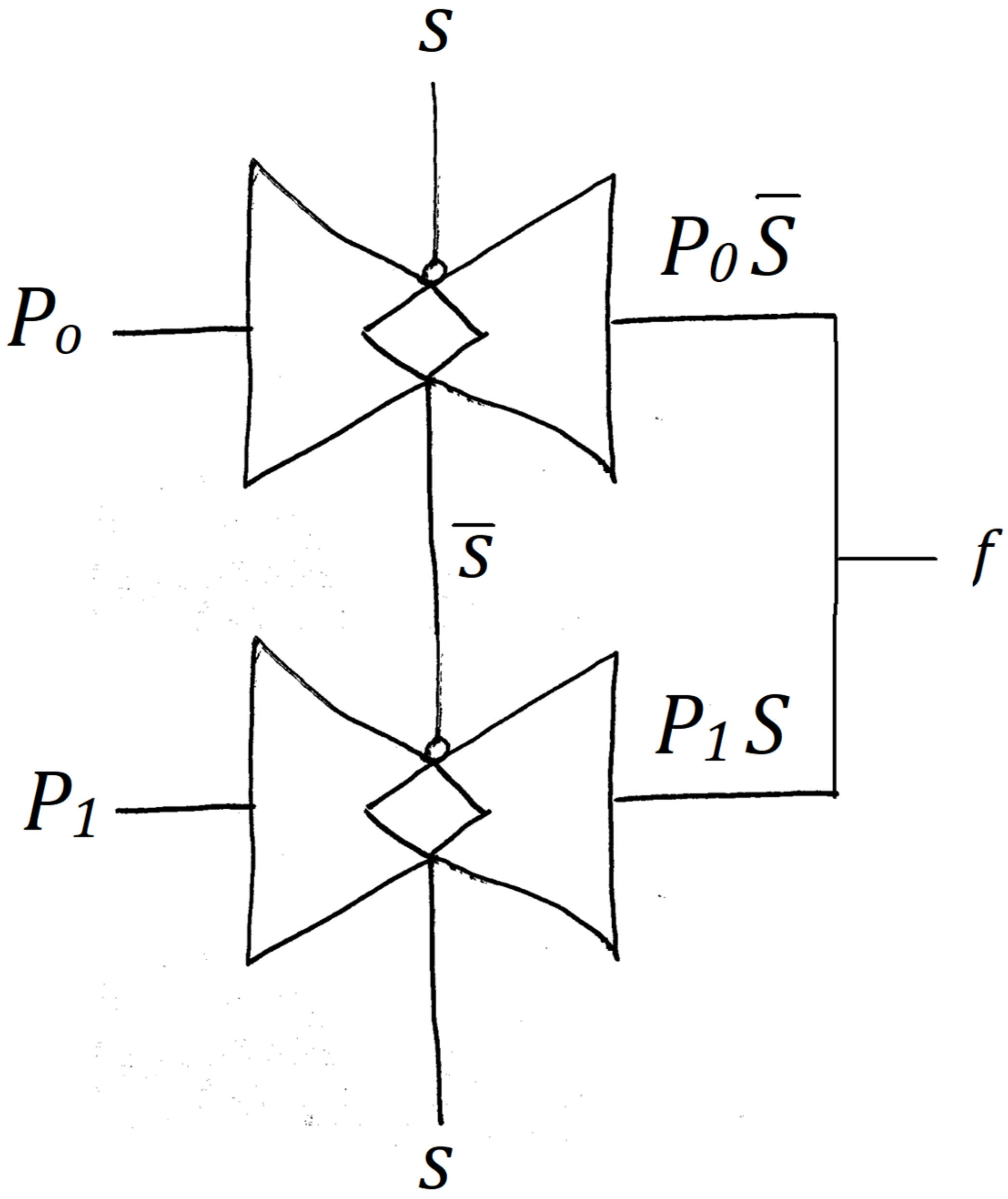
P_0 active, when S= 0



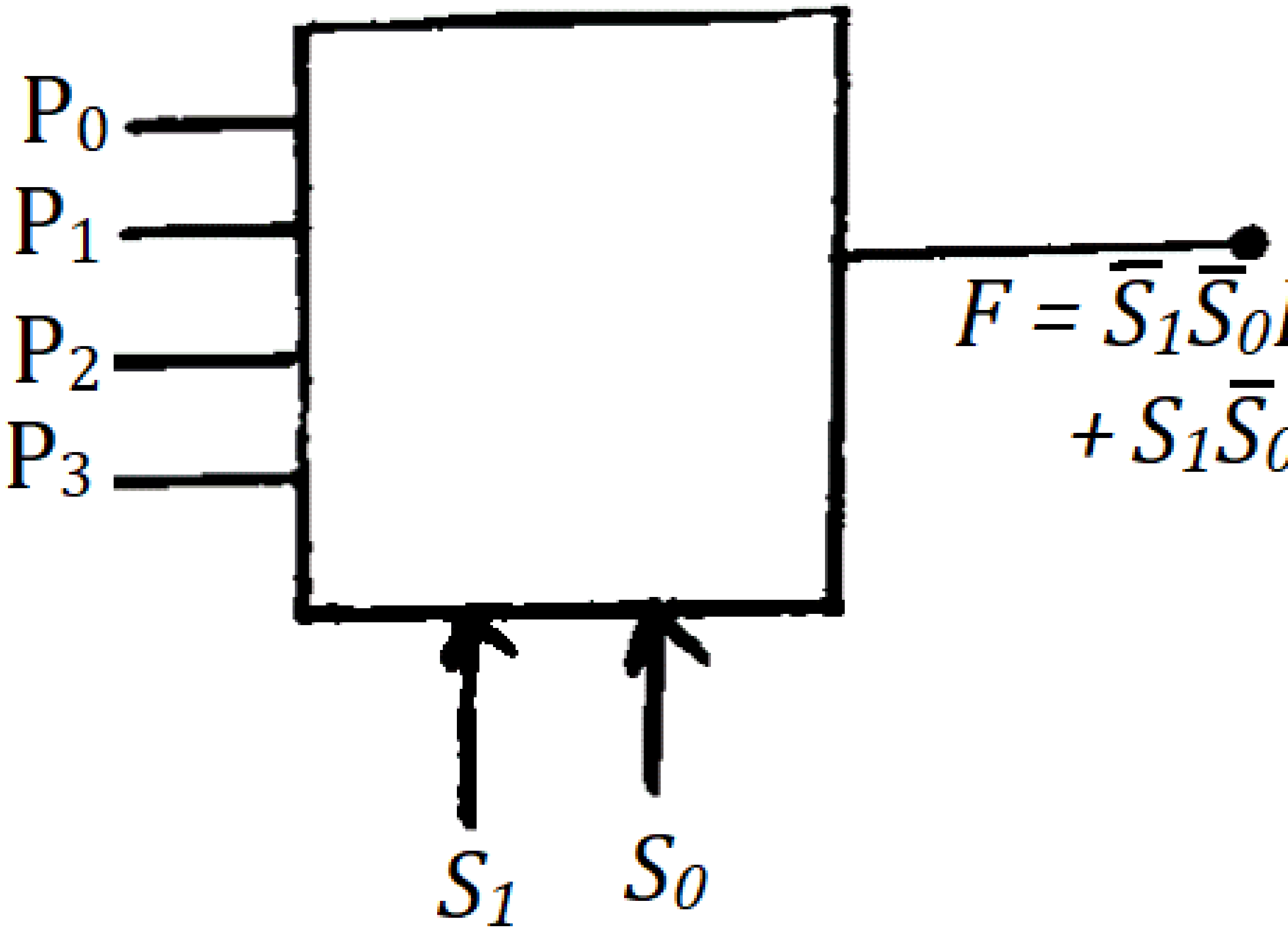
P_1 active, when S= 1

2 x 1 MUX

$$F = \bar{S}P_0 + SP_1$$



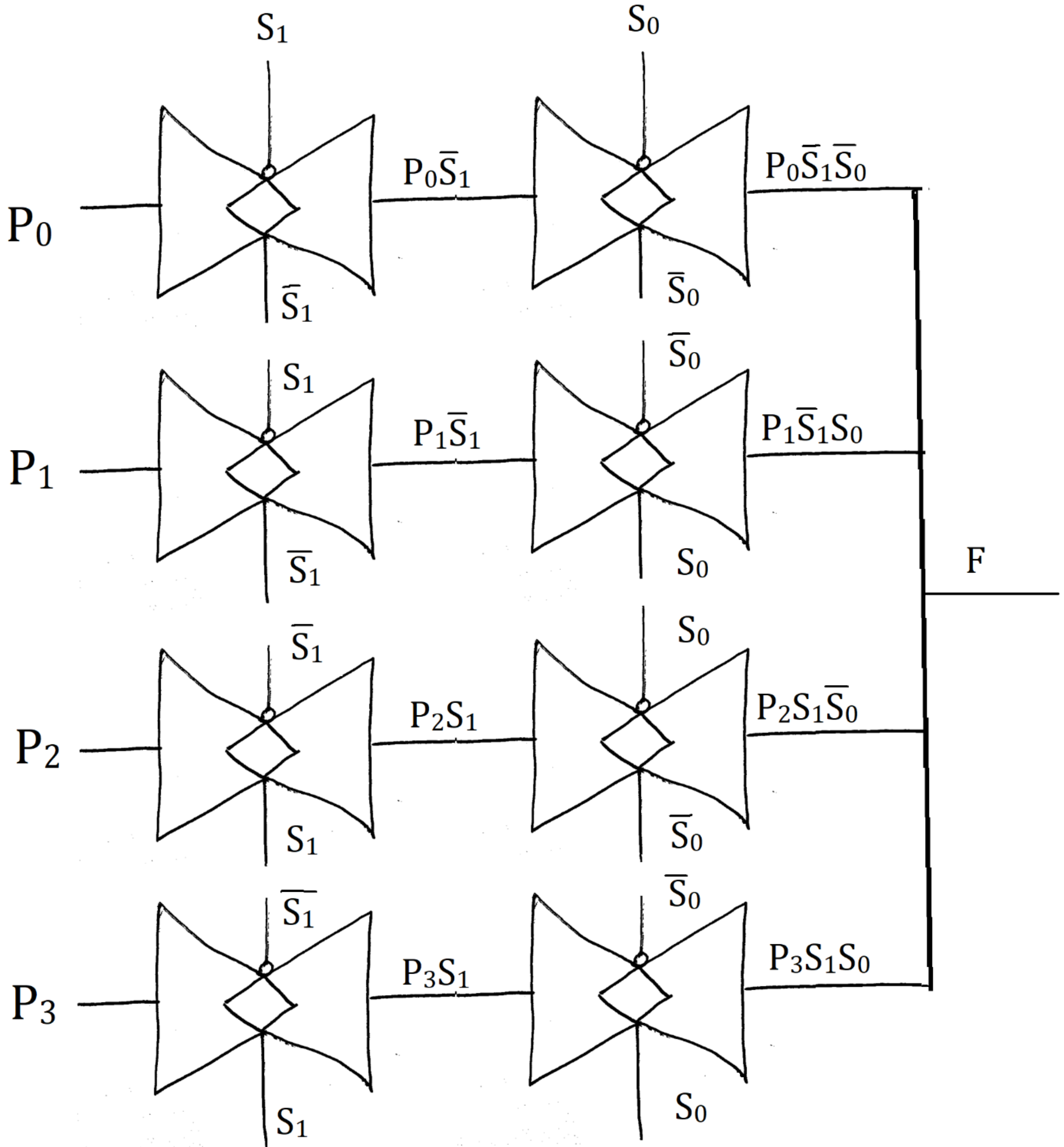
4 x 1 MUX



$$F = \bar{S}_1\bar{S}_0P_0 + \bar{S}_1S_0P_1 + S_1\bar{S}_0P_2 + S_1S_0P_3$$

4 x 1 MUX

$$F = P_0\overline{S_1}\,\overline{S_0} + P_1\overline{S_1}S_0 + P_2S_1\overline{S_0} + P_3S_1S_0$$



Laws of Boolean Algebra

Name	AND form	OR form
Identity law	$1A = A$	$0 + A = A$
Null law	$0A = 0$	$1 + A = 1$
Idempotent law	$AA = A$	$A + A = A$
Inverse law	$A\overline{A} = 0$	$A + \overline{A} = 1$
Commutative law	$AB = BA$	$A + B = B + A$
Associative law	$(AB)C = A(BC)$	$(A + B) + C = A + (B + C)$
Distributive law	$A + BC = (A + B)(A + C)$	$A(B + C) = AB + AC$
Absorption law	$A(A + B) = A$	$A + AB = A$
De Morgan's law	$\overline{AB} = \overline{A} + \overline{B}$	$\overline{A + B} = \overline{A}\overline{B}$

Expressing Boolean function with Mean terms

$F = a + b\bar{c}$

$= a.1.1 + 1.\, b\bar{c}$

$= a\,(b + \bar{b})(c + \bar{c}) + (a + \bar{a})b\bar{c}$

$= (ab + a\bar{b})\,(c + \bar{c}) + ab\bar{c} + \bar{a}b\bar{c}$

$= abc + ab\bar{c} + a\bar{b}c + a\bar{b}\,\bar{c} + ab\bar{c} + \bar{a}b\bar{c}$

$= abc + ab\bar{c} + a\bar{b}c + a\bar{b}\,\bar{c} + \bar{a}b\bar{c}$ [Idempotent Law (x+x =x)]

$= \Sigma(2,4,5,6,7)$

Implement F(a,b,c) = $\Sigma(2,4,5,6,7)$ using Transmission Gate

Truth Table for F(a,b,c) = $\Sigma(2,4,5,6,7)$

a	b	c	f
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

K-Map

Let b and c are the control signals.

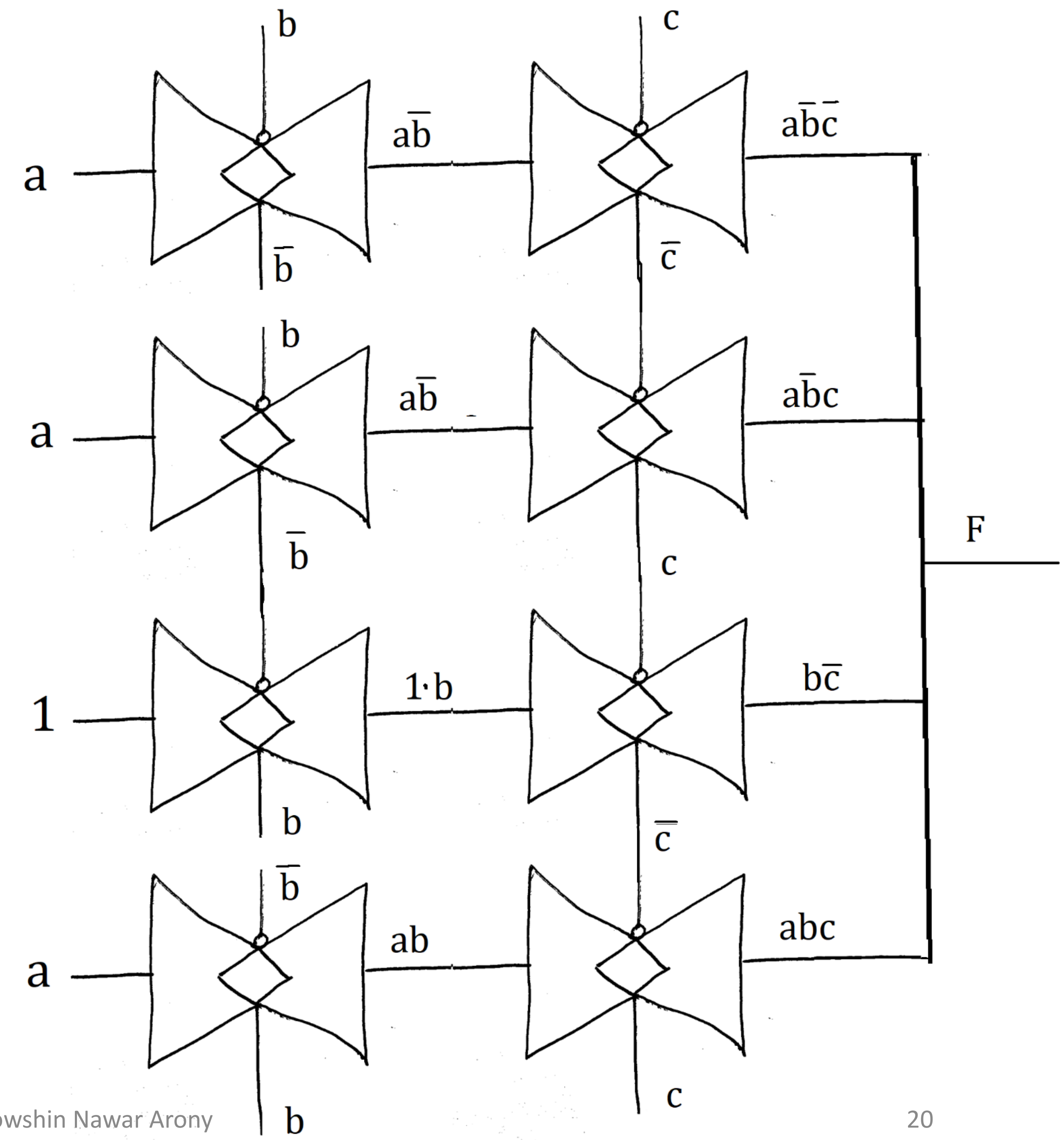
a \ bc	00	01	11	10
0	0	1	3	2
1	4	5	7	6
	a	a	a	1

$F(a,b,c) = \Sigma(2,4,5,6,7)$

$a\bar{b}\,\bar{c} + a\bar{b}c + b\bar{c} + abc$

Implement using Transmission Gate:

$f(a,b,c) = a\overline{b}\,\overline{c} + a\overline{b}c + b\overline{c} + abc$



2nd Approach

Let, b and c are the control signal

a	b	c	f
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

b	c	output
0	0	a
0	1	a
1	0	1
1	1	a

$$a\bar{b}\,\bar{c} + a\bar{b}c + b\bar{c} + abc$$

3rd Approach

Given, $f = a+b\overline{c}$

Let, bc are control signals.

$$f(a,b,c) = b\, f(a,1,c) + \bar{b}\, f(a,0,c)$$
$$= b.c.\, f(a,1,1) + b.\bar{c}.\, f(a,1,0) + \bar{b}.c.\, f(a,0,1) + \bar{b}.\bar{c}.\, f(a,0,0)$$
$$= b.c.\, a + b.\bar{c}.\, 1 + \bar{b}.c.\, a + \bar{b}.\bar{c}.a$$
$$= abc + b\overline{c} + a\overline{b}\, c + a\overline{b}\, \overline{c}$$

Here,

$f(a,1,1) = a+b\overline{c} = a + 1.\overline{1} = a + 1.0 = a + 0 = a$

$f(a,1,0) = a+b\overline{c} = a + 1.\overline{0} = a + 1.1 = a + 1 = 1$

$f(a,0,1) = a+b\overline{c} = a + 0.\overline{1} = a + 0.0 = a + 0 = a$

$f(a,0,0) = a+b\overline{c} = a + 0.\overline{0} = a + 0.1 = a + 0 = a$

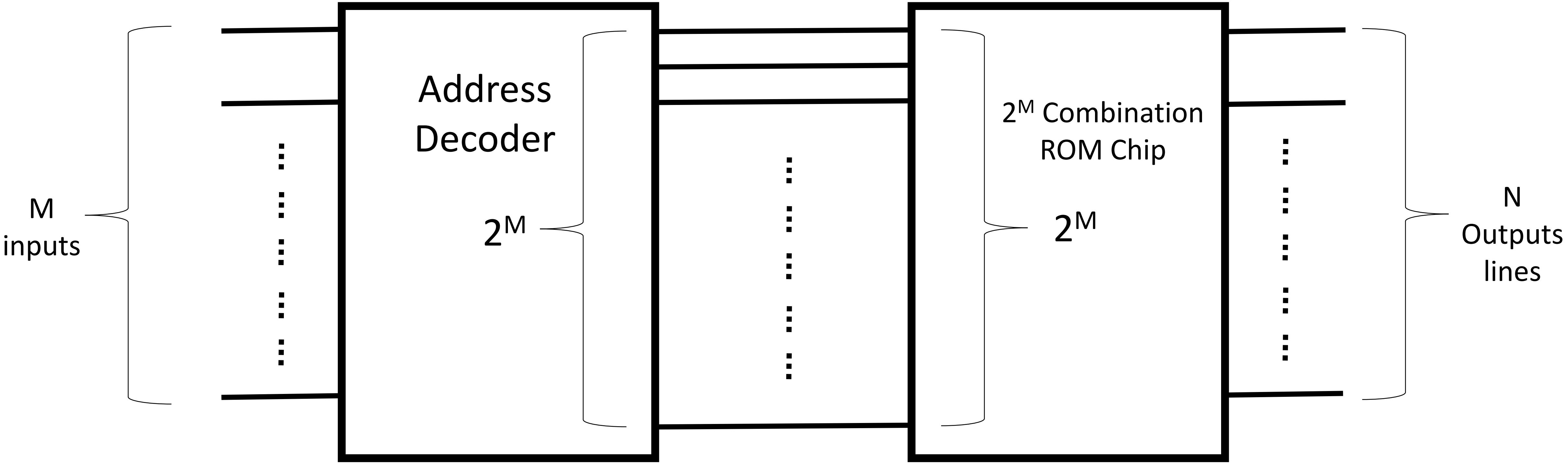
Implement using CMOS transmission gate, 2x1 or/and 4x1 MUX

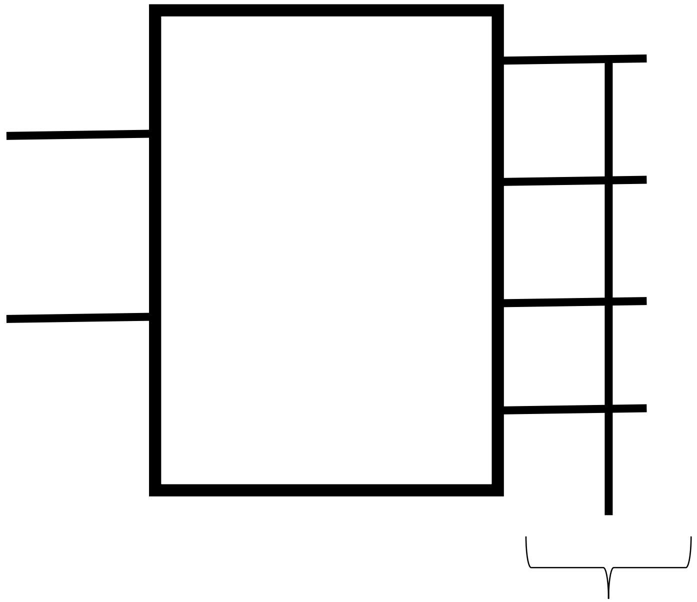
- F(a,b,c) = $\Sigma(0,2,4,6)$
- F(x,y,z) = xy + $\bar{z}$
- F(x,y,z) = xy + yz + zx
- F(a,b,c,d) = $a\bar{b} + c\bar{d}$

Read Only Memory (ROM)

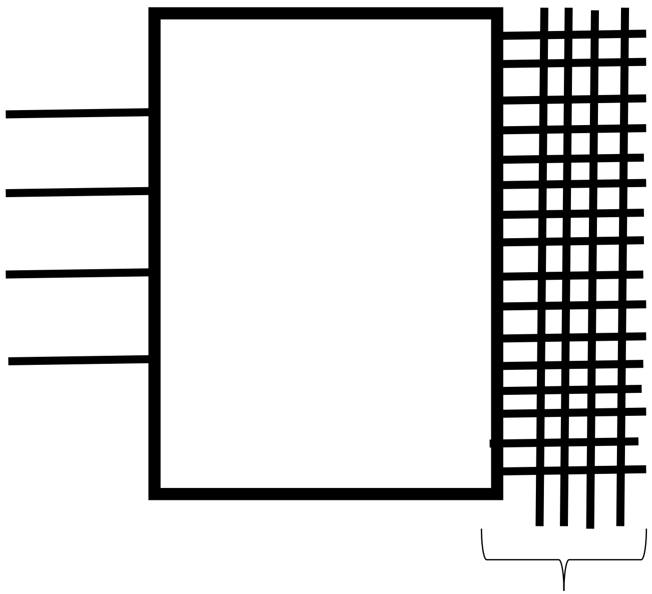
2^M x N ROM

M = No. of inputs
N = No. of outputs





1 output



4 output

2^M x N ROM

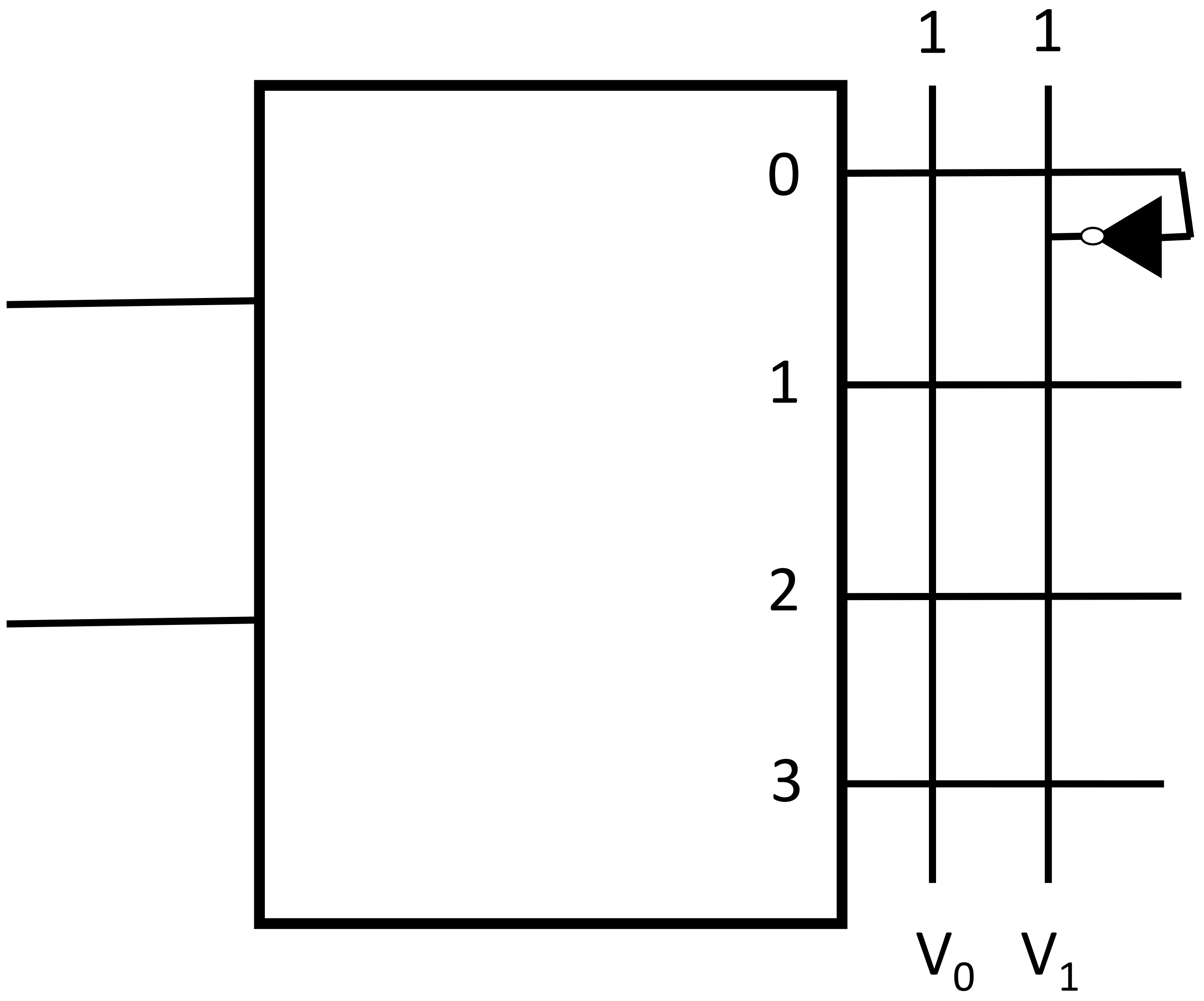
When M = 2 and N = 1

2^2 x 1 = 4 x 1 ROM

When M = 4 and N = 4

2^4 x 4 = 16 x 4 ROM

4x2 ROM



Implement the given expression using 4x1 ROM

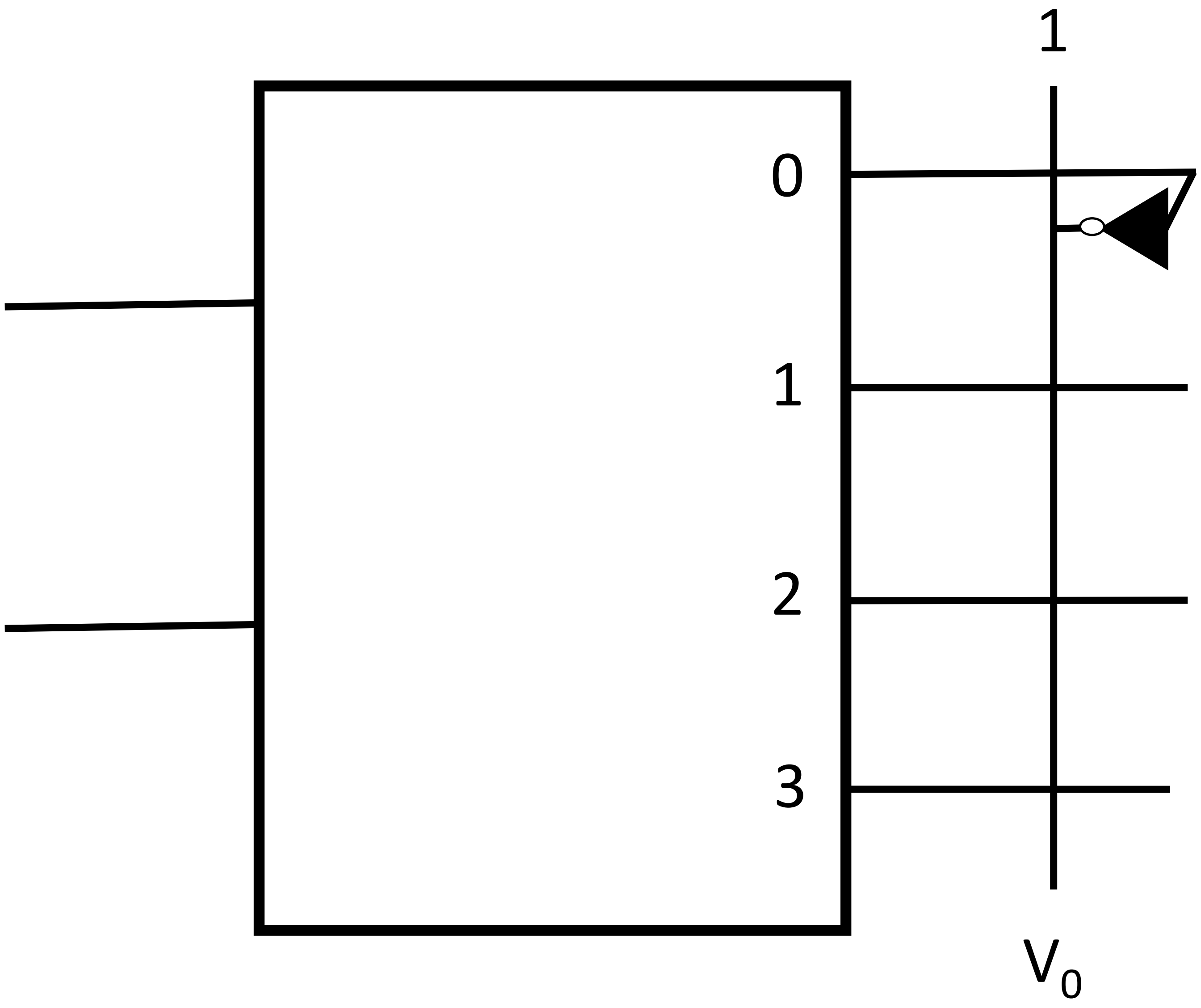
- f (A_0, A_1) = $\Sigma(1,2,3)$

So ROM size:

2^2 x 1 = 4 x 1 ROM

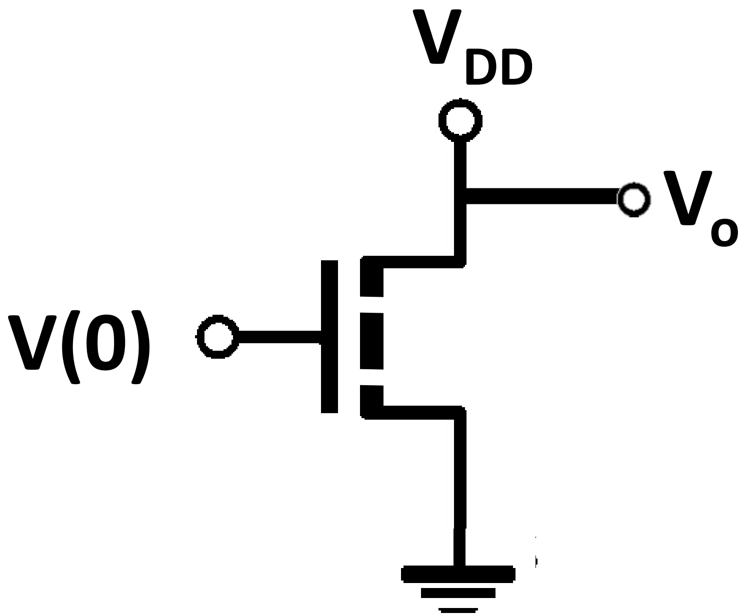
A_0	A_1	output
0	0	0
0	1	1
1	0	1
1	1	1

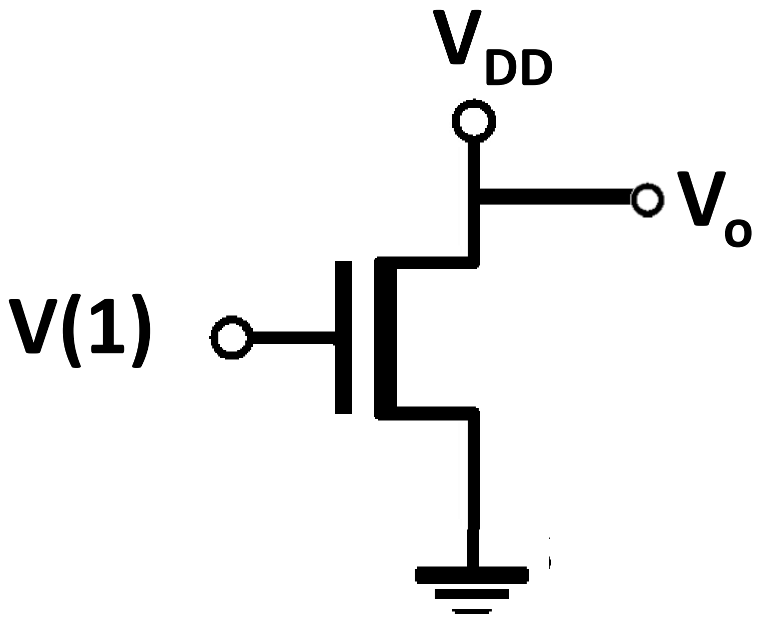
4x1 ROM



Reviewing NMOS Inverter functionality

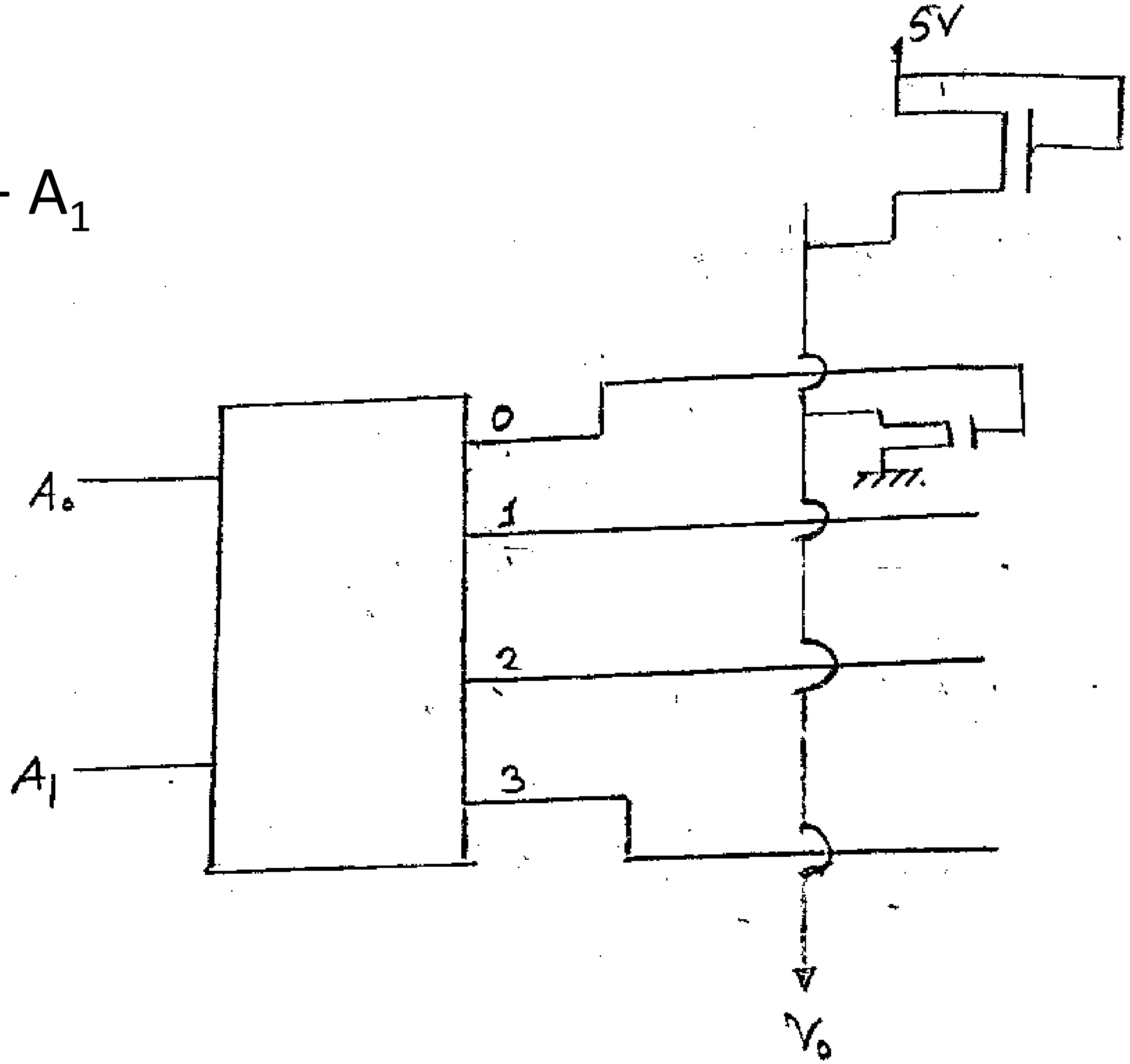
V_i	NMOS	V_o
V(0)	OFF	V_{DD}
V(1)	ON	GND





$f(A_0, A_1) = \Sigma(1,2,3) = A_0 + A_1$

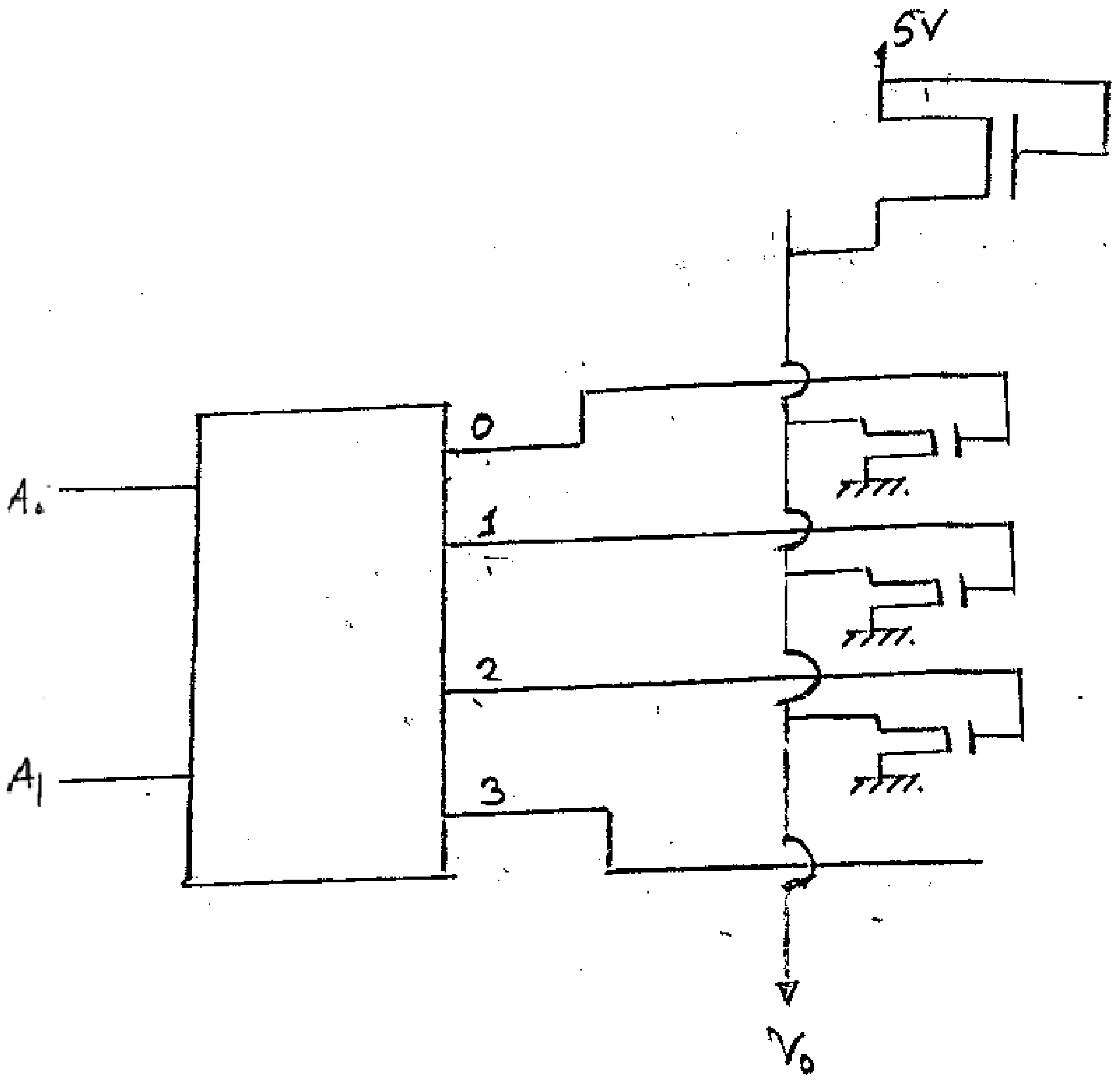
A_0	A_1	output
0	0	0
0	1	1
1	0	1
1	1	1



Use NMOS for 0 outputs.

$$f(A_0, A_1) = \Sigma(3) = A_0 A_1$$

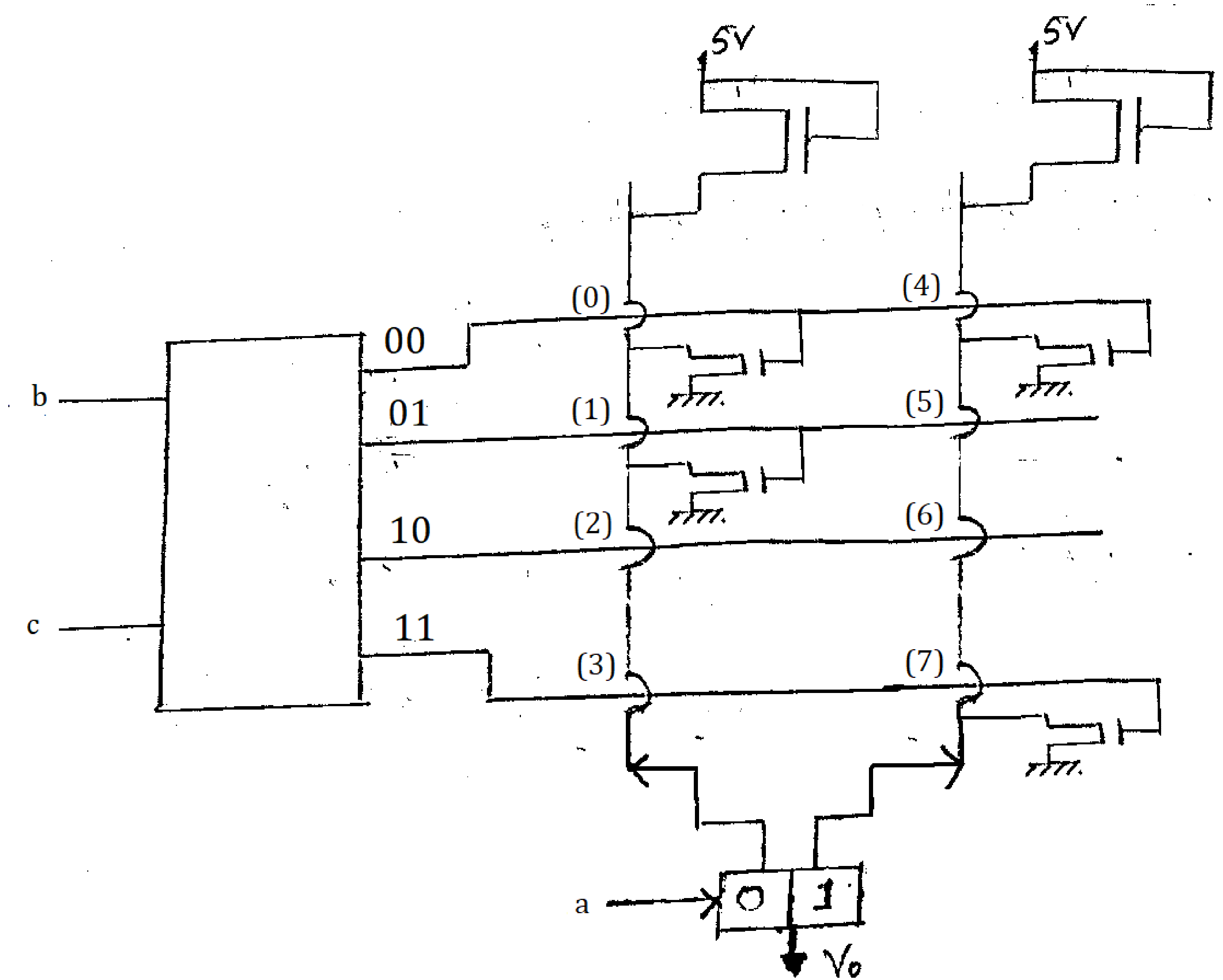
A_0	A_1	output
0	0	0
0	1	0
1	0	0
1	1	1



Implement f (a,b,c) = $\Sigma(2,3,5,6)$
using 4 x 1 ROM

Here, $\pi(0,1,4,7)$

Let,
a is selector


5V
5V
(0)
(4)
00
b
01
(1)
(5)
10
(2)
(6)
c
11
(3)
(7)
a
0
1
Vo

Implement using 2x1 or/and 4x1 ROM

- F(a,b,c) = $\Sigma(0,2,4,6)$
- F(x,y,z) = xy + $\bar{z}$
- F(x,y,z) = xy + yz + zx

*Hint: Express the equation into min terms and then implement them.