AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Department of Computer Science and Engineering

DIGITAL LOGIC DESIGN LAB
CSE 2106

Experiment No : 09

Experiment Name : (a) Design a 4 to 2 Line Priority Encoder Where the Priority is - $I_0 < I_1 < I_2 < I_3$

(b) Implement the following Boolean Function Using

I. An 8 to 1-Line Multiplexer (IC-74151)

II. A 4 to 1-Line Multiplexer (IC-74153)

And other Basic Gates. $F(A,B,C,D) = \Sigma(1,3,5,8,11,14)$

(c) Implement the following Boolean Function Using

I. 1 to 8 Line De-Multiplexer / 3 to 8 Line Decoder (IC-74138)

II. 1 to 16 Line De-Multiplexer / 4 to 16 Line Decoder (IC-74154)

$F(A,B,C,D) = \Sigma(2,3,5,7,11,13)$

Submitted by

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a) Experiment Name :

Design a 4 to 2 Line Priority Encoder where the Priority is - $I_0 < I_1 < I_2 < I_3$.

Objective :

A priority encoder is a circuit or algorithm that compresses multiple binary inputs into a smaller number of outputs. The output of a priority encoder is the binary representation of the original number starting from zero of the most significant input bit. If two or more inputs are given at the same time, the input having the highest priority will take precedence. The outputs are often used to control interrupt requests by acting on the highest priority encoder.

Truth Table :

I_3	I_2	I_1	I_0	F_1	F_0
0	0	0	1	0	0
0	0	1	x	0	1
0	1	x	x	1	0
1	x	x	x	1	1

Expression :

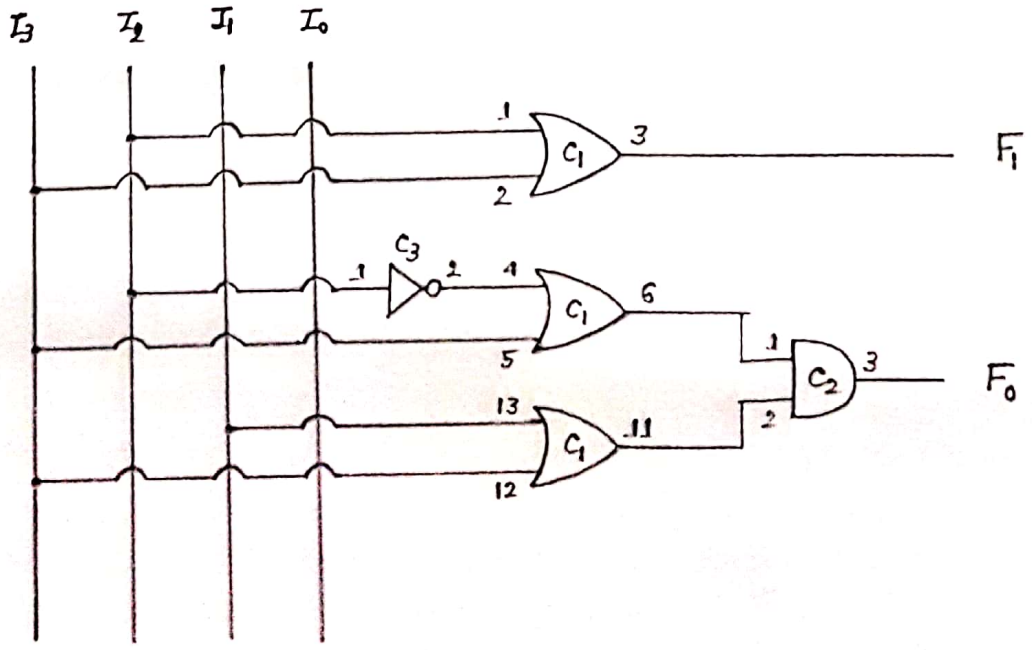
$$F_1 = \bar{I}_3 I_2 + I_3 = (I_3 + \bar{I}_3)(I_3 + I_2)$$

$$\therefore F_1 = I_2 + I_3$$

$$F_0 = \bar{I}_3 \bar{I}_2 I_1 + I_3$$

$$\therefore F_0 = (\bar{I}_2 + I_3)(I_1 + I_3)$$

Circuit Diagram :



IC Requirements :

1. C_1 → 7432 (OR Gate) — 1 piece
2. C_2 → 7408 (AND Gate) — 1 piece
3. C_3 → 7404 (NOT Gate) — 1 piece

Conclusion :

In this experiment, we use basic logic gates (AND, OR, NOT) to design the priority encoder circuit. We have to be ensure that connections are proper to get exact output. We also have to be careful when we will work to set the circuit. If we get output to the inputs according to the function, then our experiment is successful.

b) Experiment Name :

Implement the following Boolean Function Using

I. An 8 to 1 Line Multiplexer (IC-74151)

II. A 4 to 1 Line Multiplexer (IC-74153)

And other Basic Gates.

$$F(A,B,C,D) = \Sigma(1,3,5,8,11,14)$$

Objective :

In electronics, a multiplexer (mux) is a derice that selects between several analog and digital input signals and towards it to a single output line. A multiplexer of input s has selectlines, which are used to select which input line to send to the output. Multiplexer are mainly used to increase the amount of data that can be sent over the network within a certain amount of time. and bandwidth. A 8X1 multiplexer has three selection lines and 8 input lines. On the other hand a 4X1

MUX has 2 selection lines and 4 input lines. The main objective of the experiment is to implement the given boolean function using 8X1 MUX and 4X1 MUX.

i) Using 8 to 1 line Multiplexer :

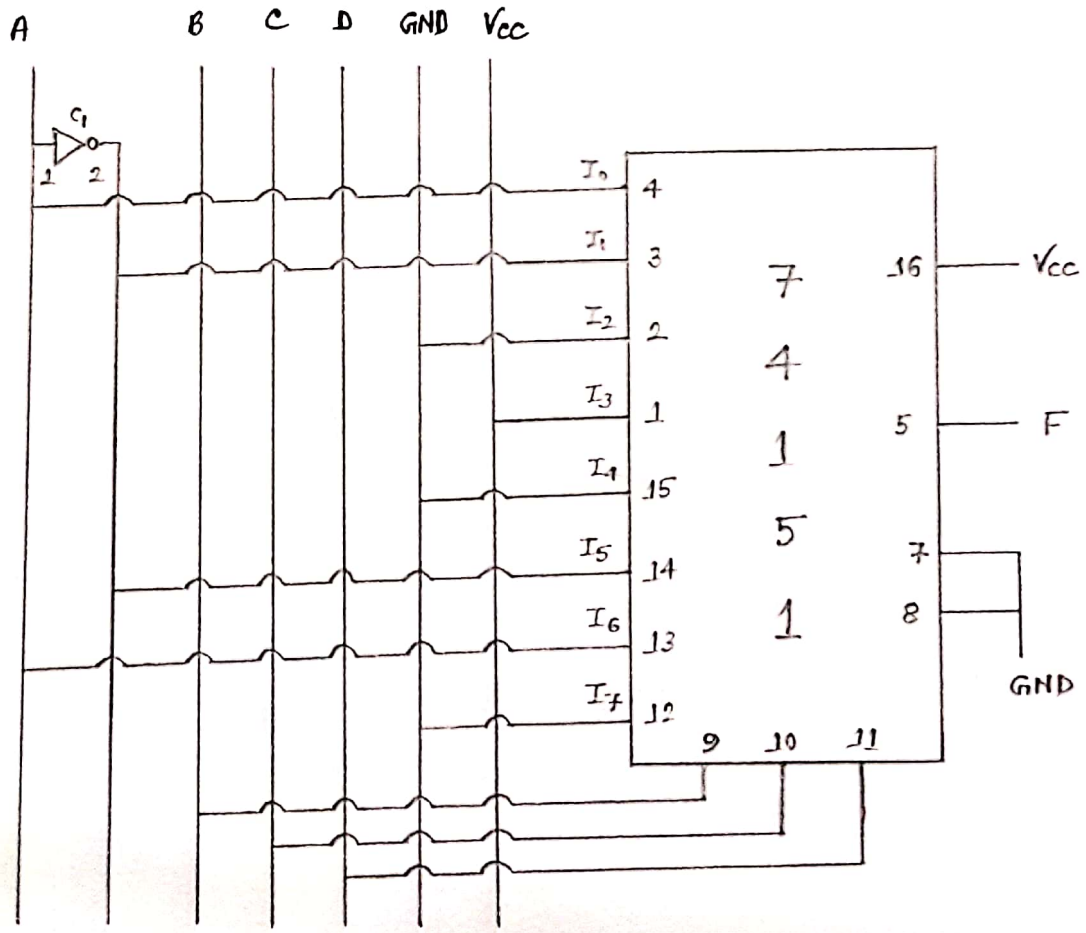
Truth Table :

Decimal	Input				Output
	A	B	C	D	F
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	0
5	0	1	0	1	1
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	1
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	1
12	1	1	0	0	0
13	1	1	0	1	0
14	1	1	1	0	1
15	1	1	1	1	0

Implementation Table :

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{A}$	0	(1)	2	(3)	4	(5)	6	7
A	(8)	9	10	(11)	12	13	(14)	15
	A	$\bar{A}$	0	1	0	$\bar{A}$	A	0

Circuit Diagram :



IC Requirements :

1. C_1 → 7404 (NOT Gate) – 1 piece
2. C_2 → 74151 (8 to 1 MUX) – 1 piece

ii) Using 4 to 1 Multiplexer :

Implementation Table :

	I_0	I_1	I_2	I_3
$\bar{A}\bar{B}$	0	(1)	2	(3)
$\bar{A}B$	4	(5)	6	7
$A\bar{B}$	(8)	9	10	(11)
AB	12	13	(14)	15

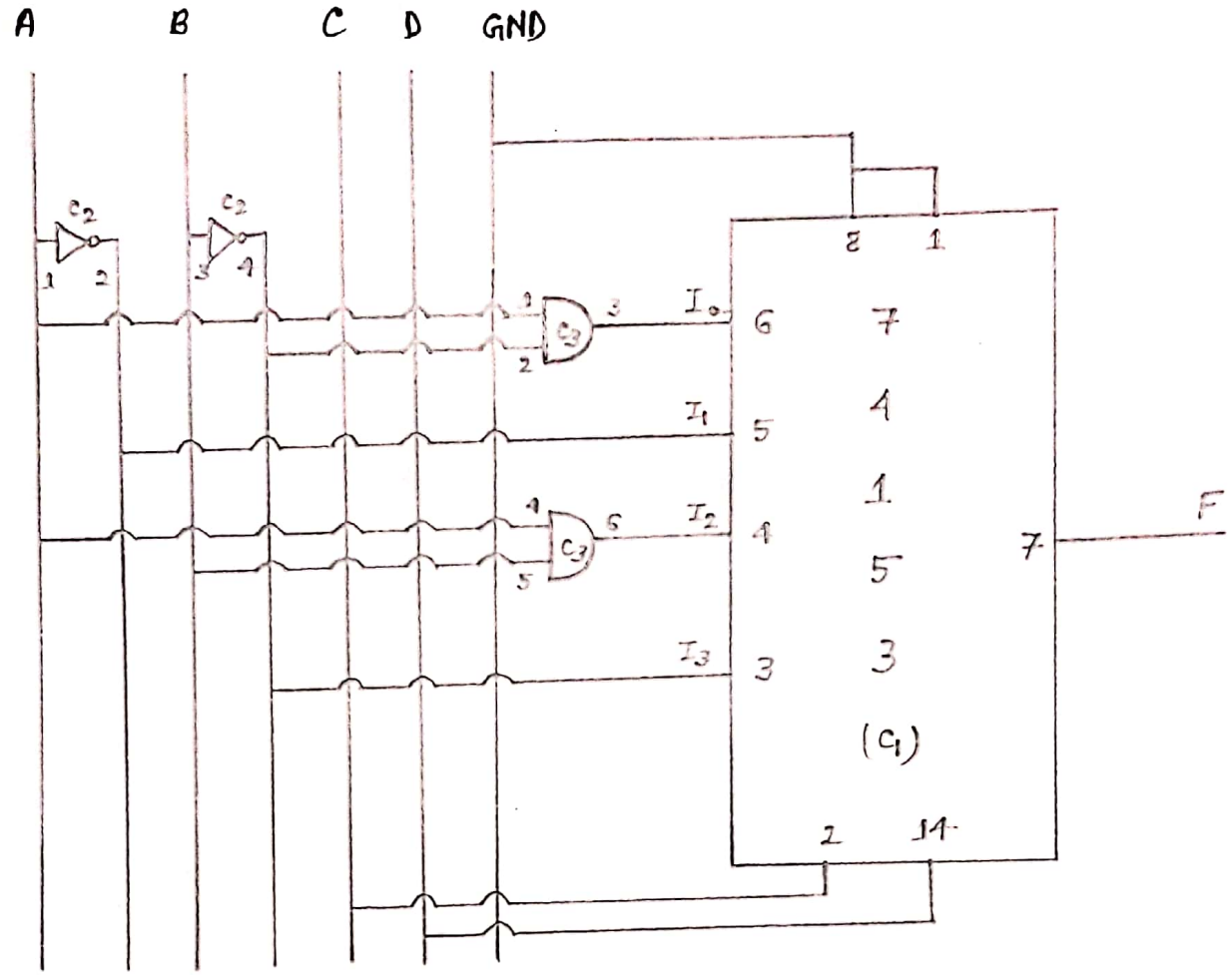
$I_0 = A\bar{B}$

$I_1 = \bar{A}\bar{B} + \bar{A}B = \bar{A}(\bar{B}+B) = \bar{A}.1 = \bar{A}$

$I_2 = AB$

$I_3 = \bar{A}\bar{B} + A\bar{B} = \bar{B}(\bar{A}+A) = \bar{B}.1 = \bar{B}$

Circuit Diagram :



IC Requirements :

1. C_1 → 74153 (4×1 MUX) — 1 piece
2. C_2 → 7404 (NOT Gate) — 1 piece
3. C_3 → 7408 (AND Gate) — 1 piece

Conclusion :

We have implemented a 4X1 MUX and 8X1 MUX. We will have to be careful in using the multiplexers. We have to be ensure that connections are proper according to pin numbers. If we get output to the inputs according to the function, then our experiment is successful.

c) Experiment Name :

Implement the following boolean function using :

i) 1 to 8 Line De-Multiplexer / 3 to 8 Line Decoder (IC-74138)

ii) 1 to 16 Line De-Multiplexer / 4 to 16 Line Decoder (IC-74154)

$$F(A,B,C,D) = \Sigma(2,3,5,7,11,13)$$

Objective :

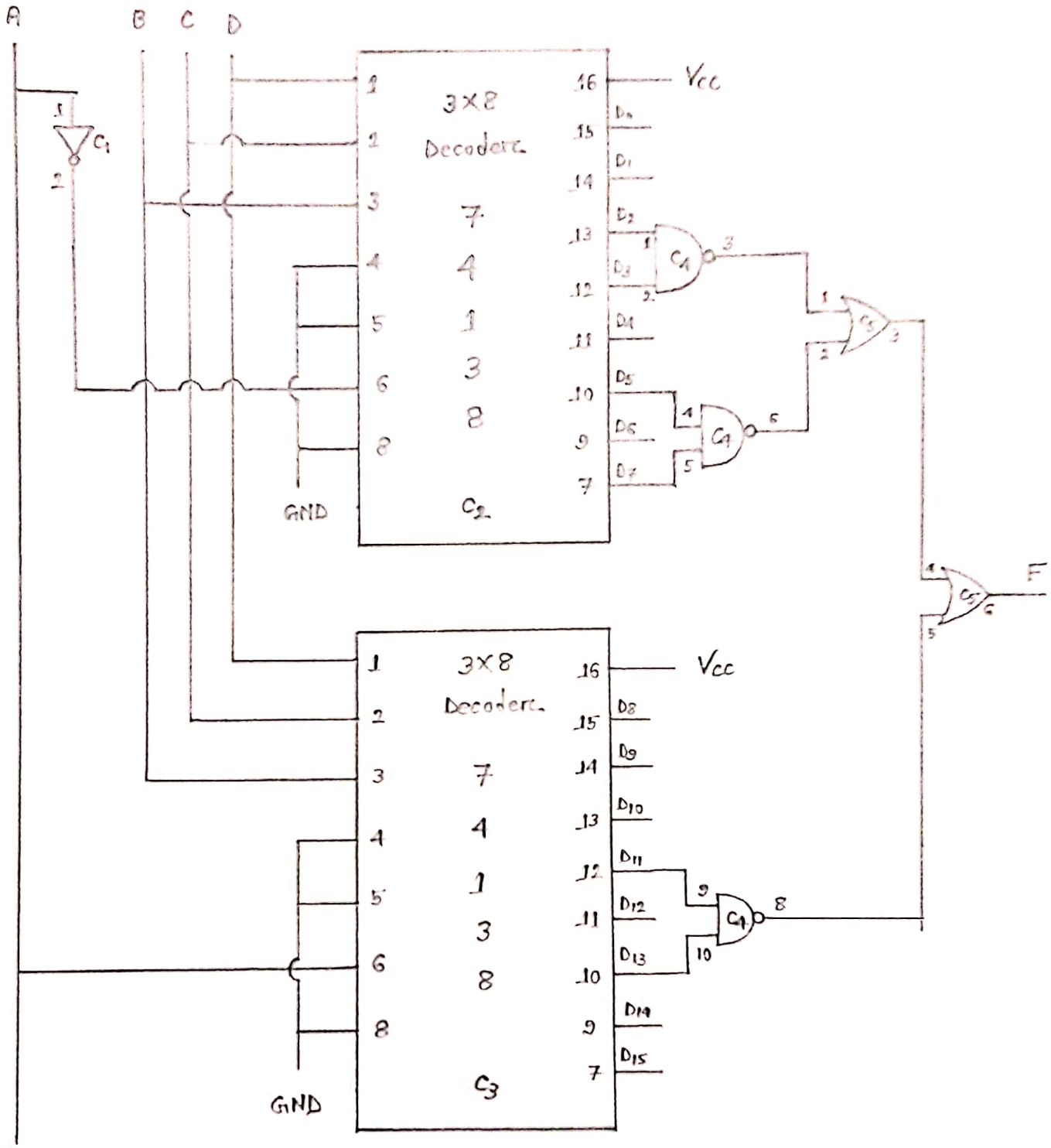
In digital electronics, a binary decoder is a combinational circuit that converts binary information from the n coded inputs to a maximum of 2^n unique outputs. As such, a decoder which has n number of input lines has 2^n number of output lines. The main objective of this experiment is to implement the given function using 3 to 8 Line decoder as well as 4 to 16 line decoder.

Truth Table :

Input				Output
A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

Circuit Diagram :

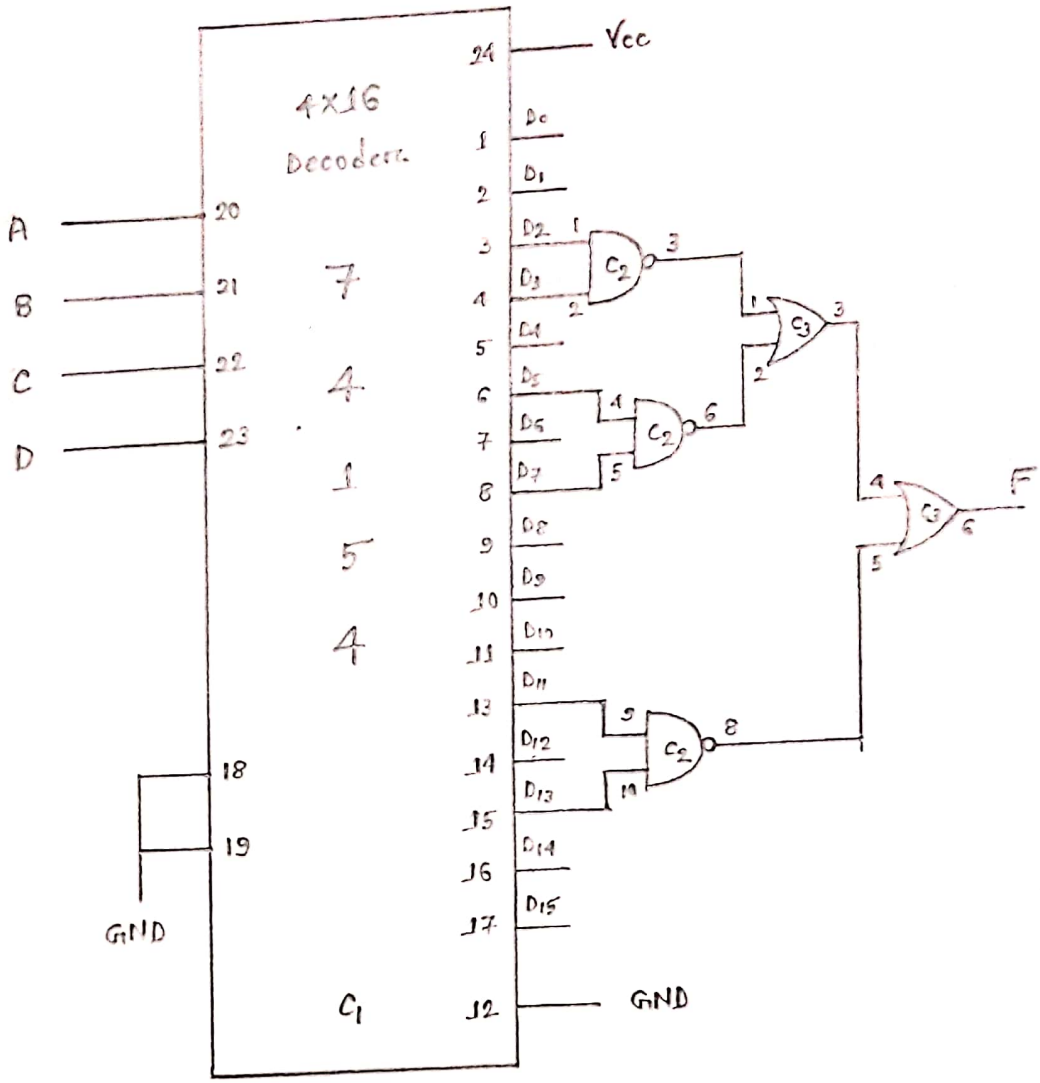
i) Using 3 to 8 Line decoder :



IC Requirements :

1. C_1 → 7404 (NOT Gate) — 1 piece
2. C_2, C_3 → 74138 (3X8 Decoder) — 2 pieces
3. C_4 → 7400 — 1 piece
4. C_5 → 7432 (OR Gate) — 1 piece

ii) Using 4 to 16 line decoder :



IC Requirements :

1. C_1 → 74154 (4X16 Decoder) → 1 piece
2. C_2 → 7400 → 1 piece
3. C_3 → 7432 (OR Gate) → 1 piece

Conclusion :

We have implemented a 3 to 8 line Decoder and a 4 to 16 line decoder. If our connections are proper and we get output according to input then our experiment is successful.