Ahsanullah University of Science and Technology (AUST)

Department of Computer Science and Engineering

LAB REPORT

Course No. : CSE2210

Course Title: Digital Electronics and Pulse Techniques Lab

Experiment Number: 01

Name of the Experiment: Study of DL & DTL Gates

Submitted By:

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Name of the Experiment :

Study of DL and DTL gates.

Objective :

Diode Logic (DL) is the construction of boolean logic gates from diodes. Diode transistor Logic (DTL) is a class of digital circuits that is the direct ancestor of transistor – transistor logic. The main objective of this experiment is the study of DL and DTL gates by measuring the output voltage and other voltage at various points for all possible inputs.

Circuit Diagram :

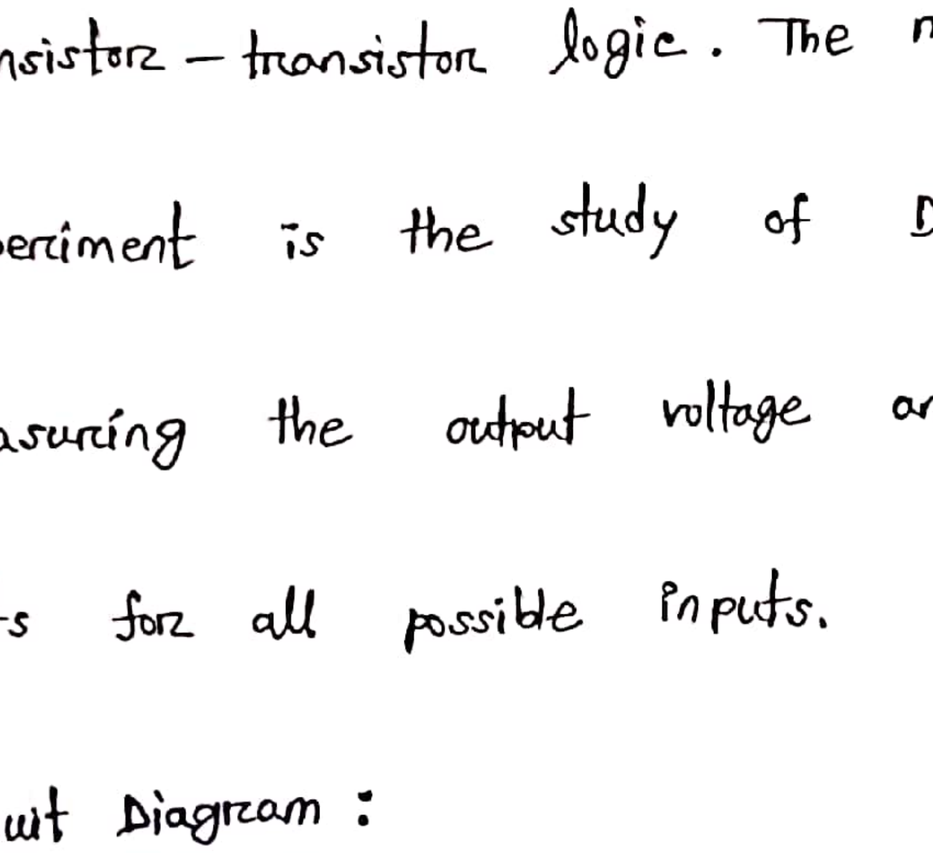

Fig : Circuit 1

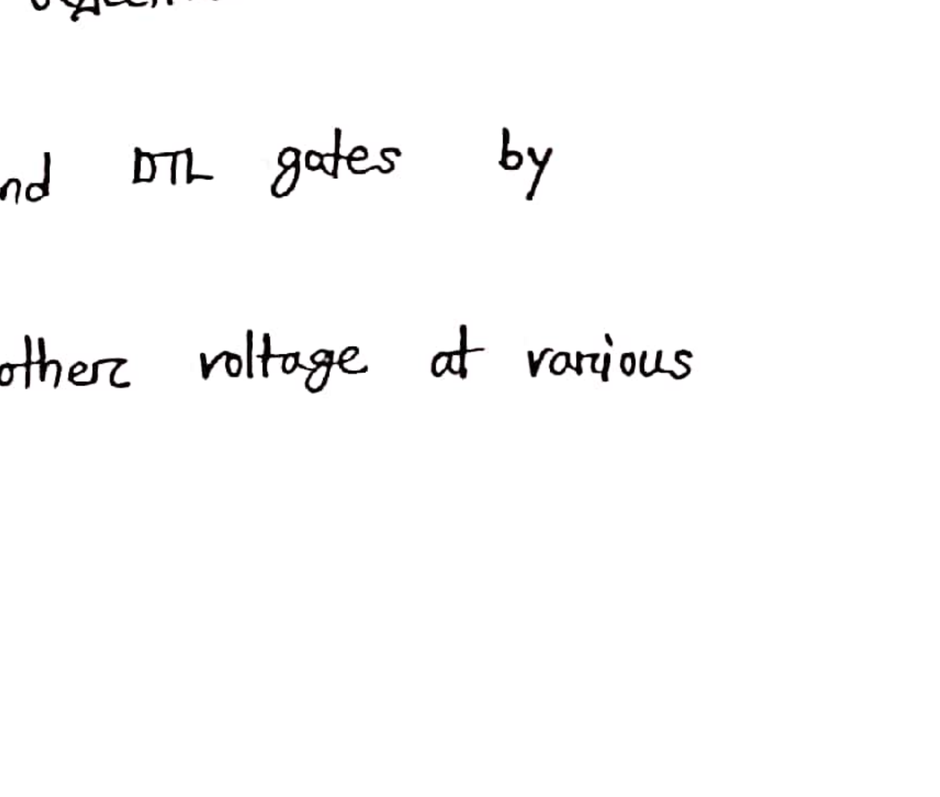

Fig : Circuit 2

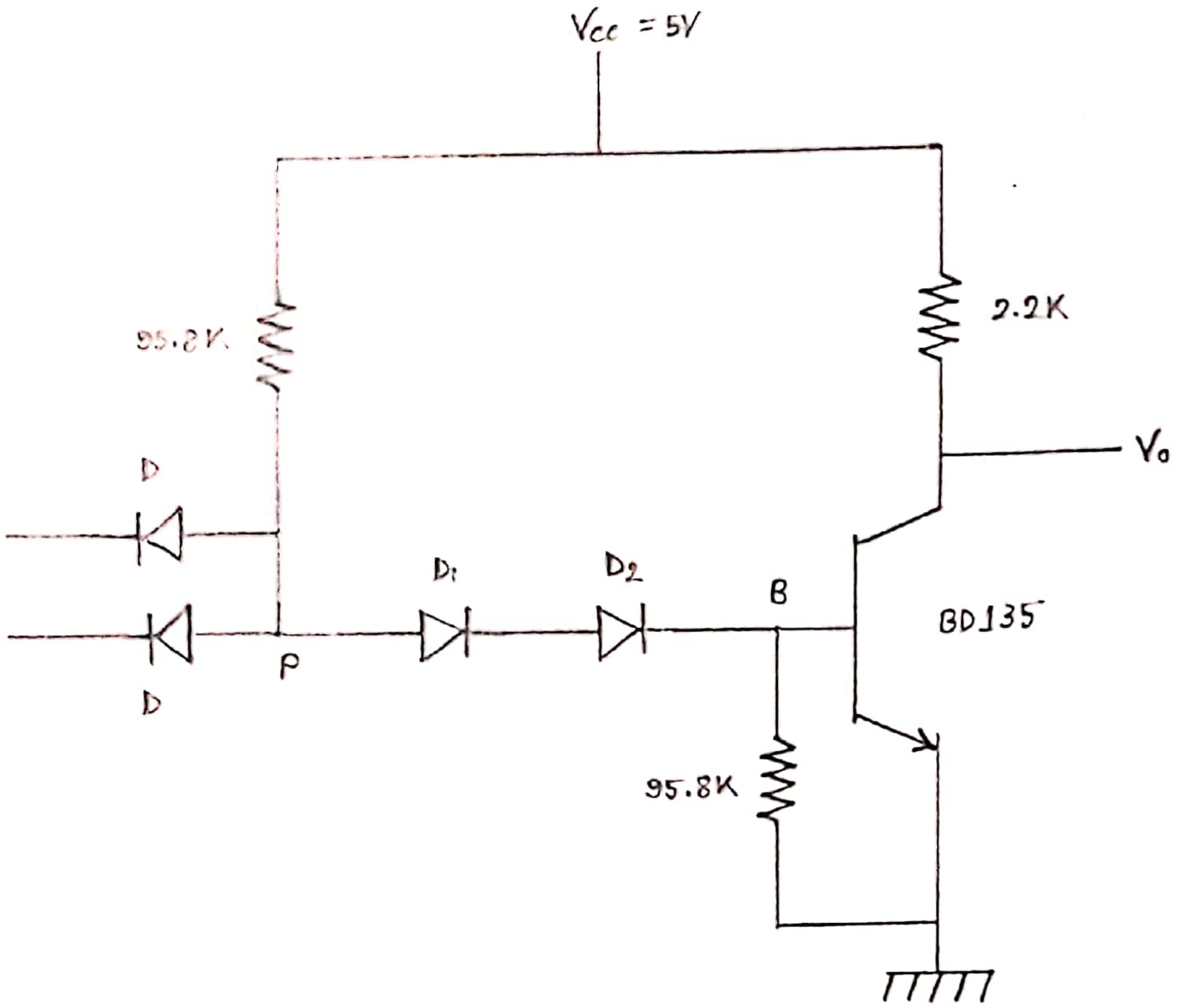

Fig: Circuit 3

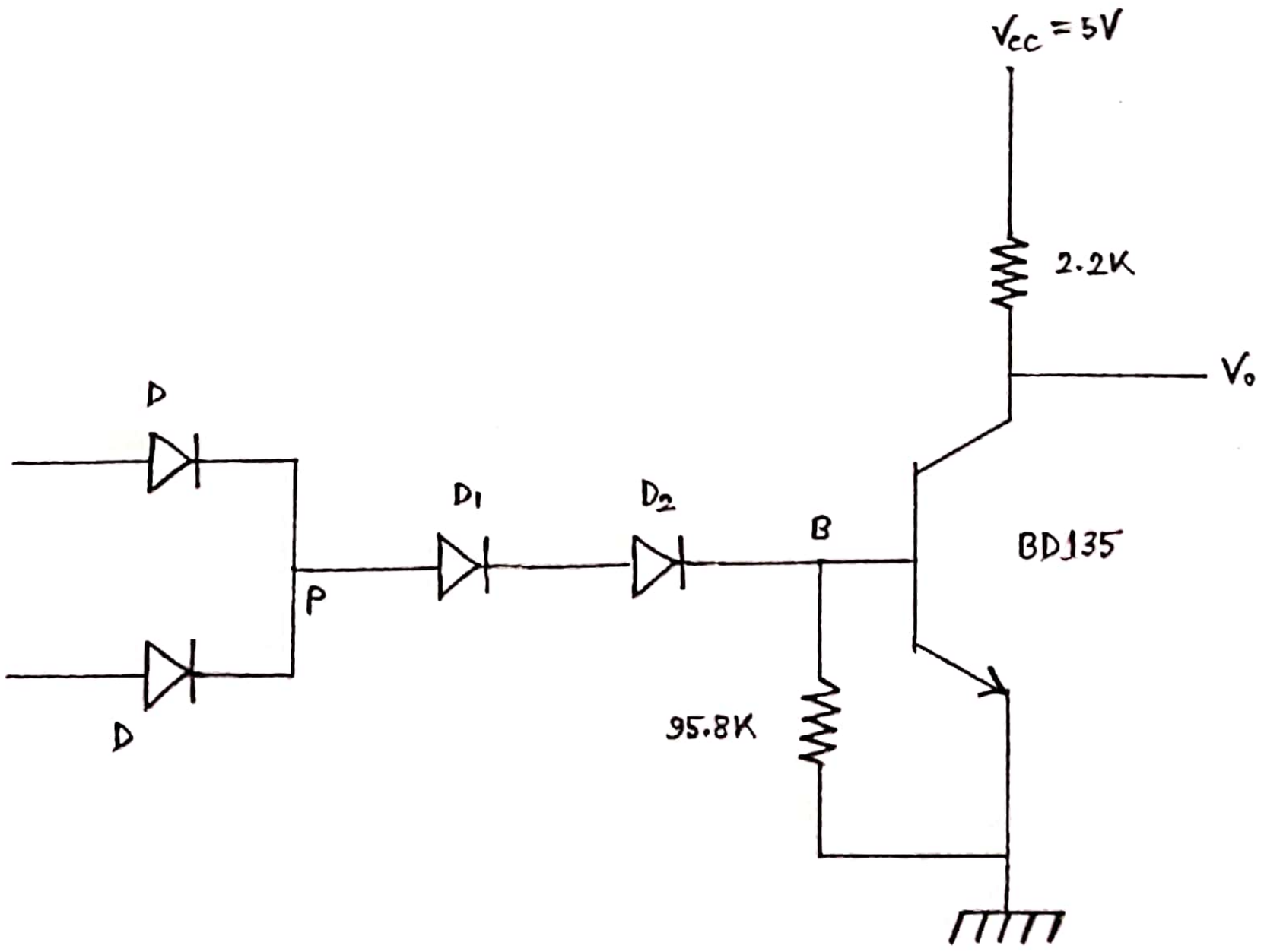

Fig: Circuit 4

Answers to the Questions :

① Analyze the circuit 1 and circuit 2 with the help of truth table for both positive and negative logic.

Ans: For ckt 1, when we give high voltage to both of the inputs, only then it gives the high voltage output. For any other input combinations it gives low voltage output.

A	B	V_o
0V	0V	0.57V
0V	5V	0.60V
5V	0V	0.60V
5V	5V	5.00V

Voltage level representation for positive logic :-

A	B	V_o
V(0)	V(0)	V(0)
V(0)	V(1)	V(0)
V(1)	V(0)	V(0)
V(1)	V(1)	V(1)

So, in positive logic this circuit works an as AND Gate.

Now, Voltage representation of negative logic :-

A	B	V_o
V(1)	V(1)	V(1)
V(1)	V(0)	V(1)
V(0)	V(1)	V(1)
V(0)	V(0)	V(0)

So, for negative logic this circuit works as an OR Gate.

For circuit 2, when we give both of the inputs low voltage only then the output gives low voltage. For any other input combinations the circuit given high voltage.

For positive Logic,

A	B	V_o
0V	0V	0.00V
0V	5V	4.40V
5V	0V	4.40V
5V	5V	4.43V

Voltage level representation for positive logic:

A	B	V_o
V(0)	V(0)	V(0)
V(0)	V(1)	V(1)
V(1)	V(0)	V(1)
V(1)	V(1)	V(1)

So, this circuit works as an OR gate in positive logic.

For negative logic,

A	B	V_o
V(1)	V(1)	V(1)
V(1)	V(0)	V(0)
V(0)	V(1)	V(0)
V(0)	V(0)	V(0)

So, this circuit works as an AND gate for negative logic.

② What happens if V_R is more positive than V(1)?

[ckt 1]

Ans: If we set V_R more positive than V(1), then both of the diodes will be in forward bias, so if we give high voltage input for both of the inputs we wont be able to get high voltage output. And also it will hamper the property of the circuit.

③ What happens if not all inputs have the same upper level ? [ckt 1, ckt 2]

Ans: If not all inputs have same upper level then one diode will be in forward bias and the other will be at reverse bias condition. So, we will not get the proper output. The AND gate property of ckt 1 and the OR gate property of ckt 2 will be hampered.

④ Why diode D_2 is used ? [ckt 3, ckt 1]

Ans: We have used diode D_2 because if only the one diode D_1 is used between the voltage meter then that would represent the diode cut off in voltage. Then it can be said theoretically Q point is in the cut off. But a small spike of noise will turn Q on. That is why D_2 is used to prevent the gate from malfunctioning.

⑤ Can emitter and collector interchanged ? [ckt 3, ckt 1]

Ans: Emitter and Collector can only be interchanged if the transistor is in inverse active state. That means if base - emitter junction is in reverse bias and base - collector junction is in forward bias. If we can apply this condition in ckt 3 and ckt 1, only then the emitter and collector can be interchanged. But in that case

the output will not remain the same and which will cause the hamper of NOR and NAND gate properties of the circuits.

⑥ What is the significant of $h_{FE\,(min)}$? [ckt 3, ckt 1]

Ans: If we want to have the transistor in saturation mode, the transistor needs to be greater or equal to the minimum value of h_{FE}. The $h_{FE\,(min)}$ represents the ratio of collector current (I_C) and base current (I_B).

Experimental Data :

Circuit 1 (AND Gate) –

A	B	V_o
0V	0V	0.57 V
0V	5V	0.60 V
5V	0V	0.60 V
5V	5V	5.00 V

Positive Logic AND Gate

Circuit 2. (OR Gate) -

A	B	V_o
0V	0V	0.00V
0V	5V	1.10V
5V	0V	1.10V
5V	5V	1.13V

Circuit 3 (NAND Gate) -

A	B	V_D	V_{D1}	V_{D2}	V_P	V_{CE}	V_o
0V	0V	0.56V	0.28V	0.28V	0.56V	5.00V	5.00V
0V	5V	-1.12V	0.29V	0.29V	0.58V	5.00V	5.00V
5V	0V	0.58V	0.29V	0.29V	0.58V	5.00V	5.00V
5V	5V	-3.32V	0.57V	0.57V	1.68V	2.10V	2.10V

Circuit 1 (NOR Gate) -

A	B	V_D	V_{D1}	V_{D2}	V_P	V_{CE}	V_o
0V	0V	0.00V	0.00V	0.00V	0.00V	5.00V	5.00V
0V	5V	0.85V	0.85V	0.85V	2.46V	0.03V	0.03V
5V	0V	-2.16V	0.85V	0.85V	2.16V	0.03V	0.03V
5V	5V	0.85V	0.86V	0.86V	2.52V	0.04V	0.04V

Discussion :

In this experiment, we have studied DL and DTL gates using diodes and transistors. We have implemented four circuits and measured output voltages. The first circuits works as an AND gate, second circuit works as an OR gate. Third one works as an NAND gate and the fourth one works as a NOR gate which we can see from our output value. As, we got our desired values, our experiment has been done successfully.