Using the ideal parameters

Negative Logic AND Gate

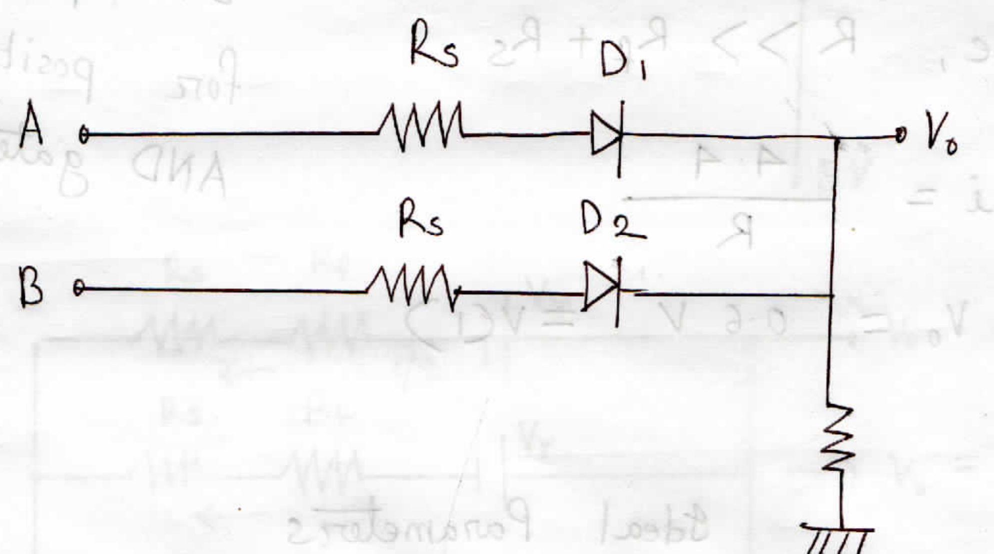
Negative Logic

$V(0) = 5V$

$V(1) = 0V$

AND Gate

A	B	V_o
V(0)	V(0)	V(0)
V(0)	V(1)	V(0)
V(1)	V(0)	V(0)
V(1)	V(1)	V(1)

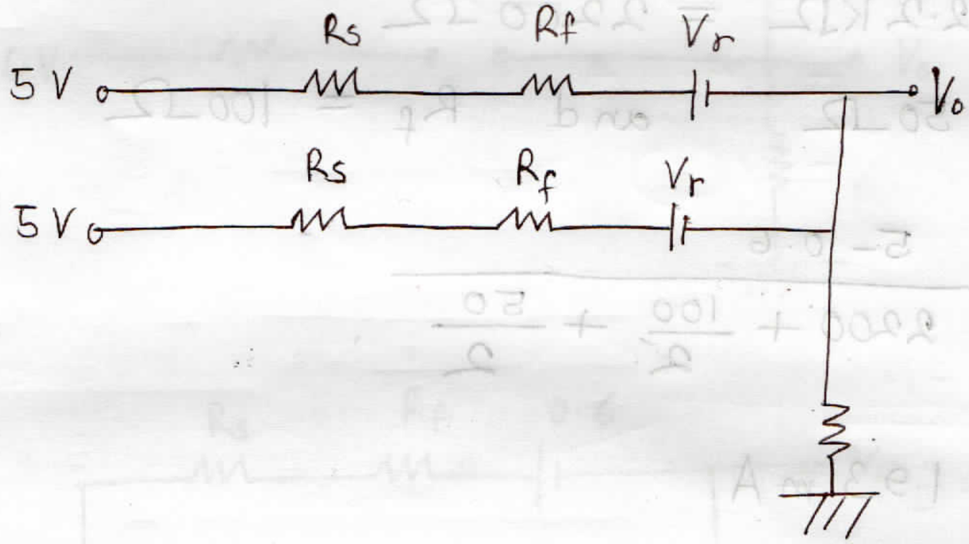


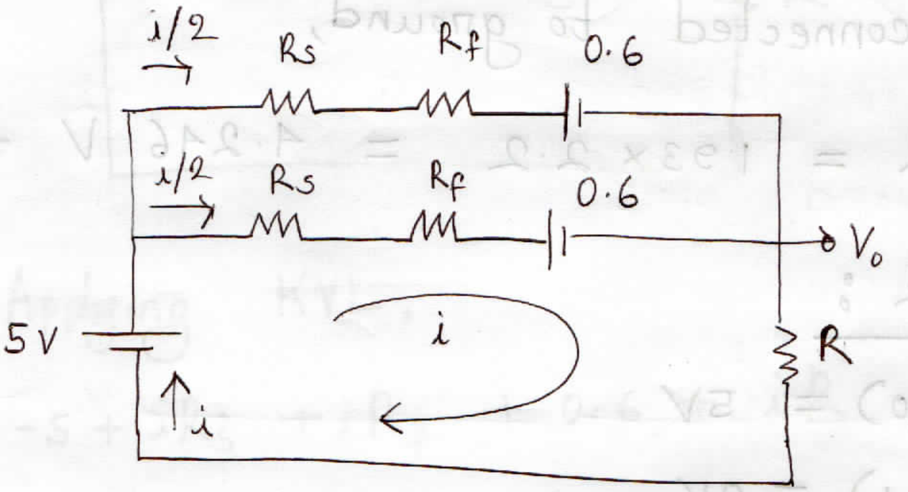
Case 1:

$A = V(0) = 5V$

$B = V(0) = 5V$

Both diodes are in forward bias





Applying KVL,

$$-5 + iR + V_r + \frac{i}{2} R_f + \frac{i}{2} R_s = 0$$

$$i = \frac{5 - V_r}{R + \frac{R_f}{2} + \frac{R_s}{2}}$$

Putting the ideal parameters, i.e

$R = 2.2 K\Omega = 2200\ \Omega$

$R_s = 50\ \Omega$ and $R_f = 100\ \Omega$

$$i = \frac{5 - 0.6}{2200 + \frac{100}{2} + \frac{50}{2}}$$

$= 1.93\ mA$

Since connected to ground,

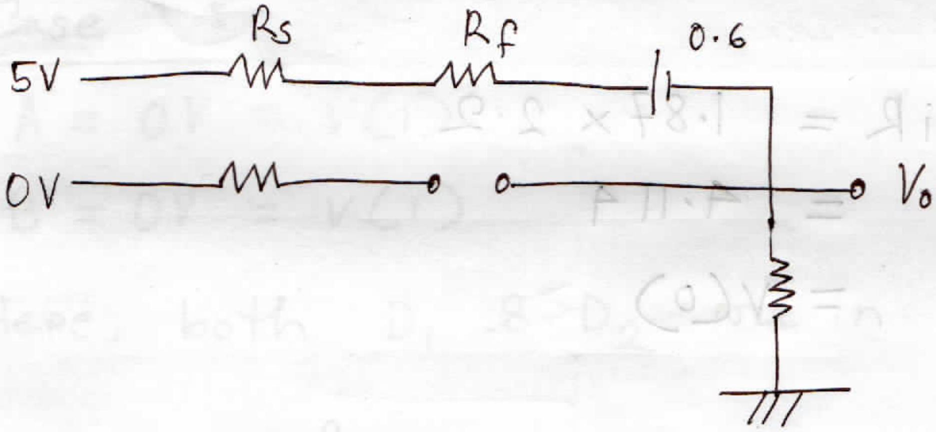
$V_o = iR = 1.93 \times 2.2 = 4.246\ V = V(0)$

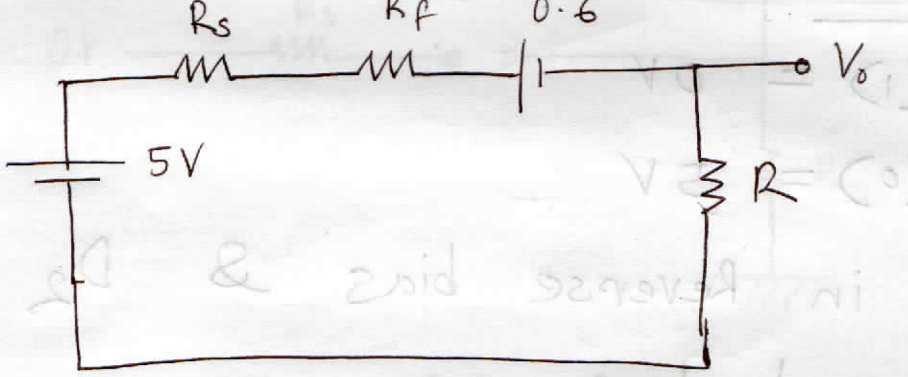
<u>Case 2 :</u>

$A = V(0) = 5V$

$B = V(1) = 0V$

Here, D_1 is in forward bias and D_2 in reverse bias.





Applying KVL,

$$-5 + iR_s + iR_f + 0.6 + iR = 0$$

$$\Rightarrow i(R_s + R_f + R) = 5 - 0.6$$

$$\Rightarrow i = \frac{5 - 0.6}{R_s + R_f + R}$$

$$= \frac{5 - 0.6}{1000 + 50 + 2200}$$

$$\therefore i = 1.87 \text{ mA}$$

So,

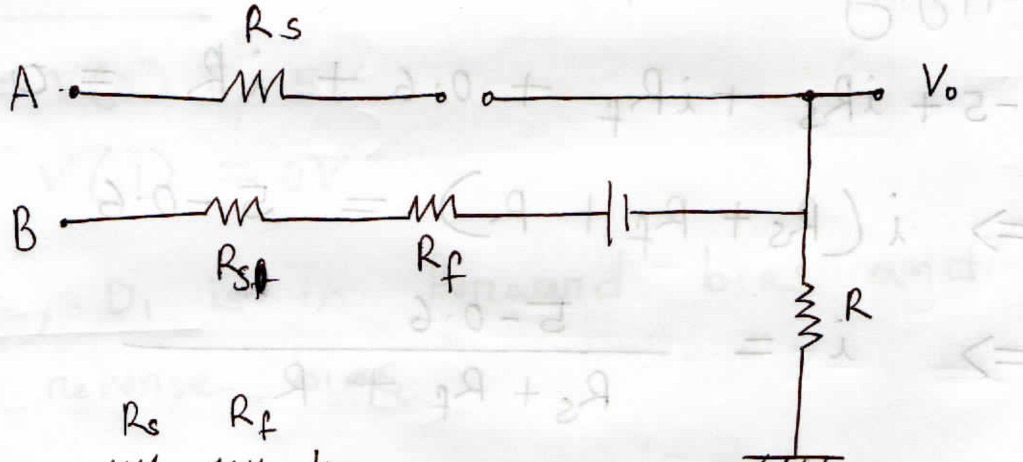
$$V_o = iR = 1.87 \times 2.2$$
$$= 4.114$$
$$= V(0)$$

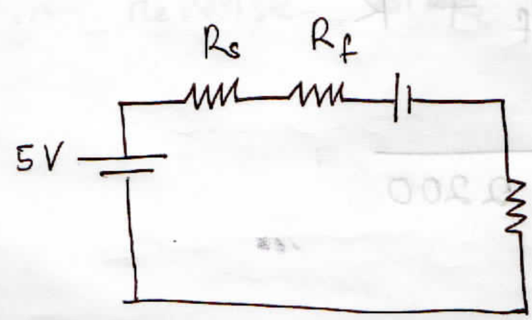
Case 3 :

$A = V(1) = 0V$

$B = V(0) = 5V$

D_1 is in Reverse bias & D_2 is in Forward bias



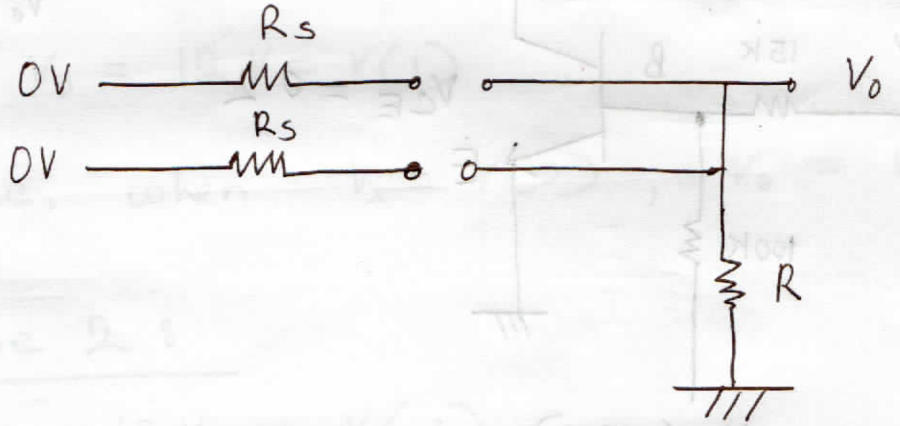


Case 4 :

$A = 0V = V(1)$

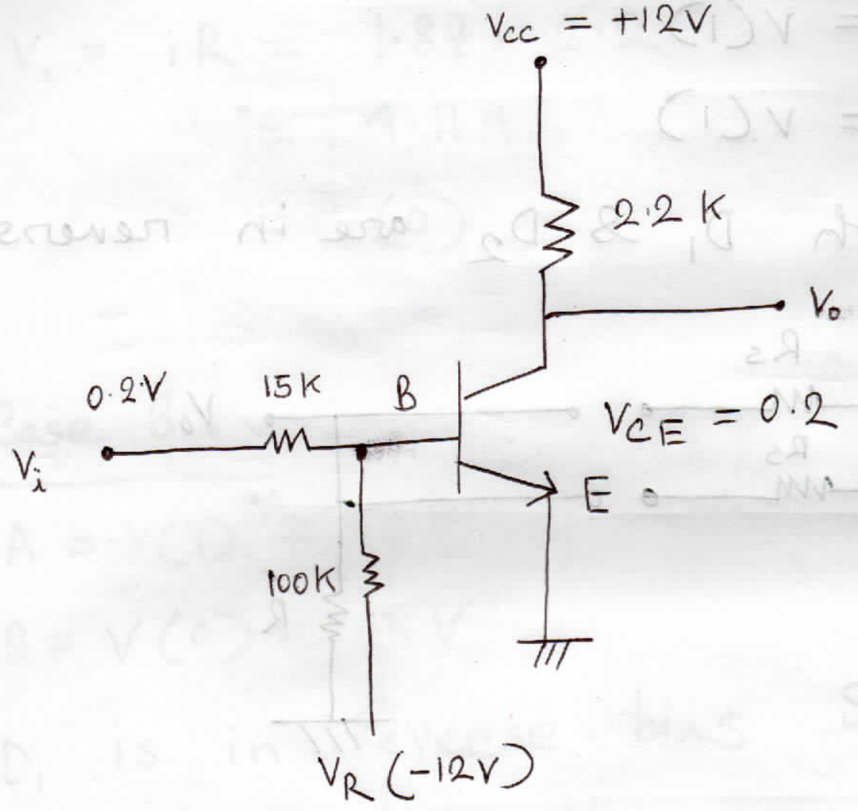
$B = 0V = V(1)$

Here, both D_1 & D_2 are in reverse bias.



$\therefore V_o = 0V = V(1)$

Transistorized NOT Gate



Here,

V_i = inpu

V_o = outpu

Positive Logic, so

$V_L = 0.2\,V = V(0)$

$V_H = 12\,V = V(1)$

Case 1:

$V_i = 0.2\,V = V(0)$

Using Superposition Theorem,

$$V_B = \frac{15}{15+100}(-12) + \frac{100}{15+100}(0.2)$$

$\therefore V_B = -1.391\ V$

As, $V_{BE} = -1.391\ V < 0.5\ V$

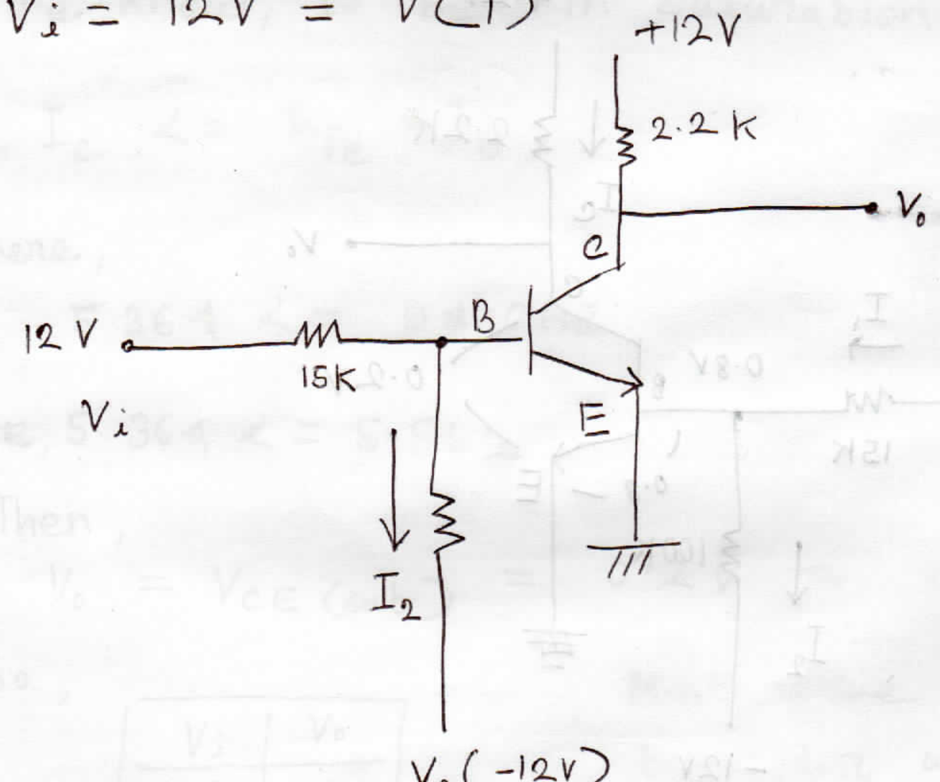
which is the cut in voltage. So, the transistor will be in cut-off state.

$\therefore V_0 = 12\ V = V(1)$

Thus, when $V_i = V(0)$, $V_0 = V(1)$.

<u>Case 2 :</u>

$V_i = 12\ V = V(1)$



Let us assume that ~~tha~~ the transistor is in saturation mode,

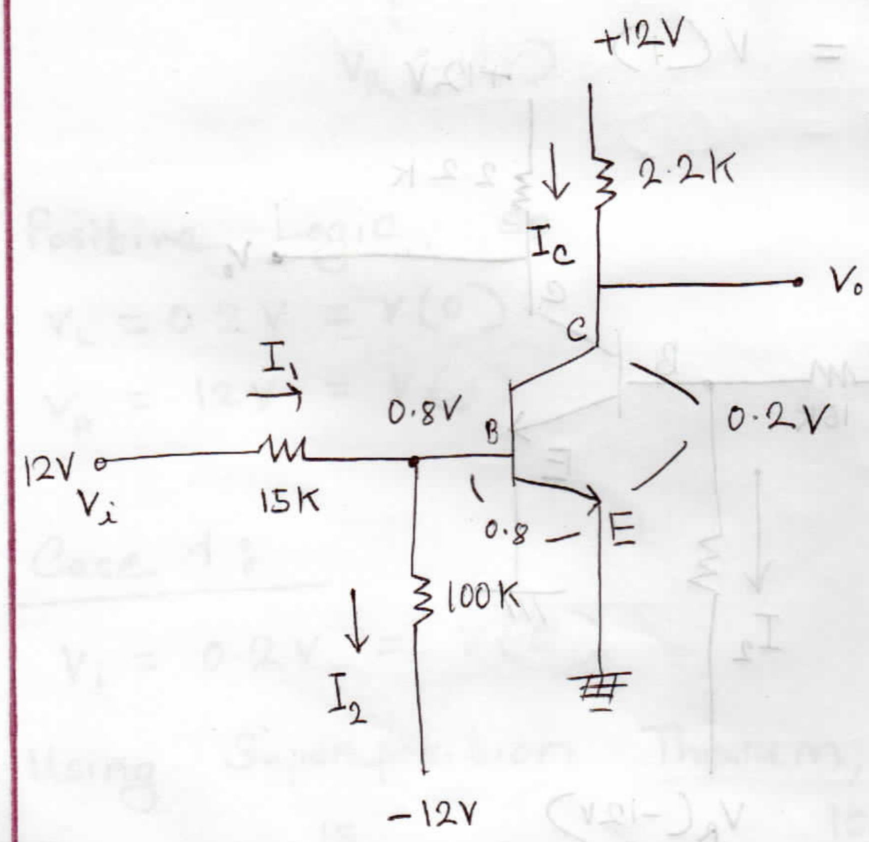
So,

$$V_{CE}\,(sat) = 0.2\,V, \quad V_{BE}\,(sat) = 0.8\,V$$

$$I_c \le h_{fe} * I_B$$

$$\Rightarrow h_{fe} \ge \frac{I_c}{I_B}$$

$$\therefore h_{fe\,(min)} = \frac{I_c}{I_B}$$



$$I_1 = \frac{12-0.8}{15K} = 0.746 \text{ mA}$$

$$I_2 = \frac{0.8-(-12)}{100K} = 0.128 \text{ mA}$$

$$\therefore I_B = I_1 - I_2 = 0.618 \text{ mA}$$

$$I_c = \frac{12-0.2}{2.2} = 5.364 \text{ mA}$$

$$\therefore h_{fe}(min) = \frac{I_c}{I_B} = \frac{5.364}{0.619} = 8.66 \approx 9$$

we know, to be in saturation mode,

$$I_c <= h_{fe} * I_B$$

here,

$$5.364 <= 9 * 0.618$$

ie, $5.364 <= 5.562$

Then,

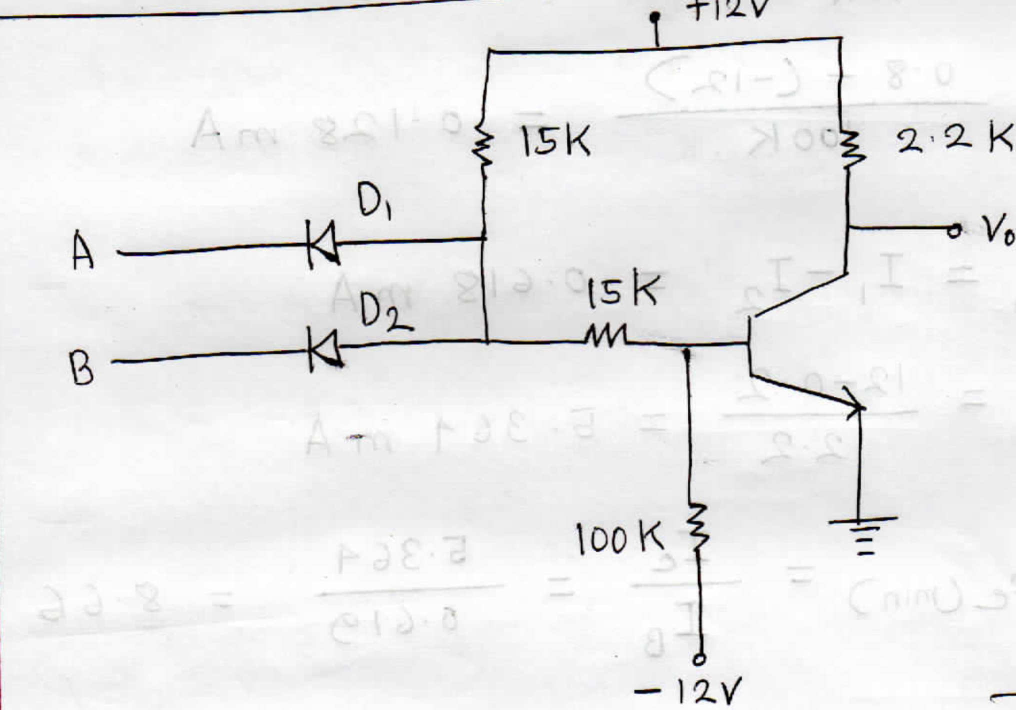
$$V_o = V_{CE}(sat) = 0.2V = V(0)$$

So,

V_i	V_o
0.2	12
12	0.2

Min^m value for which transistor will be in saturation, $h_{fe}(min) = 9$

DTL Positive Logic NAND gate :



NAND

0 0	→ 1
0 1	→ 1
1 0	→ 1
1 1	→ 0

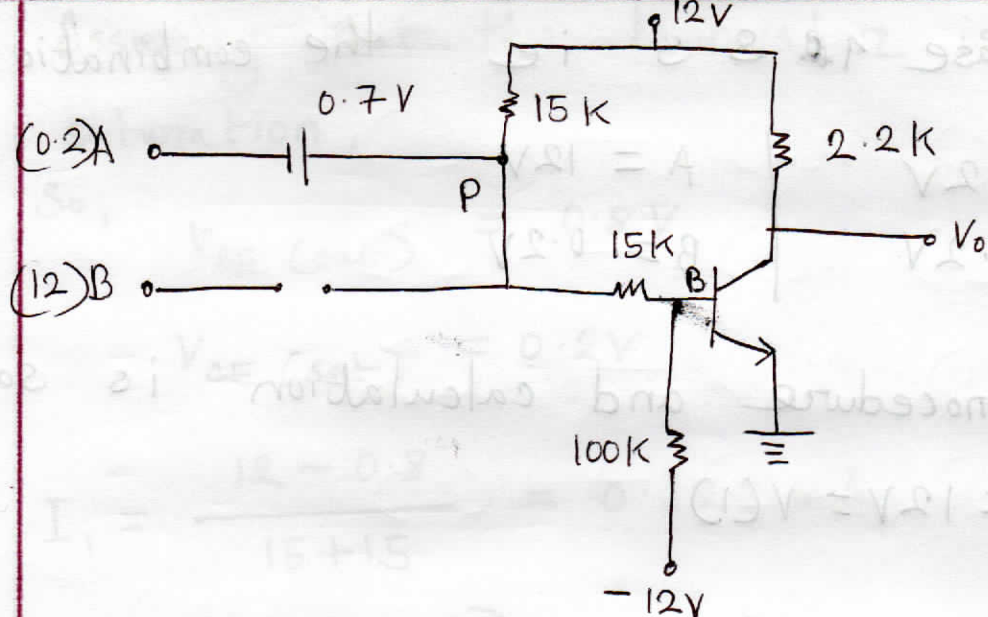
Case 1 :

$A = 0.2\,V = V(0)$

$B = 12\,V = V(1)$

So, D_1 is in Forward Bias

D_2 is in Reverse Bias



Here, Voltage at point P, $V_p = 0.2 + 0.7$
$= 0.9V$

Now, using Superposition,

$$V_B = \frac{100}{15+100}(0.9) + \frac{15}{15+100}(-12)$$

$$= -0.782\ V < 0.5\ V$$

which is the cut in voltage of transistor
So, transistor is is cut off mode.

$\therefore\ V_o = 12V = V(1)$

For case 1 & 3 i.e the combination,

$A = 0.2V$ | $A = 12V$

$B = 0.2V$ | $B = 0.2V$

DIY The procedure and calculation is same.

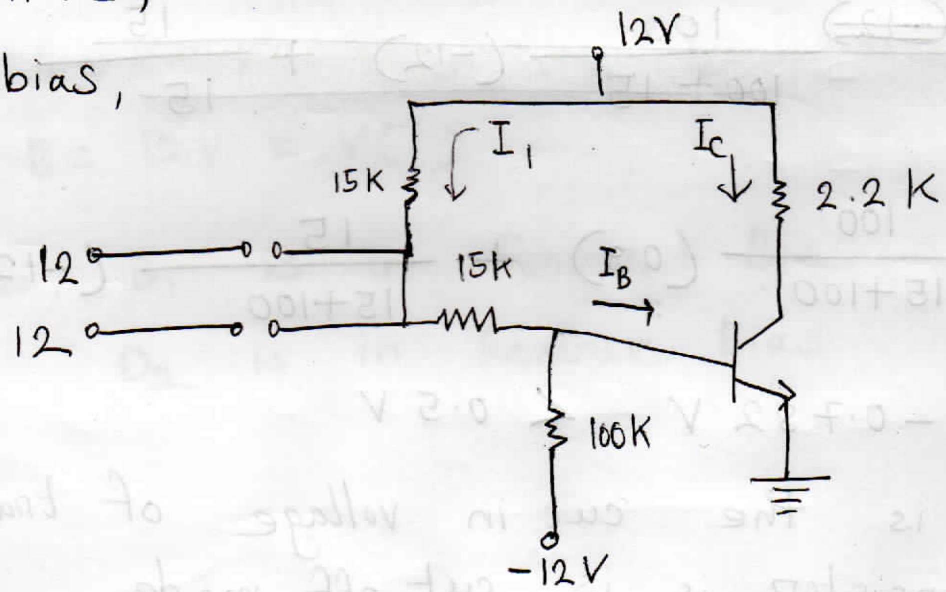
$\therefore V_0 = 12V = V(1)$

Case 4 :

$A = 12V = V(1)$

$B = 12V = V(1)$

Here, both D_1 & D_2 are in reverse bias,



Assuming that the transistor is in saturation,

So,

$$V_{BE\,(sat)} = 0.8\,V$$

$$V_{CE\,(sat)} = 0.2\,V$$

$$I_1 = \frac{12 - 0.8}{15+15} = 0.373\ mA$$

$$I_2 = \frac{0.8 - (-12)}{100} = 0.128\ mA$$

$$I_B = I_1 - I_2 = 0.245\ mA$$

$$I_c = \frac{12-0.2}{2.2} = 5.3636\,mA \approx 5.364\ mA$$

$$h_{fe\,(min)} = \frac{I_c}{I_B} = \frac{5.364}{0.245} = 21.89 \approx 22$$

here,

$$I_c <= h_{fe} * I_B$$

So, transistor will be in saturation mode.

$$\therefore\ V_0 = 0.2\,V = V(0)$$

Min^m value at which transistor will be in saturation is ~~22~~ $h_{fe\,(min)} = 22$

Thus,

$V(0) \quad V(0) \rightarrow V(1)$

$V(0) \quad V(1) \rightarrow V(1)$

$V(1) \quad V(0) \rightarrow V(1)$

$V(1) \quad V(1) \rightarrow V(0)$

The truth table is for NAND gate.

So, proved.

Ques:

Prove that the previous ckt works like a -ve logic NOR gate.

Find the minimum value & mode of operation.