AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Department: Computer Science and Engineering

Program: Bachelor of Science in Computer Science and Engineering

Lab Final Examination: Fall 2019

Year: 2nd Semester: 1st

Course Number: CSE 2106

Course Name: Digital Logic Design Lab

Time: 55 minutes Full Marks: 20

1. Write down the correct answers in answer script [5.0]

a. Which gates are easier to fabricate with electronic components?

i. NAND ii. AND iii. OR iv. NOR

b. The 2-input XOR has a high output only when the input values are

i. low ii. high iii. same iv. different

c. Digital circuit can be made by the repeated use of

i. NAND gates
ii. OR gates
iii. NOT gates
iv. None of the above

d. Number of entries in the truth table of a 3 input NAND gate is

i. 3 ii. 6 iii. 8 iv. 9

e. Which is the prohibited state/ condition in S-R latch and needs to be avoided due to unpredictable nature of output?

i. S=0, R=0 ii. S=1, R=0
iii. S=0, R=1 iv. S=1, R=1

2. What is a binary parallel adder? [1.5]

3. Define a shift register. [1.5]

4. Implement the following Boolean function using only one multiplexer (IC 74151), [12.0] F (A, B, C, D) = ∑ (1, 2, 5, 8, 10, 13).