
# Ahsanullah University of Science & Technology

## Department of Computer Science & Engineering

**Course No** : CSE3110
**Course Title** : Digital System Design Lab
**Assignment No** : 03

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## Introduction:

SAP-I refers to "Simple As Possible" computer which is a basic model of a microprocessor. This contains the basic registers for a functional microprocessor. SAP-I is known as the first stage in the evolution towards modern computers explained by Albert Paul Malvins. It is a bus organised computer which covers many advanced concepts along being a simple computer. Primary purpose of SAP is to develop a basic understanding of how a microprocessor works and interacts with memory and other parts of the system like input and output. SAP-I contains a number of instruction set which is given through a hex file. Here all registers are connected to the BUS with the help of tri-state buffer.

**Problem Statement:** Implementation of SAP-I.

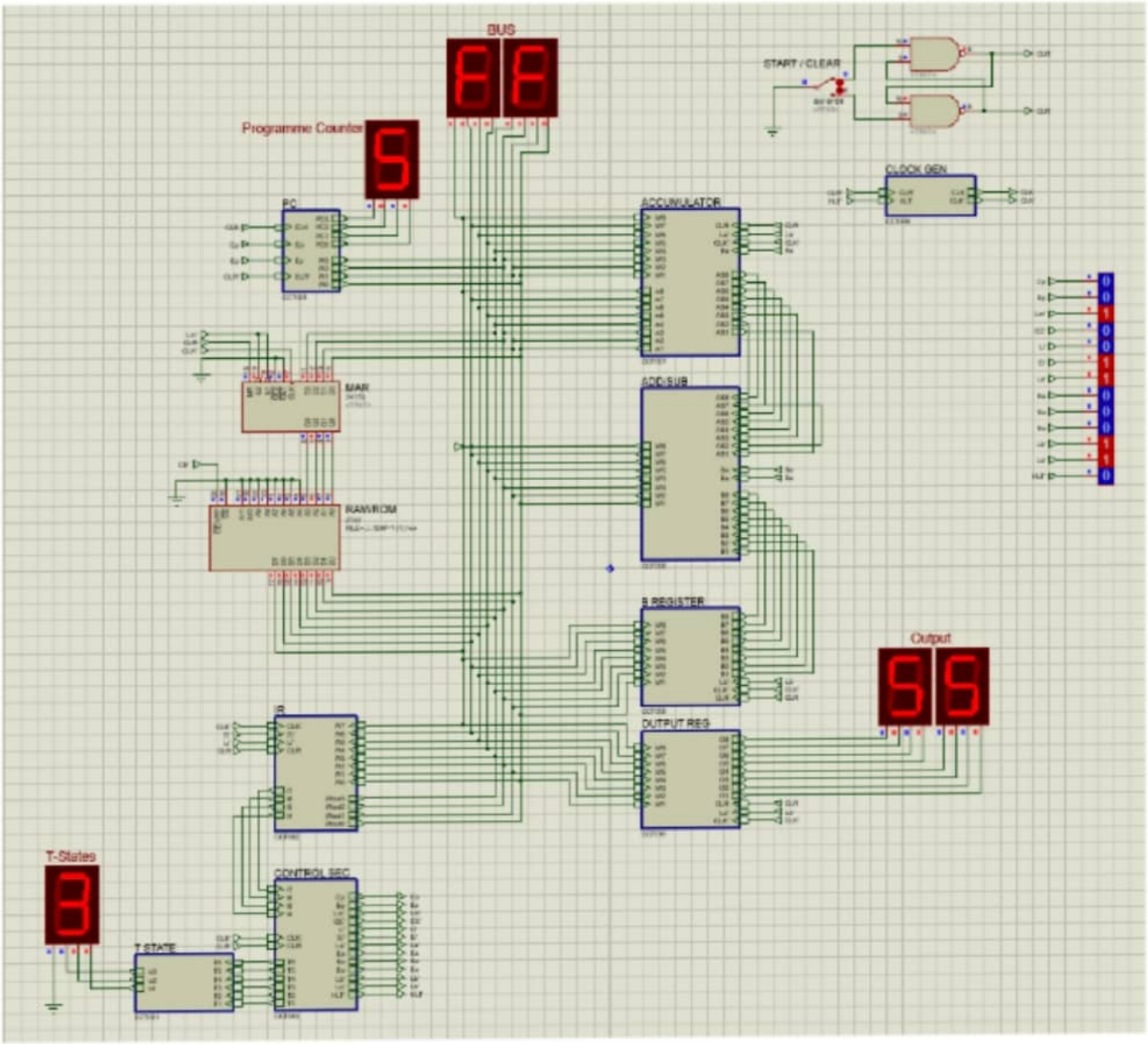
## Function Generation :

| Program in Assembly | | Machine Code |
|---|---|---|
| Address | Code | in Hex |
| 0H | LDA 6H | 06 |
| 1H | ADD 5H | 15 |
| 2H | SUB 7H | 27 |
| 3H | OUT | EF |
| 4H | HLT | FF |
| 5H | 22H | 22 |
| 6H | 66H | 66 |
| 7H | 33H | 33 |
| 8H | FFH | FF |
| 9H | FFH | FF |
| AH | FFH | FF |
| BH | FFH | FF |
| CH | FFH | FF |
| DH | FFH | FF |
| EH | FFH | FF |
| FH | FFH | FF |

Equipment and Budget:

| IC Numbers | Quantity | Amount (Tk) | |
|---|---|---|---|
| 74LS04 | 1 | 25 | |
| 74LS00 | 1 | 25 | |
| 74LS83 | 1 | 120 | |
| 74LS21 | 1 | 25 | |
| 74LS86 | 1 | 25 | |
| 74LS13 | 1 | 25 | |
| 74LS173 | 1 | 30 | |
| 74LS107 | 1 | 50 | |
| 74LS10 | 1 | 20 | |
| 7483 | 1 | 45 | |
| 4081 | 1 | 28 | |
| 4071 | 1 | 20 | |
| 4030 | 1 | 20 | |
| 4073 | 1 | 24 | |
| 2732 | 1 | 26 | |
| CLOCK | 1 | 45 | |
| LOGIC PROBE (BIG) | 1 | 35 | |
| LOGIC TOGGLE | 1 | 30 | |
| SW-SPDT | 1 | 28 | |
| NOT | 1 | 30 | |
| TRIBUFFER | 1 | 30 | |
| BUFFER-8 | 1 | 30 | |
| | Total = | 736 Tk | |

# Simulation:


BUS
Programme Counter
START / CLEAR
CLOCK GEN
PC
ACCUMULATOR
MAR
ADD/SUB
RAM/ROM
B REGISTER
Output
IR
OUTPUT REG
T-States
CONTROL SEC
T STATE

Result :

| Contents | Accumulator | OUTPUT |
|---|---|---|
| LDA 6H | 66H | 00H |
| ADD 5H | 88H | 00H |
| SUB 7H | 55H | 00H |
| OUT | 55H | 55H |
| HLT | 55H | 55H |

Output :

The output of the above input will be 55H.

## Conclusion :-

In this experiment we have implemented SAP-1 through proteous simulation. SAP-1 has both advantages and as well as some drawbacks. This architecture is based on 8 bits data manupulation and comprised with 16 x 8 memory, 16 memory locations which can held an 8 bit address.

The major drawback is that we can only stone 5 instructions in the memory for the executed program. The experiment was conducted under the supervisation of two teachers. And instrumental error is almost zero since it's being simulated through softwere.