CSE2209: Digital Electronics and Pulse Techniques

Course Conducted By:

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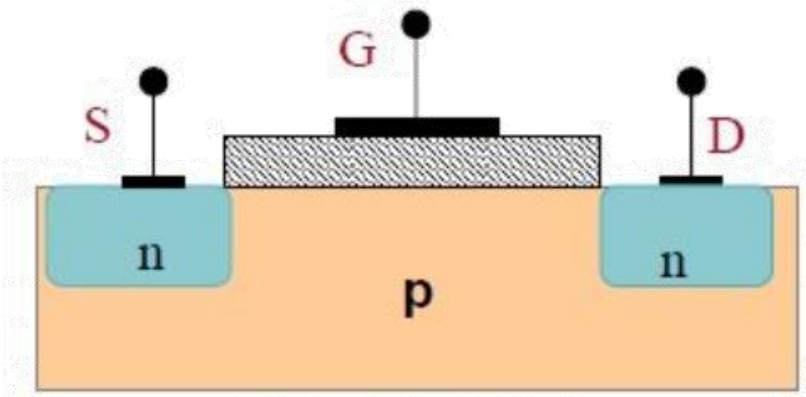
Chapter 8

Field Effect Transistors

MOSFET (Metal-Oxide-Semiconductor Field-effect Transistor)

A metal–oxide–semiconductor field-effect transistor (MOSFET) is a field-effect transistor (FET) with an insulated gate, where the voltage determines the conductivity of the device. It is used for switching or amplifying signals.

- S: Source
- G: Gate
- D: Drain
- Body: Substrate



MOSFET Structure

Classification of MOSFET

- The one way of classifying MOSFETs is depending upon the type of channel. Namely n-channel and p-channel shortly called as NMOS and PMOS respectively.

- The another way of classifying the MOSFETs is depending upon the availability of channel between source and drain terminals i.e. Enhancement mode MOSFETs and depletion mode MOSFETs.

MOSFET device types

Thus, there are four basic MOSFET device types there are :

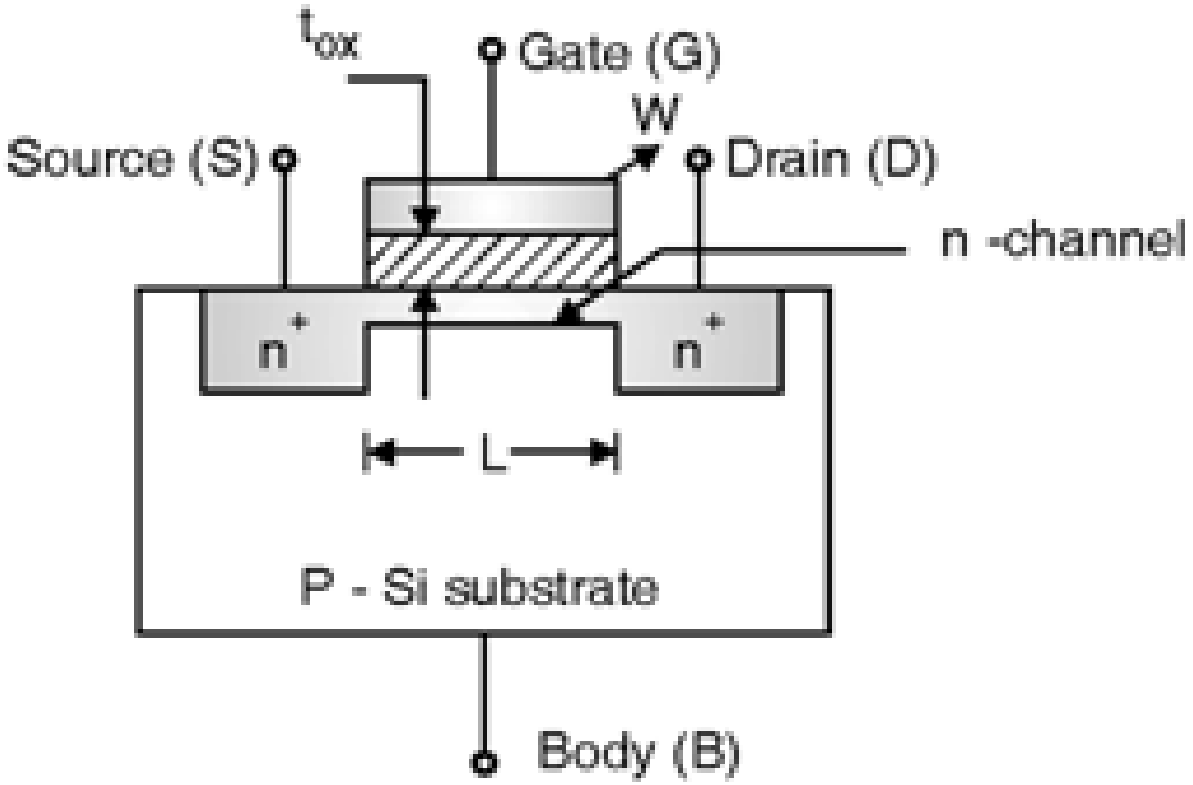
1) n-channel enhancement mode MOSFET

2) n-channel depletion mode MOSFET

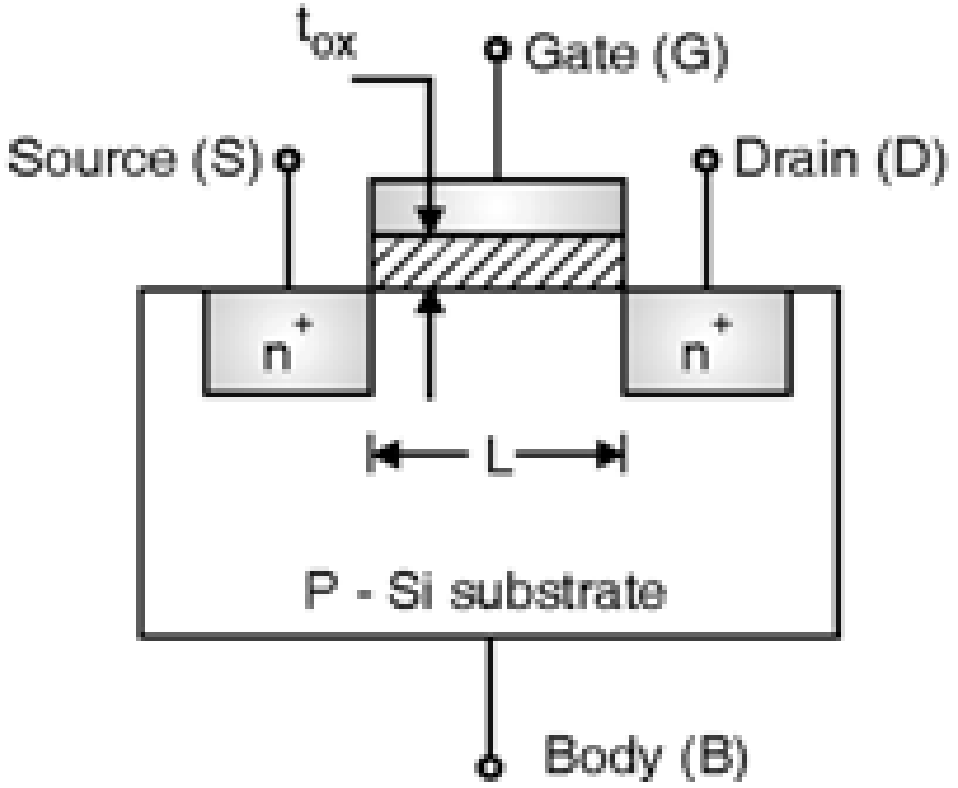
3) p-channel enhancement mode MOSFET

4) p-channel depletion mode MOSFET.

n-channel Depletion and Enhancement mode

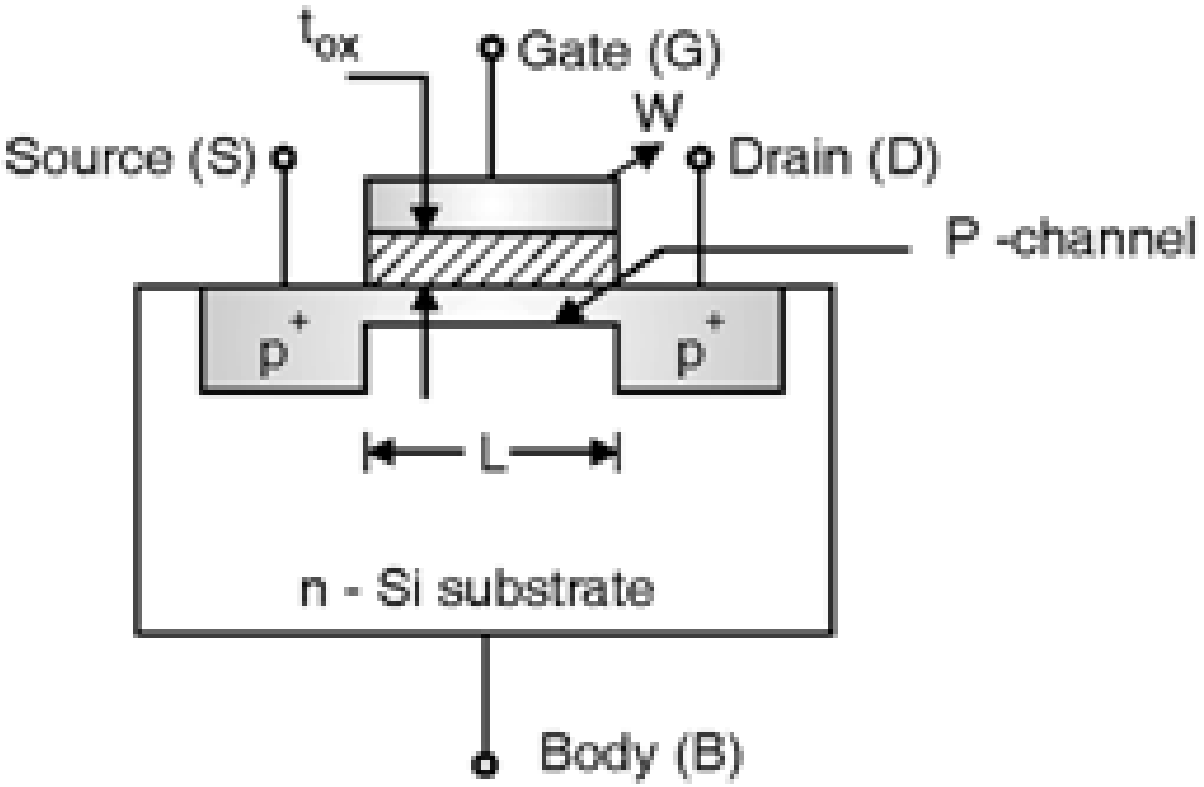


Depletion Mode

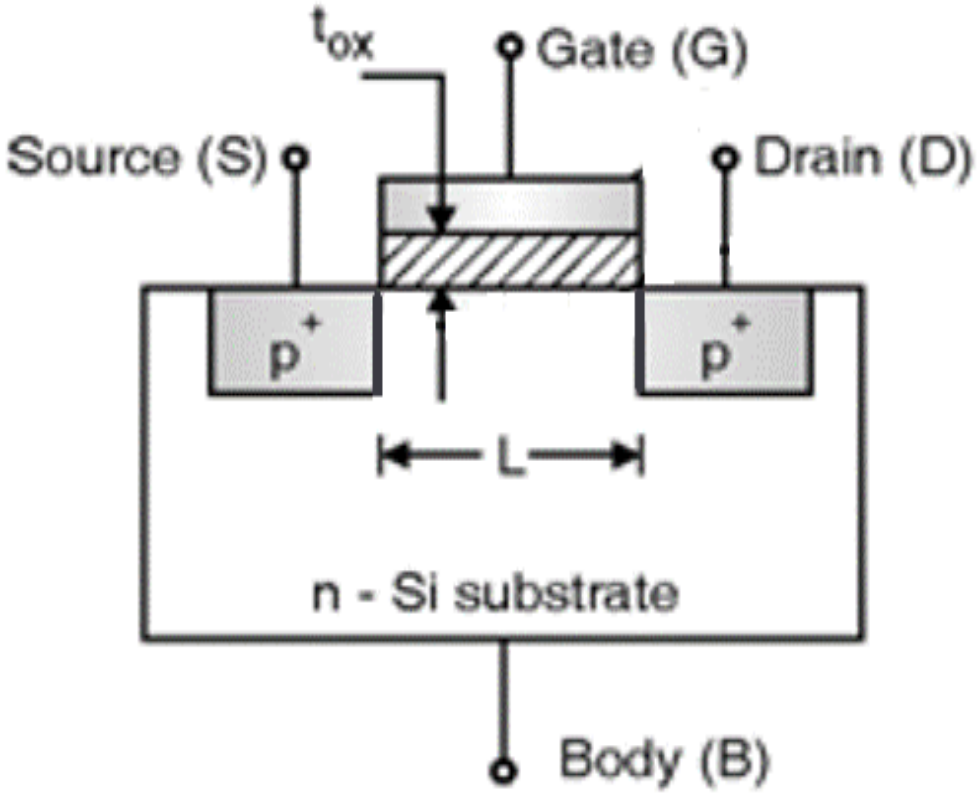


Enhancement Mode

p-channel Depletion and Enhancement mode



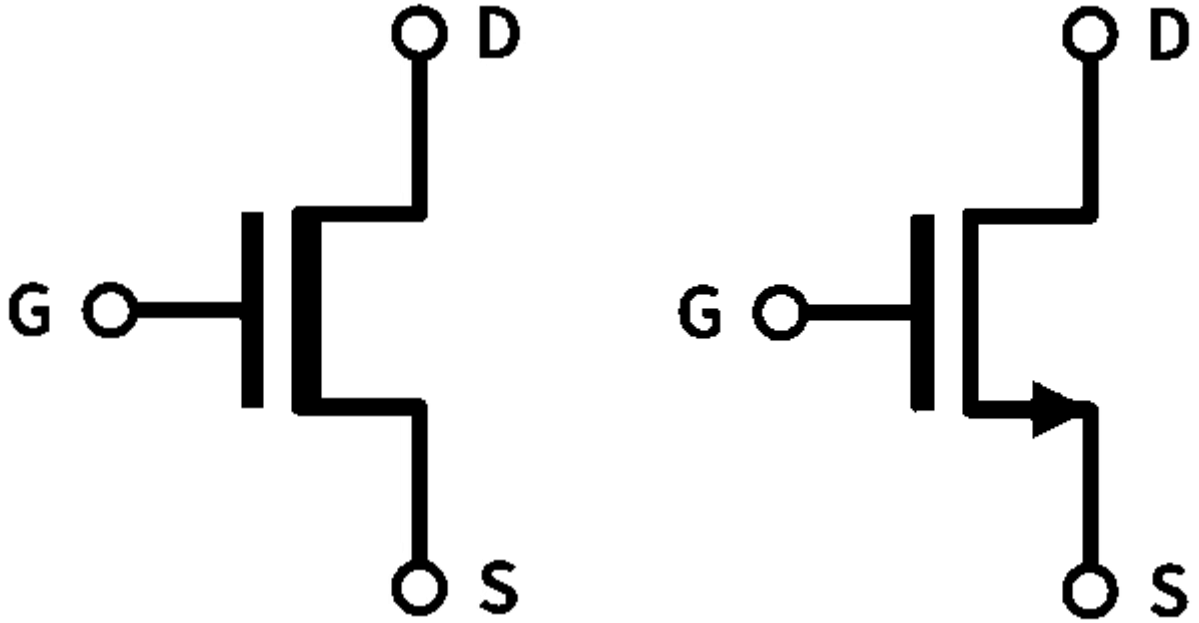
Depletion Mode



Enhancement Mode

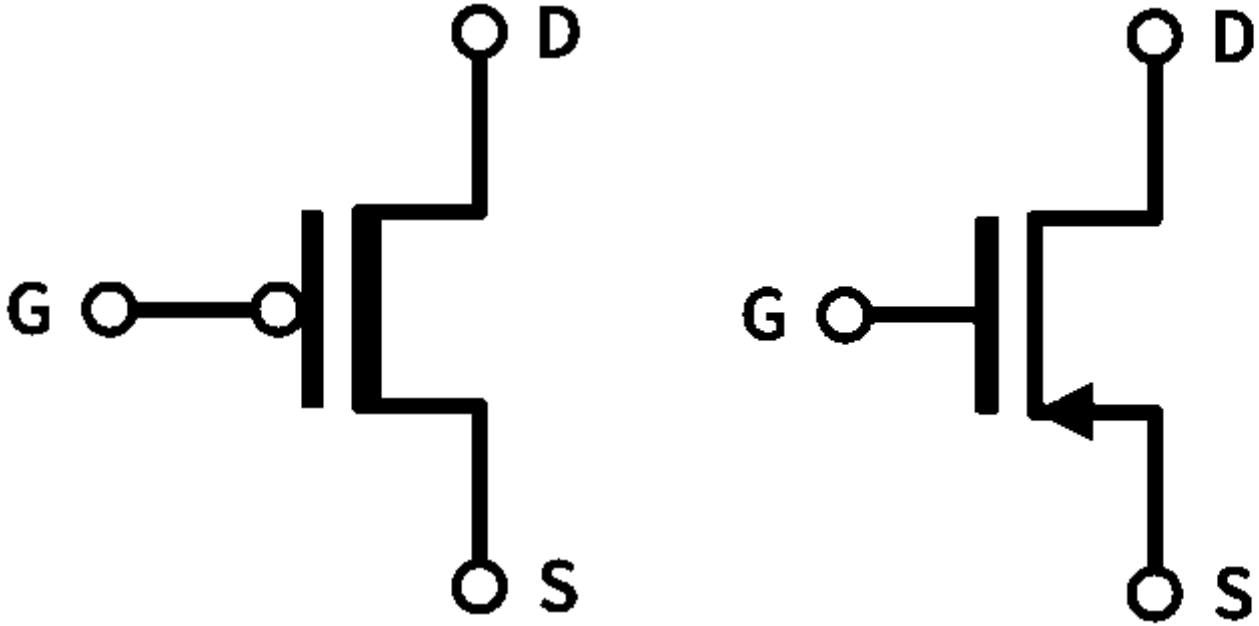
NMOS in enhancement mode

G = High, D-S short
G = Low, D-S open



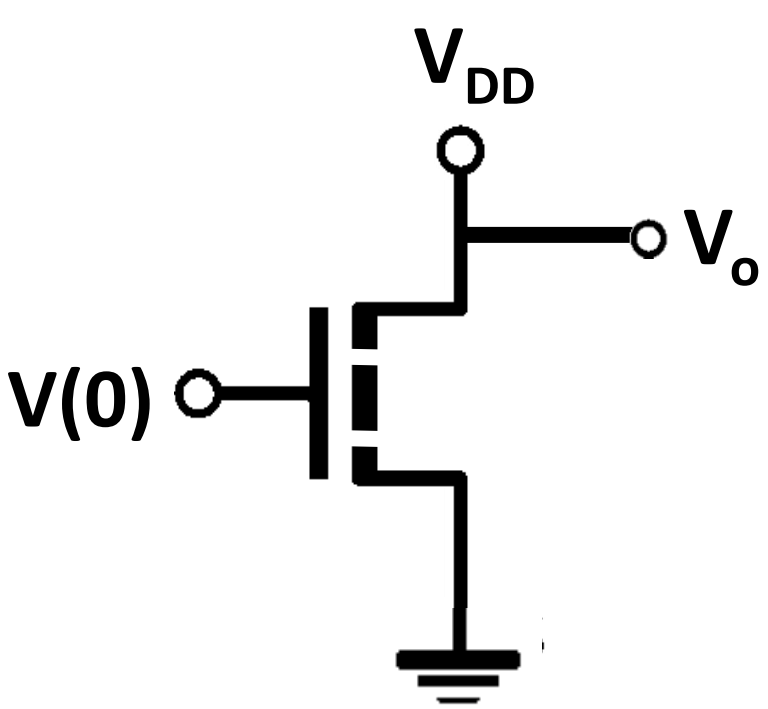
PMOS in depletion mode

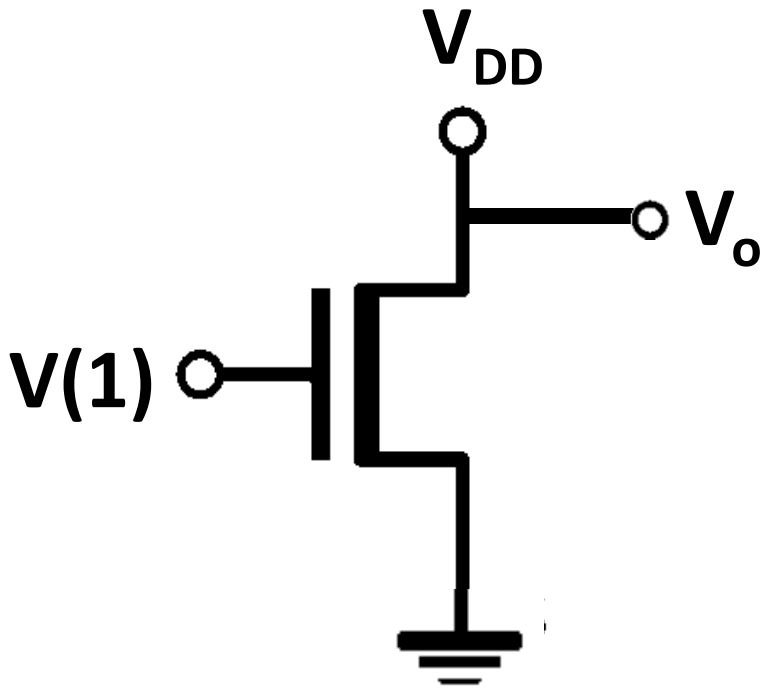
G = High, D-S open
G = Low, D-S short



NMOS Inverters

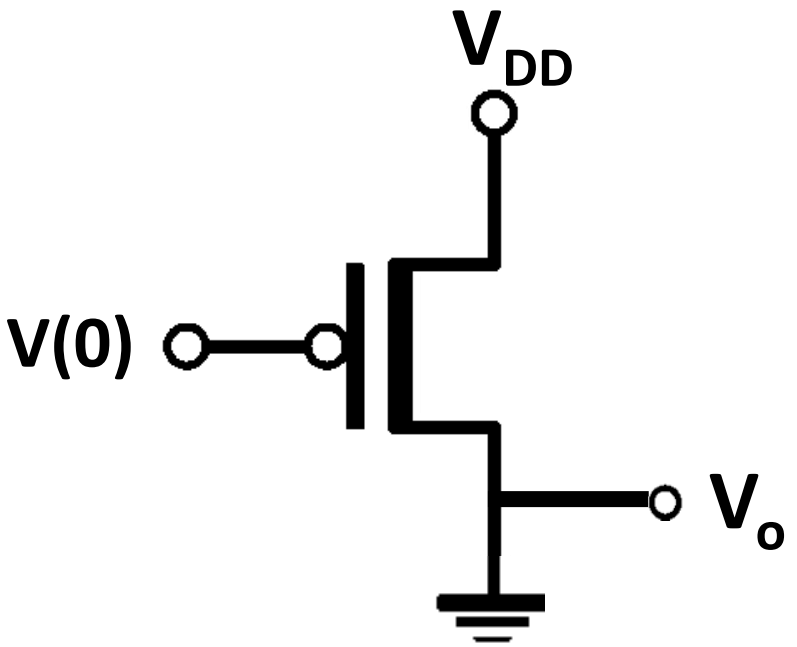
V_i	NMOS	V_o
V(0)	OFF	V_{DD}
V(1)	ON	GND

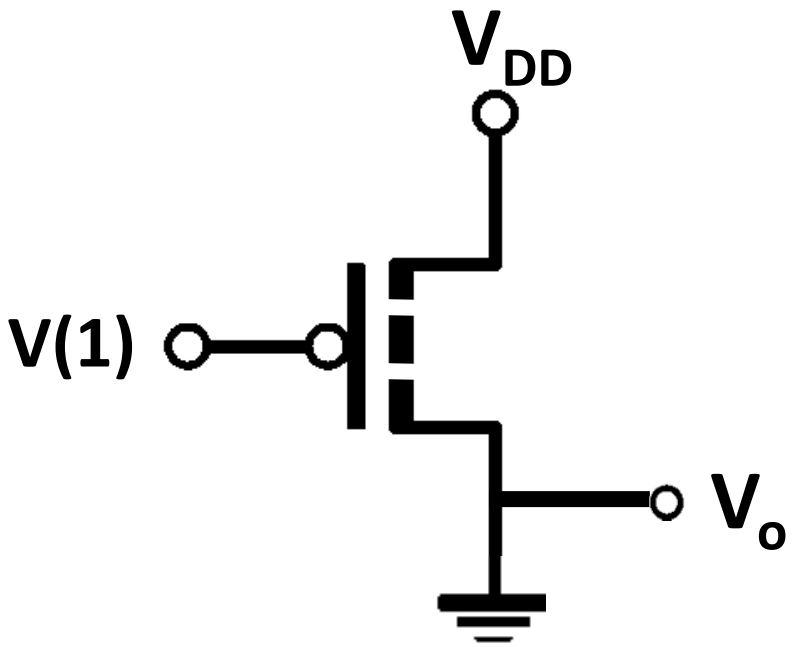




PMOS Inverters

V_i	PMOS	V_o
V(0)	ON	V_{DD}
V(1)	OFF	GND

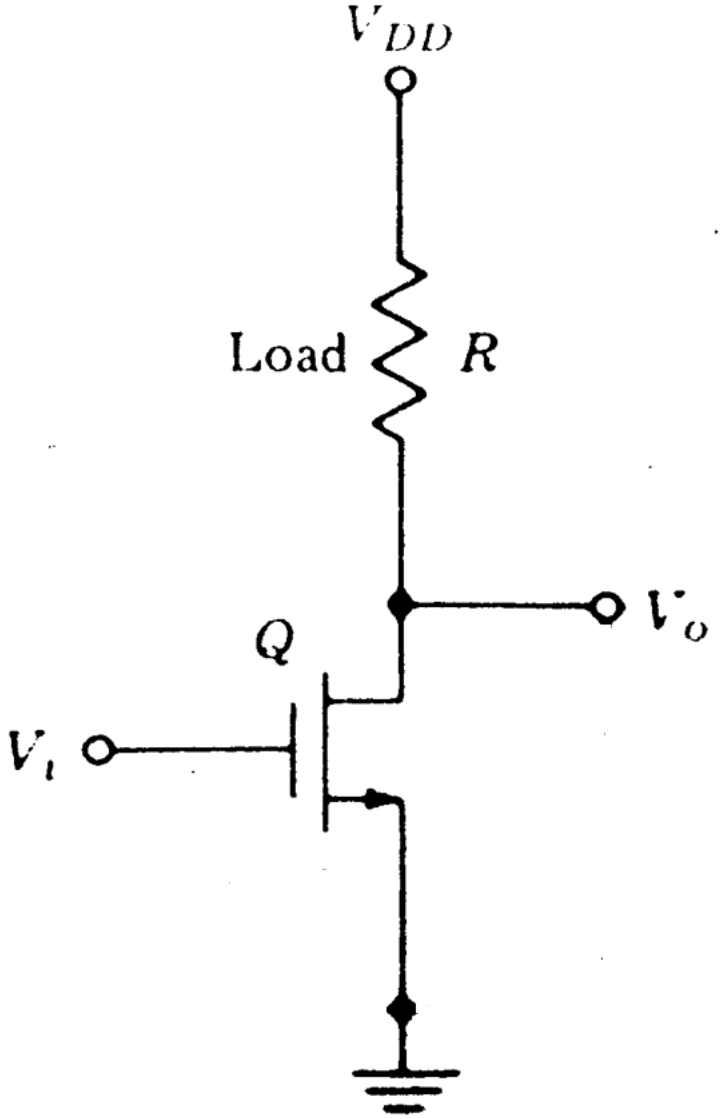


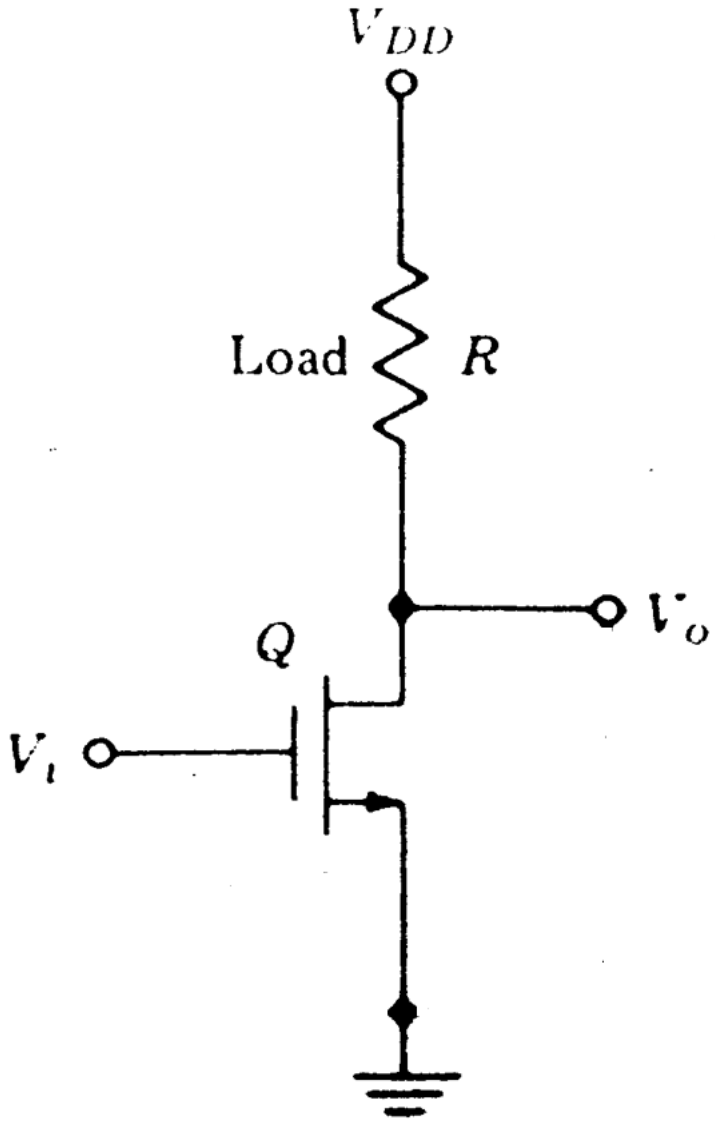


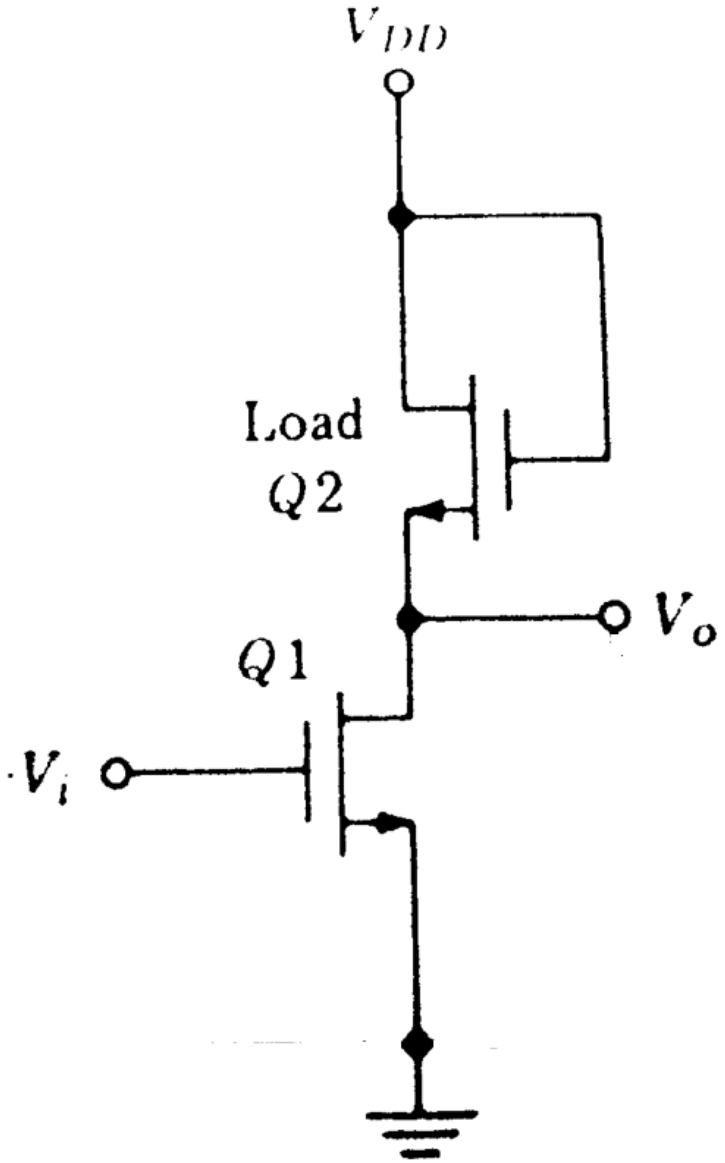
Logic Gates Using MOSFET

NOT Gate using NMOS

- Here R is used to control the current flow.
- When V_i = low,
  then Q will be open and $V_0 = V_{DD}$
- When V_i = high,
  then Q will be short and V_0 = GND

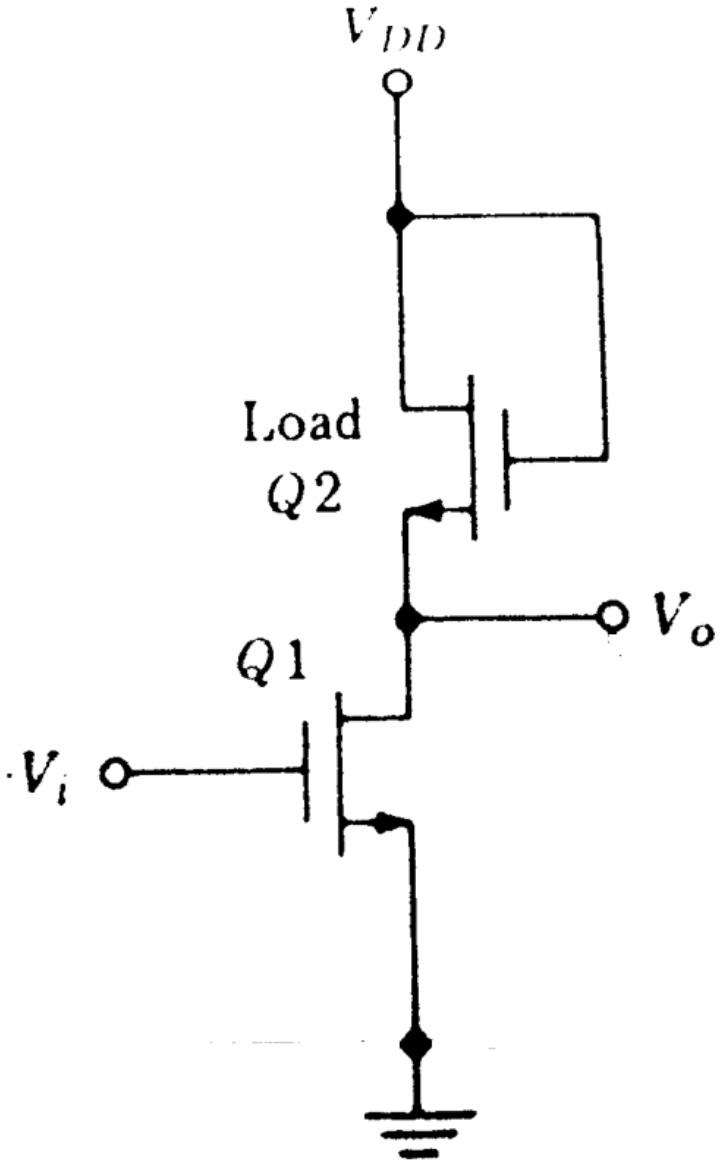



V_{DD}
Load
R
V_o
Q
V_i


V_{DD}
Load
$Q2$
V_o
$Q1$
V_i

NOT Gate using NMOS

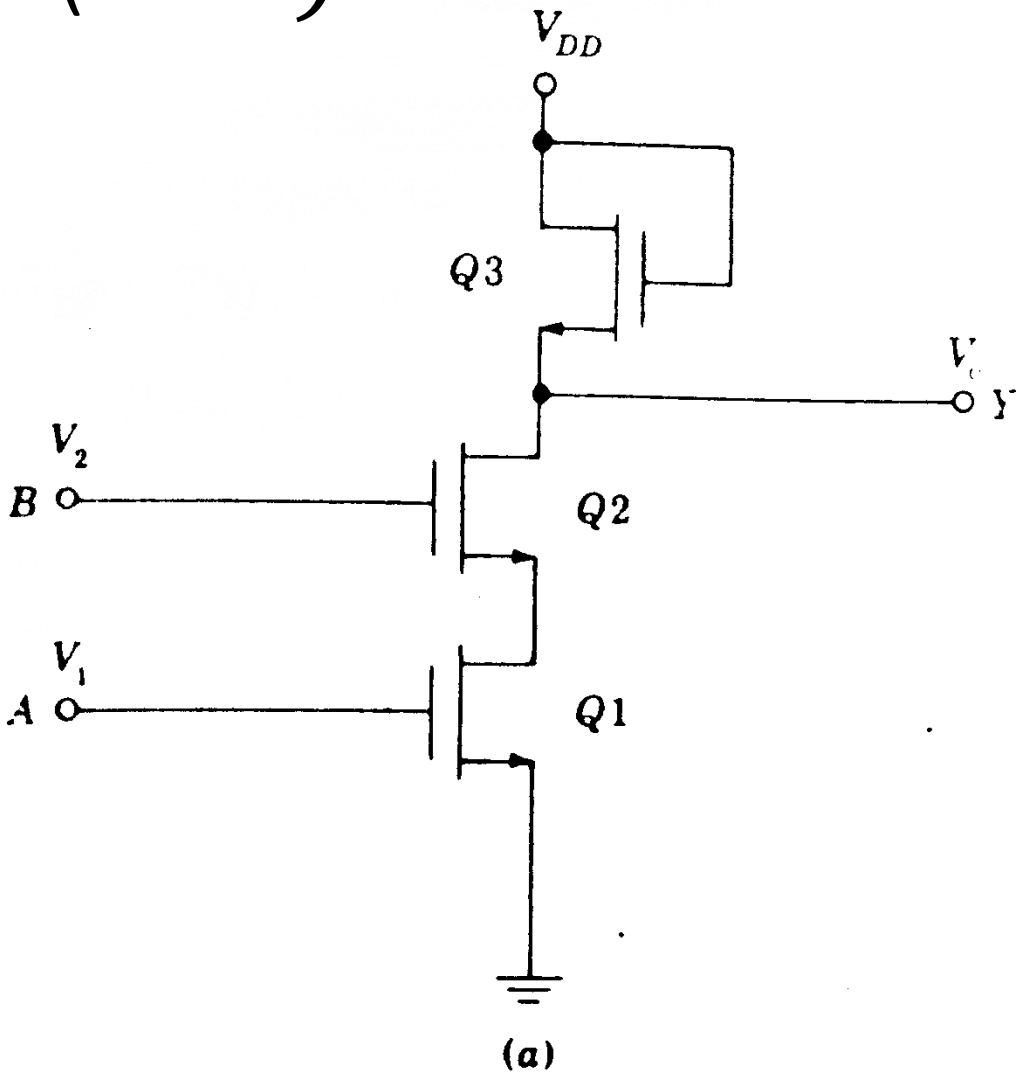
- Q2 used instead of load.Q2 is always high as Gate is directly connected to Vcc.
- When V_i = low,
  then Q will be open and $V_0 = V_{DD}$
- When V_i = high,
  then Q will be short and V_0 = GND



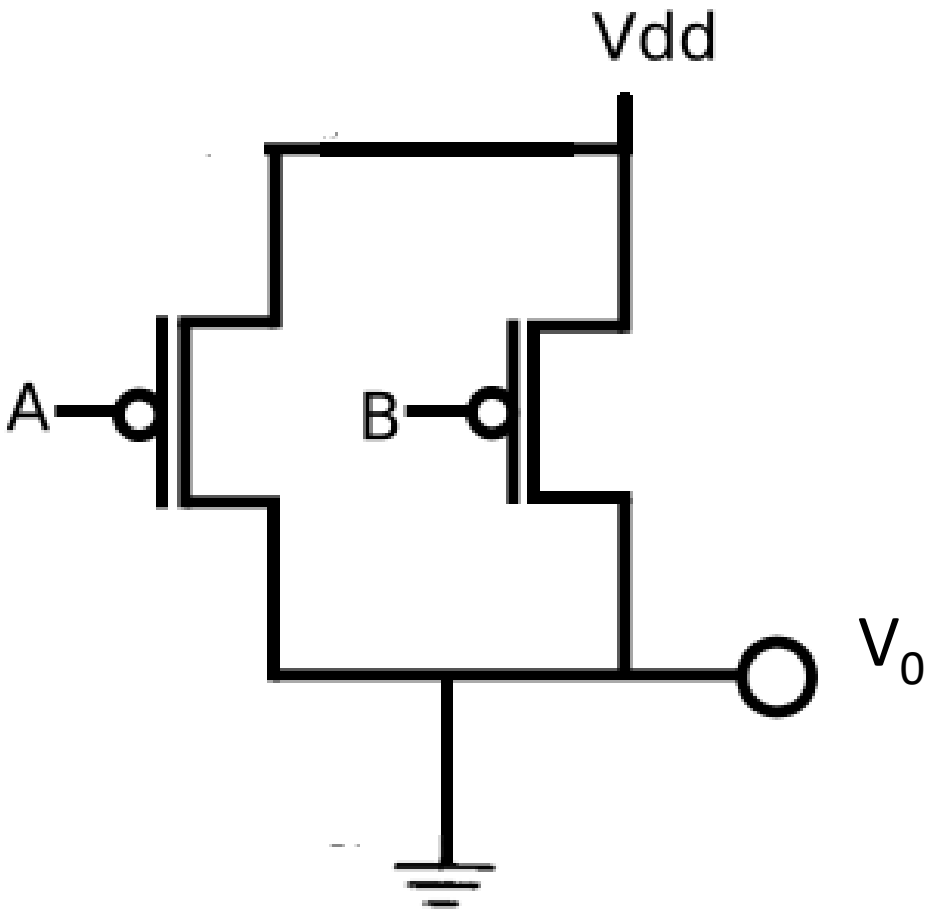
NAND Gate using NMOS ($\overline{AB}$)

A	B	Y
V_1	V_2	V_0
0	0	V_{DD}
0	V_{DD}	V_{DD}
V_{DD}	0	V_{DD}
V_{DD}	V_{DD}	0

$Y = \overline{AB}$



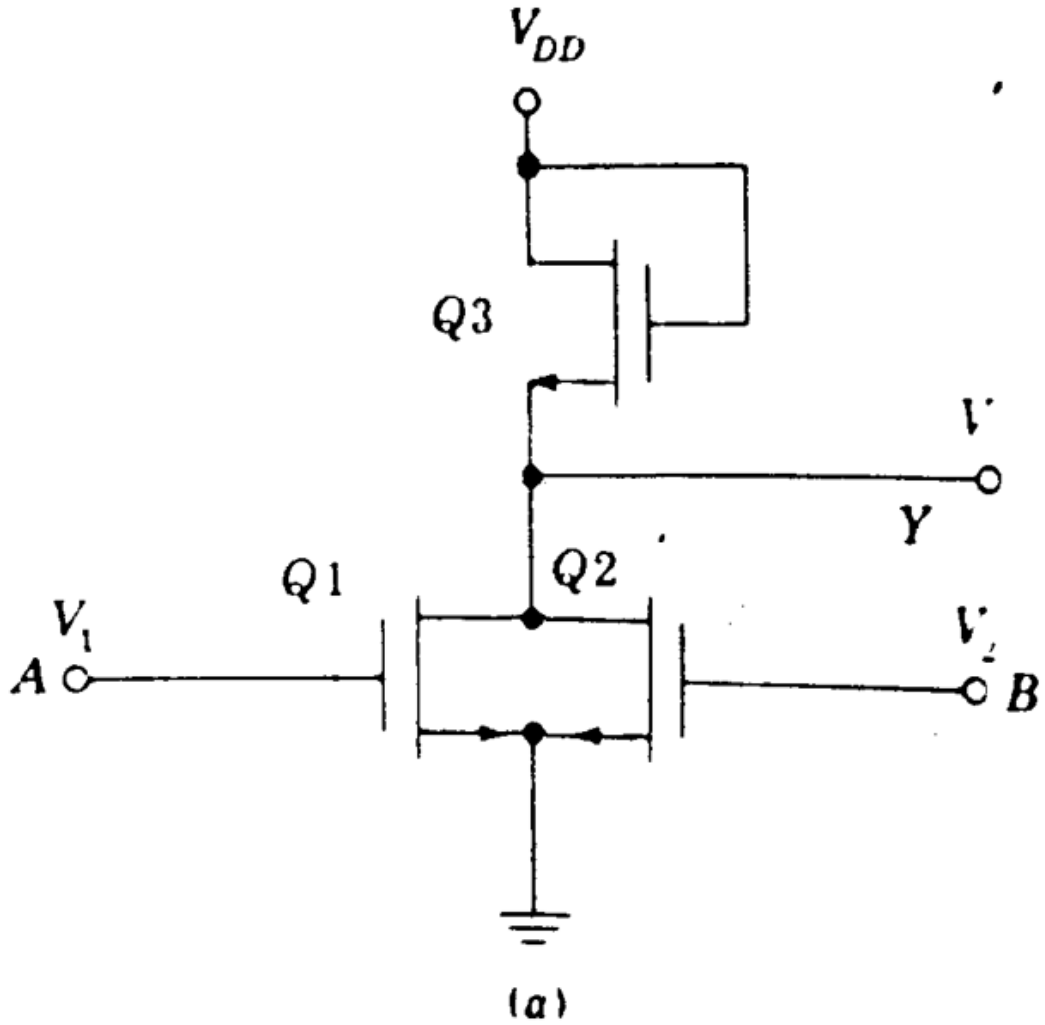
NAND Gate using PMOS ($\overline{AB}$)



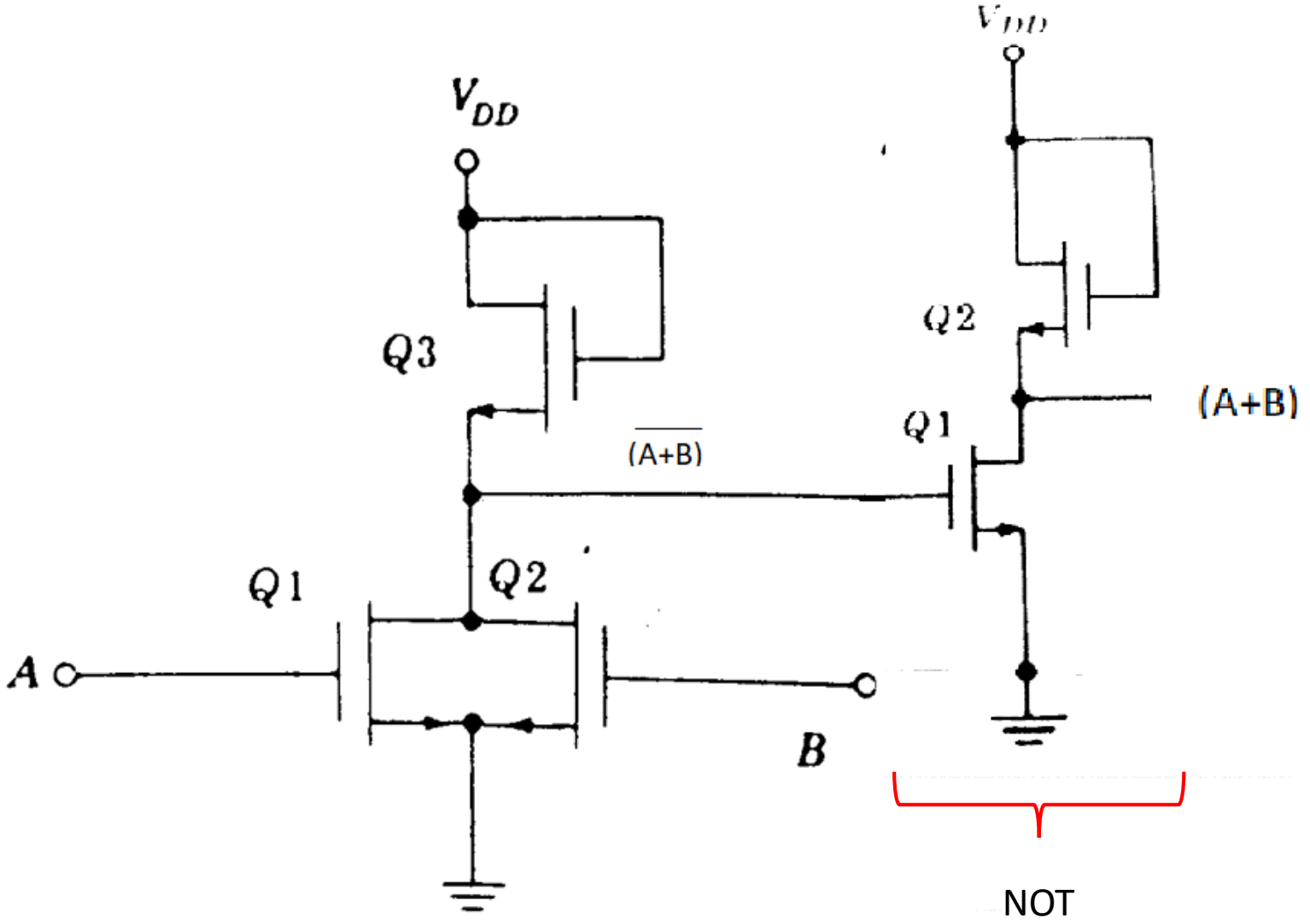
NOR Gate using NMOS ($\overline{A + B}$)

A	B	Y
V_1	V_2	V_o
0	0	V_{DD}
0	V_{DD}	0
V_{DD}	0	0
V_{DD}	V_{DD}	0

$$Y = \overline{A + B}$$



OR Gate using NMOS $(A + B)$



Draw Circuits using NMOS

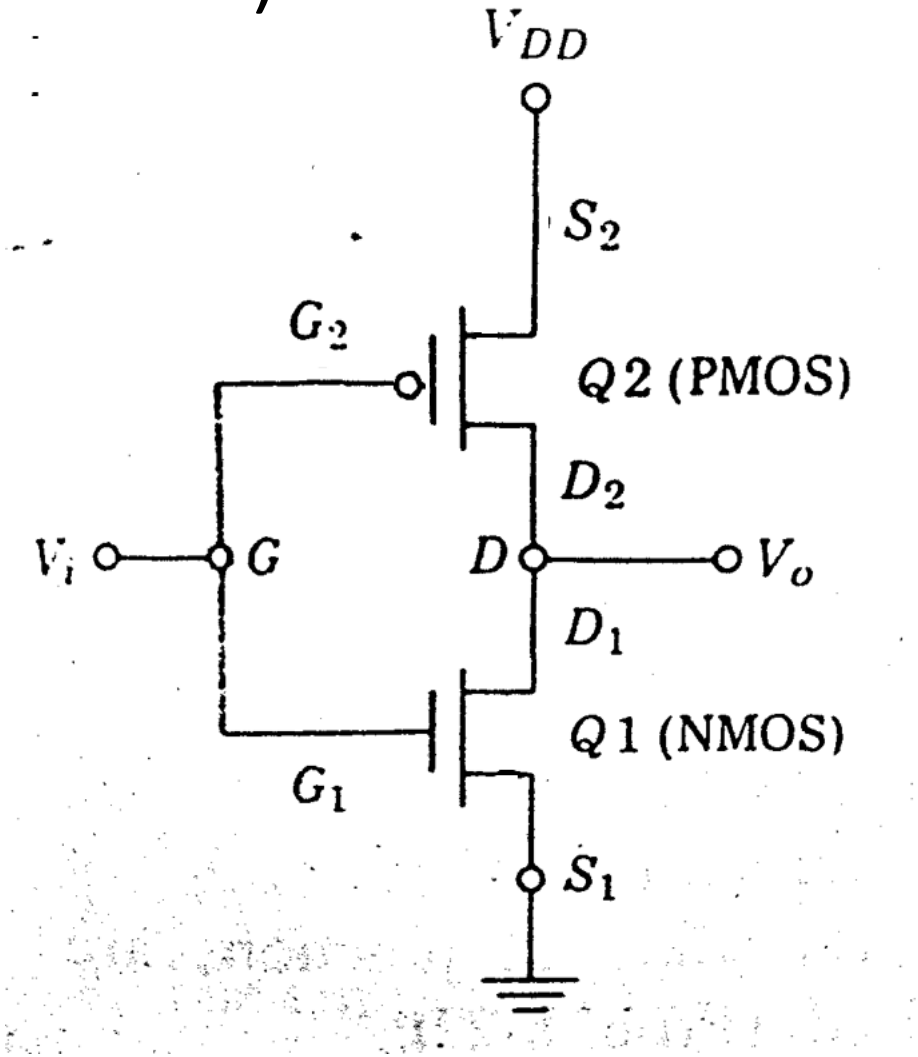
1) F = A+B
2) F= A+BC
3) F= AB + CD
4) F= $A \cdot (\overline{B + C})$
5) F = $\bar{A} \cdot (\overline{B + C})$
6) F = $(\bar{A} + B)(A + \bar{B}) + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D} + \overline{(C + \bar{E})}$

CMOS (Complementary MOSFET)

It is possible to construct p-channel and n-channel enhancement MOS devices on the same chip. Such devices are called complementary MOSFETs or CMOS.

The circuit given here works as a CMOS inverter.

The driver is transistor Q_1 and Q_2 acts as the load.

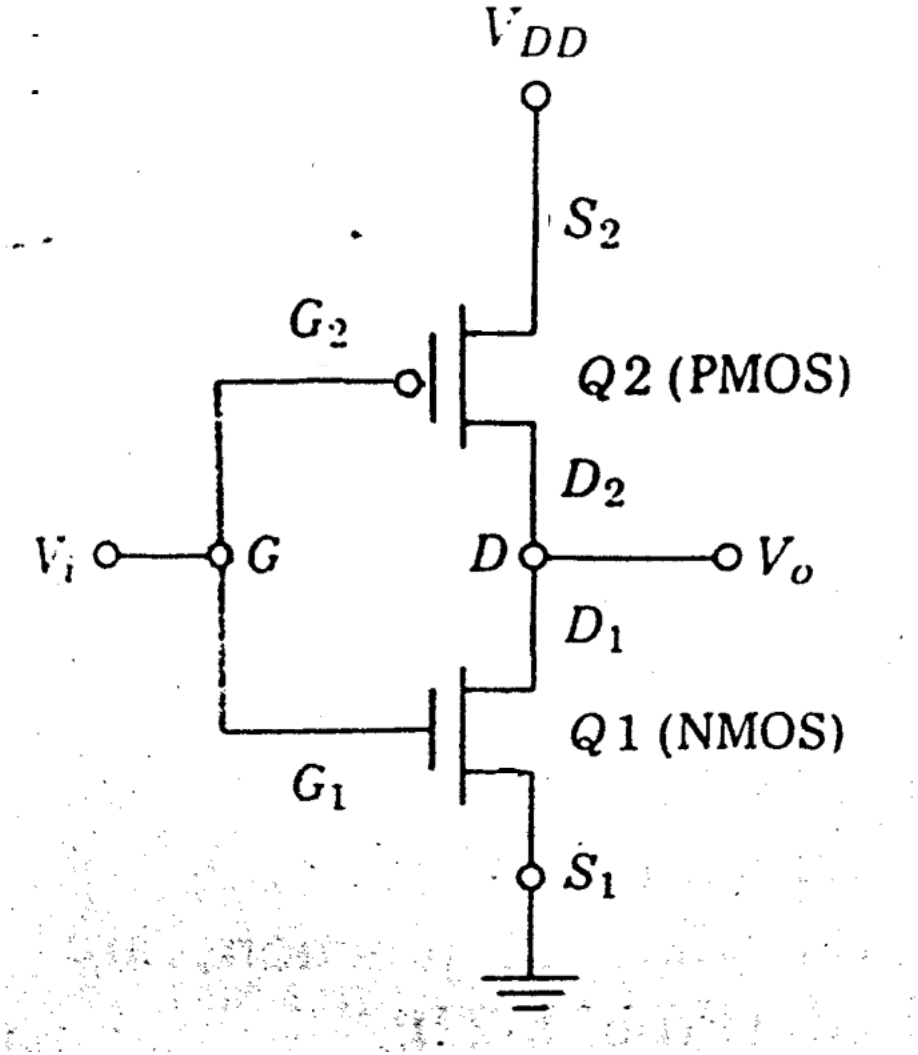


CMOS

- V_i = V(0), then
  PMOS = short, NMOS = open
  $V_o = V_{DD}$ = V(1)

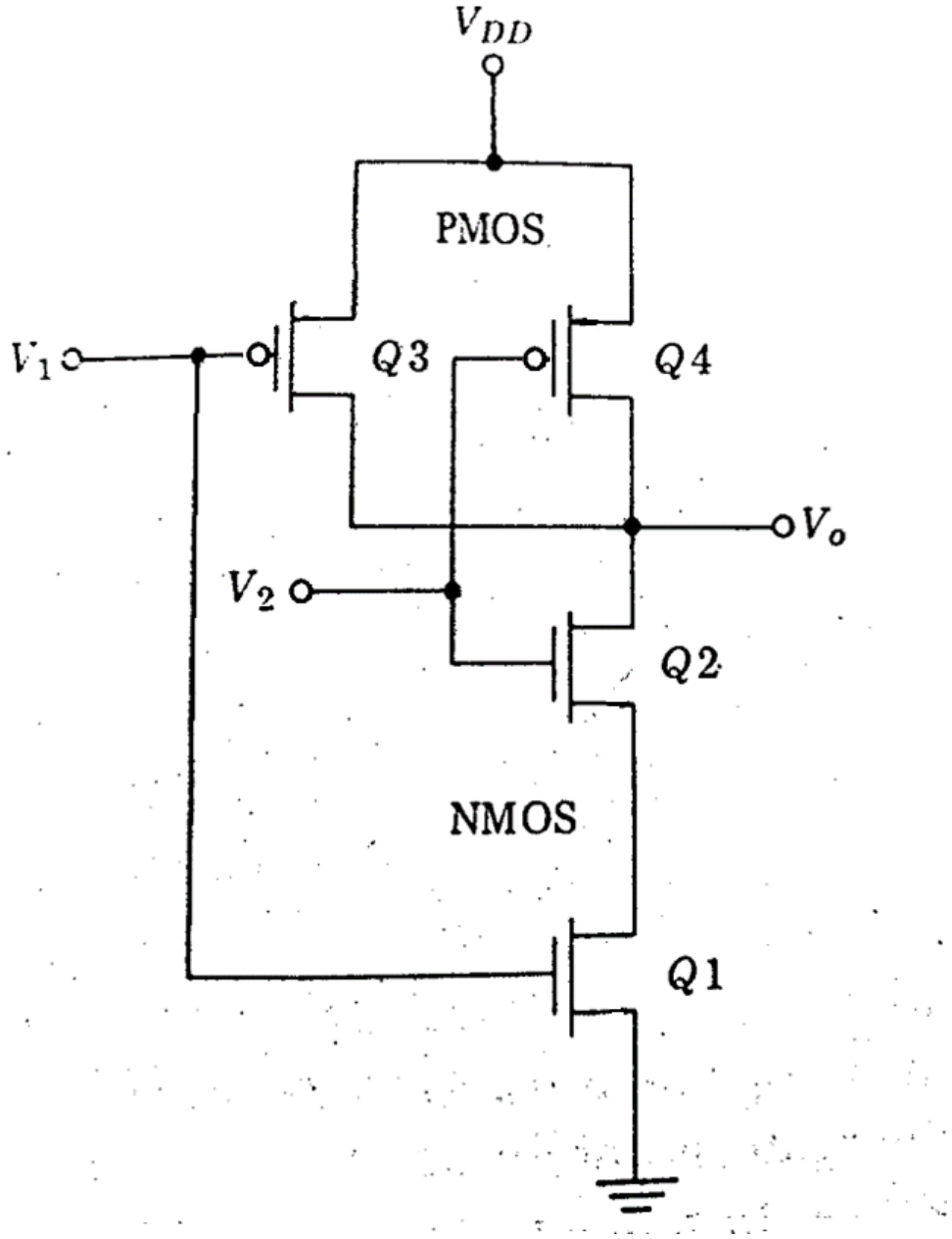
- V_i = V(1), then
  PMOS = open, NMOS = short
  V_o = GND = V(0)

V_i	V_o
Low	V_{DD}
High	GND



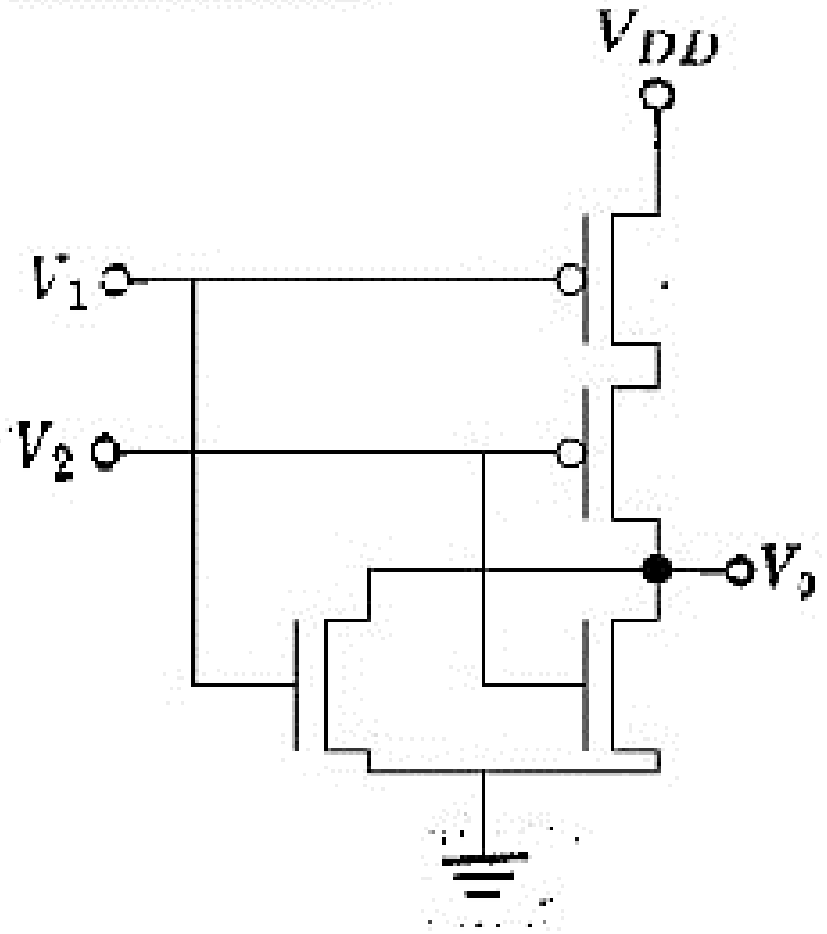
CMOS NAND

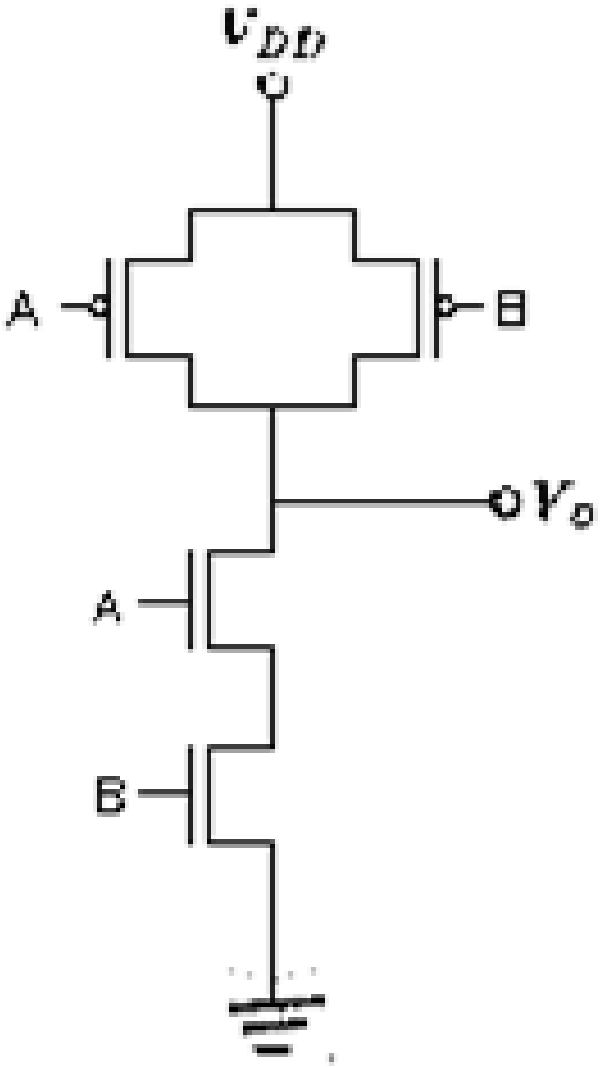
V_1	V_2	V_o
0	0	1
0	1	1
1	0	1
1	1	0



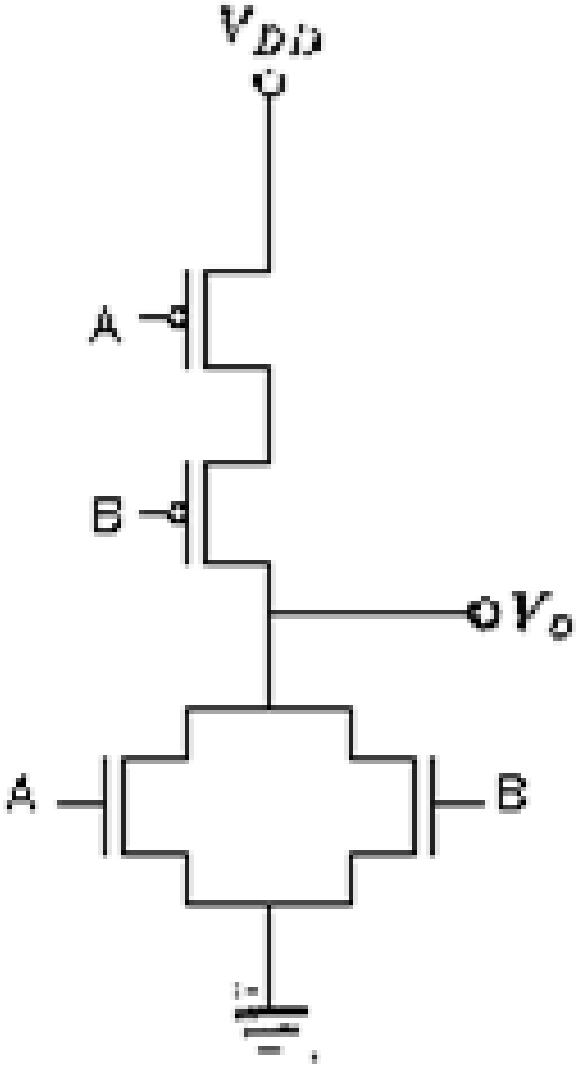
CMOS NOR

V_1	V_2	V_o
0	0	1
0	1	0
1	0	0
1	1	0





NAND



NOR

Draw Circuits using CMOS

1) F = A+B
2) F= A+BC
3) F= AB + CD
4) F= $A \cdot (\overline{B + C})$
5) F = $\bar{A} \cdot (\overline{B + C})$

Properties/Advantages of CMOS

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pg. 265

CMOS Properties

The desirable features of CMOS gates are the following.

1. The quiescent (static) power dissipation is extremely small (a few nanowatts). Appreciable power is absorbed only when switching from one state to the other. At 1-MHz switching rate the dynamic power increases to a few milliwatts in a 50-pF load (about the same as in a Schottky low-power gate).
2. The noise immunity is better than 40 percent of V_{DD}. Note that, for $V_{DD} = 10$ V in the inverter transmission characteristic of Fig. 8-26*b*, a noise voltage of 4V superimposed upon $V(0) = 0$ reduces the output from $V(1) = 10$ V by only a fraction of a volt.
3. Propagation delay is about 50 ns per gate, allowing 10-MHz clock rates. Hence, CMOS is faster than MOS but slower than TTL logic.
4. The fan-out is very high, in excess of 50.
5. The logic swing is V_{DD}, independent of the fan-out.
6. A single power supply is required, and it can be a simple and inexpensive system (because of the small standby current).
7. If $V_{DD} = 5$ V, then CMOS is TTL compatible.
8. The temperature stability is excellent (Fig. 8-26*b*).

The above advantages are offset by the increased cost because of the additional processing steps required. Also the density of gates for a given chip area is decreased since CMOS requires that PMOS and NMOS devices appear in pairs. For example,[16] a four-input NAND gate requires about 50 mil^2 for CMOS, 30 mil^2 for TTL (low power, Schottky), 11 mil^2 for PMOS, and 5.6 mil^2 for I^2L (Sec. 9-13).

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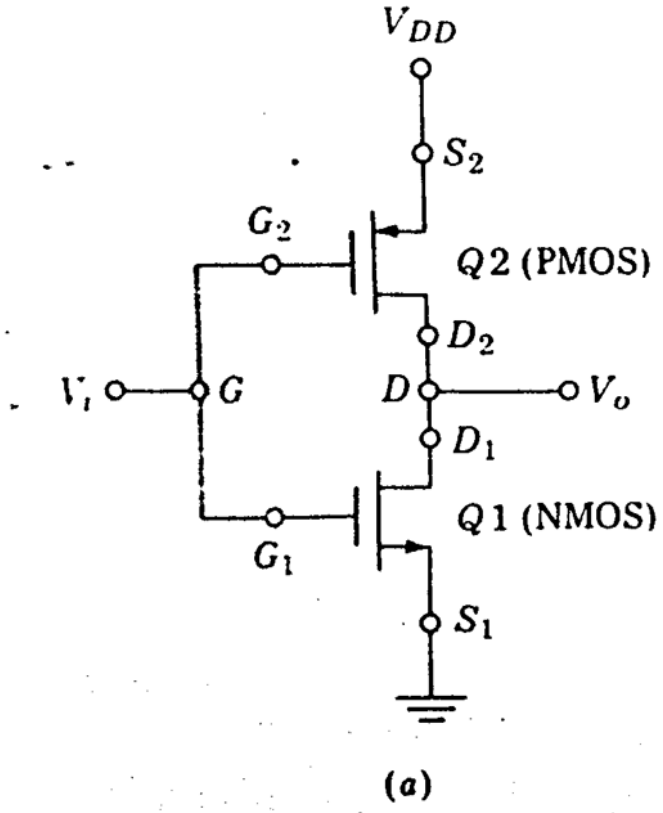
pg. 263
Reference of the Figure 8.26(b)

These diagrams are only for reference.
No need to draw in the Exam.



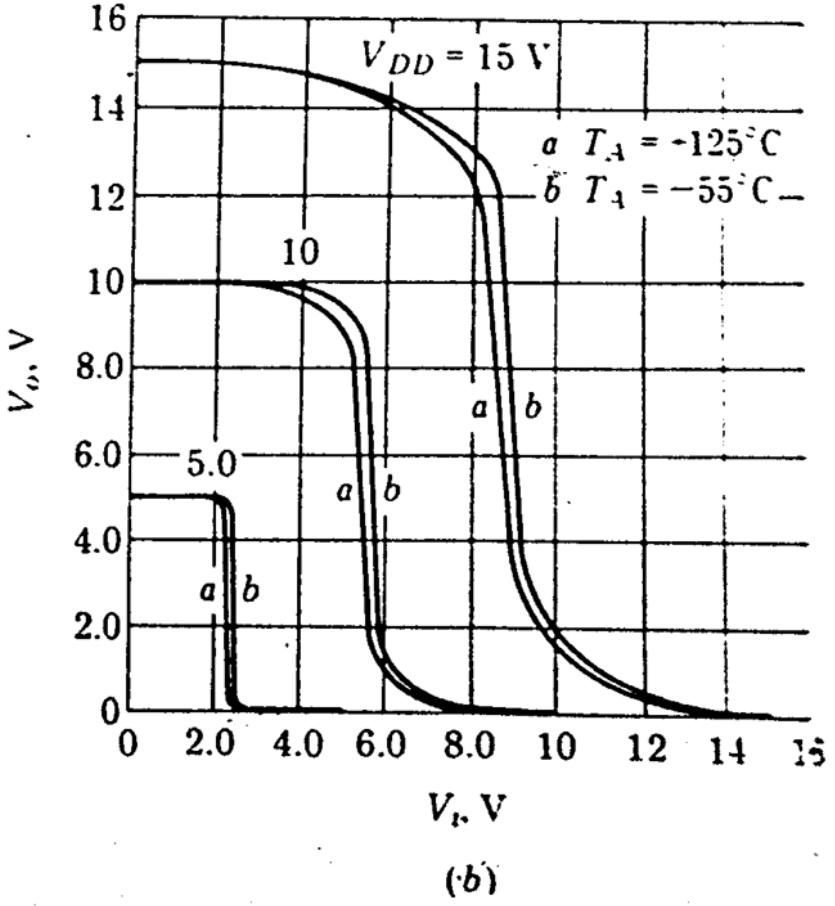


Figure 8-26 (*a*) Complementary MOS inverter. (*b*) The transfer characteristics for three values of V_{DD} and two values of temperature. *(Courtesy of Motorola Semiconductor Products, Inc.)*