CSE2209: Digital Electronics and Pulse Techniques

Course Conducted By:

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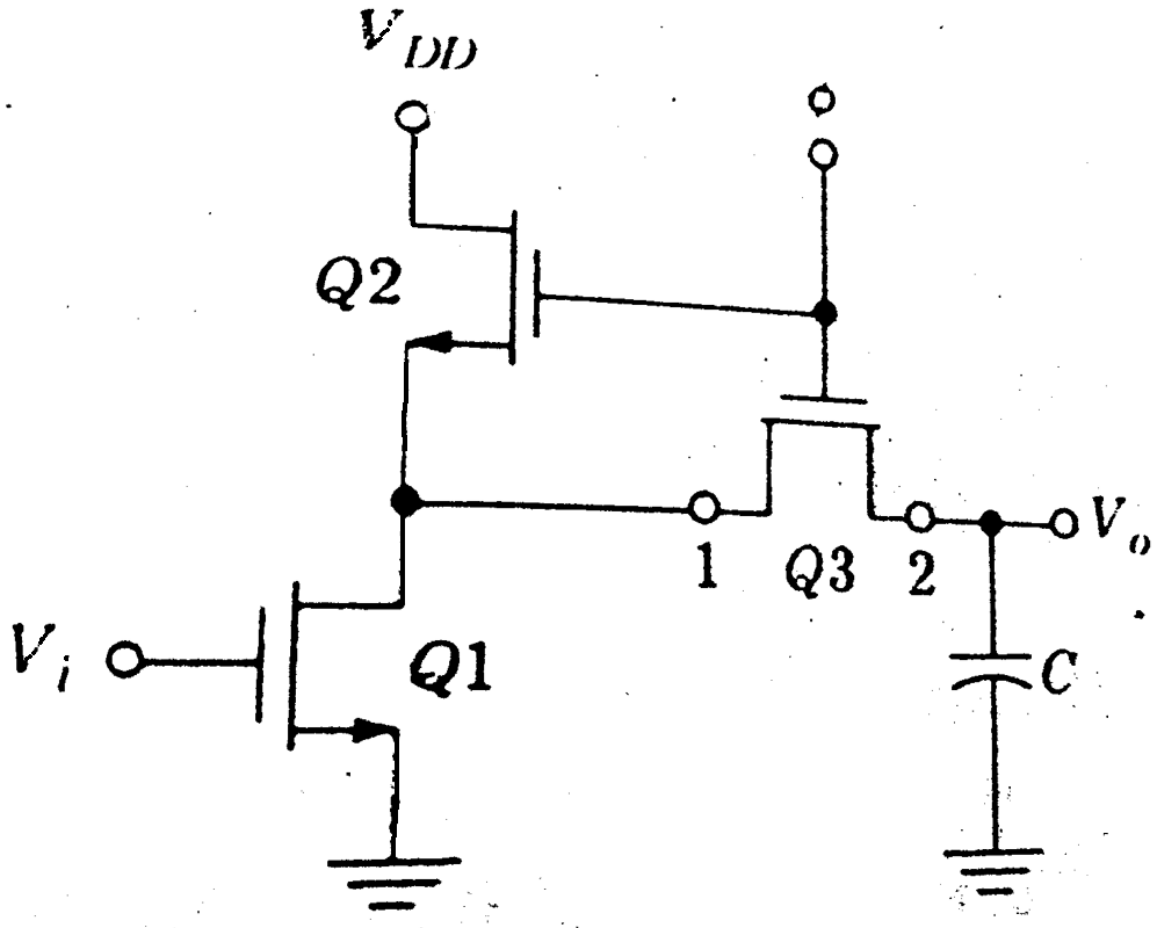
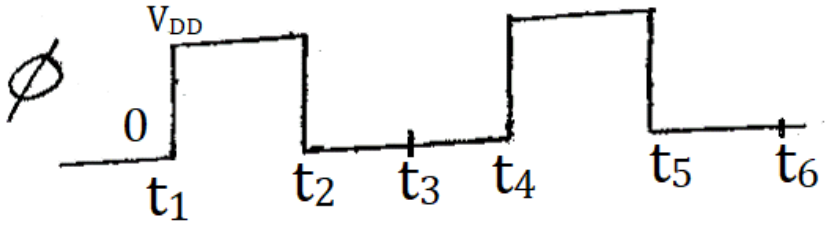
Chapter 9

Dynamic NMOS Inverter





Dynamic NMOS Inverter

At t_1:

$\Phi = V_{DD}$ then Q_2 and Q_3 are ON

$v_0 = \overline{v_i}$ *and* $C = \overline{v_i}$

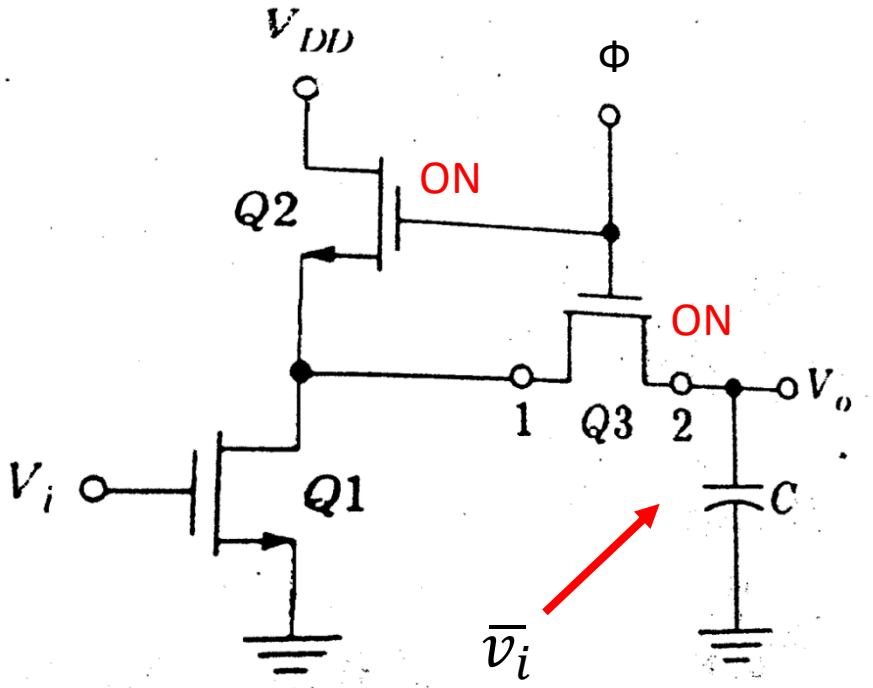
$v_i = 0$ *then* Q_1 *OFF*

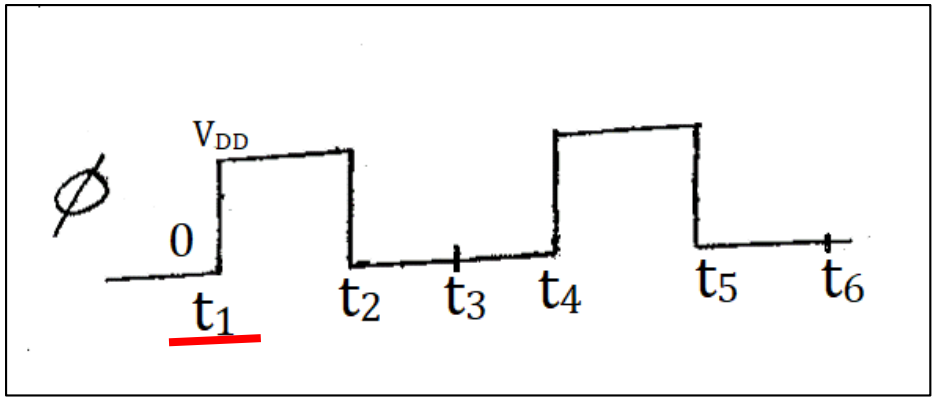
$v_0 = V_{DD}$ *and* $C = V_{DD}$

$v_i = 1$ *then* Q_1 *ON*

- v_0 *connects to ground*
- *C discharges*

$v_0 = \text{GND}$ *and* $C = \text{GND}$

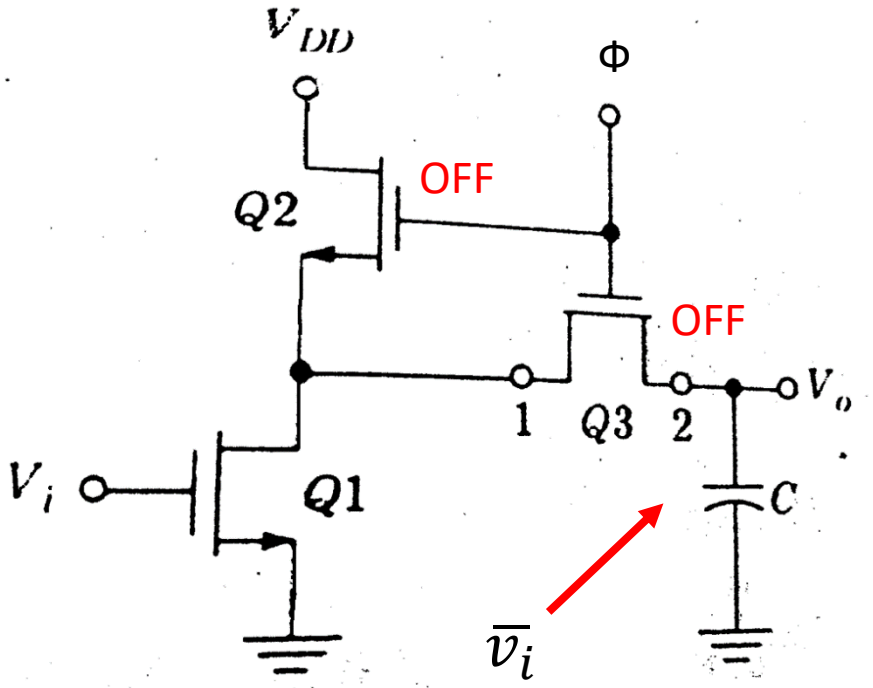




At t_2:

$\Phi = 0$ then Q_2 and Q_3 are OFF

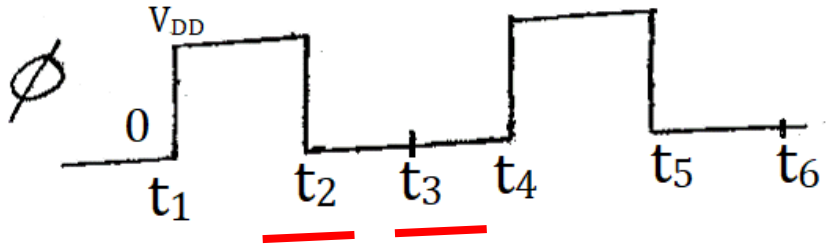
$v_0 = \overline{v_i}$ *and* $C = \overline{v_i}$



At t_3:

$\Phi = 0$ then Q_2 and Q_3 are OFF

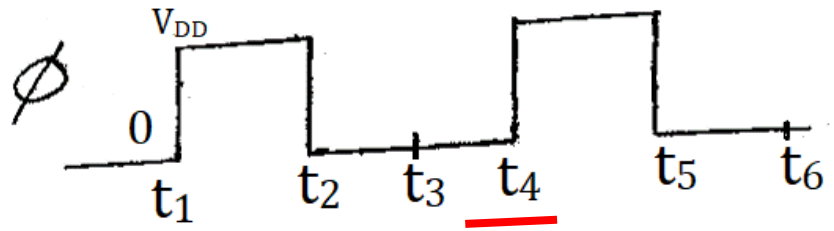
$v_0 = \overline{v_i}$ *and* $C = \overline{v_i}$

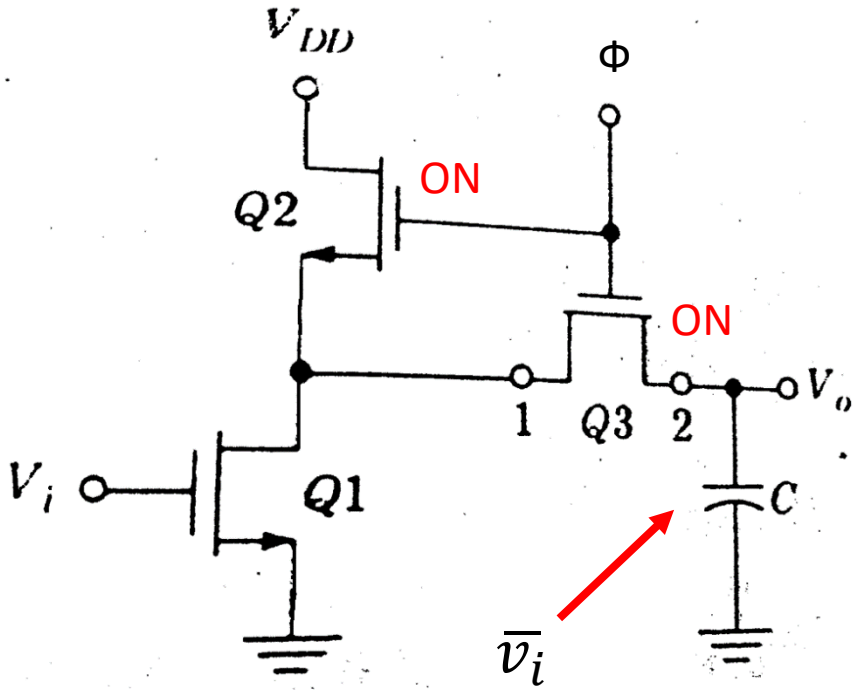


At t_4:

$\Phi = V_{DD}$ then Q_2 and Q_3 are ON

$v_0 = \overline{v_i}$ *and* $C = \overline{v_i}$

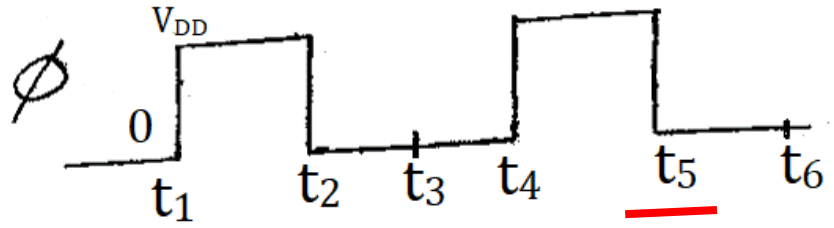


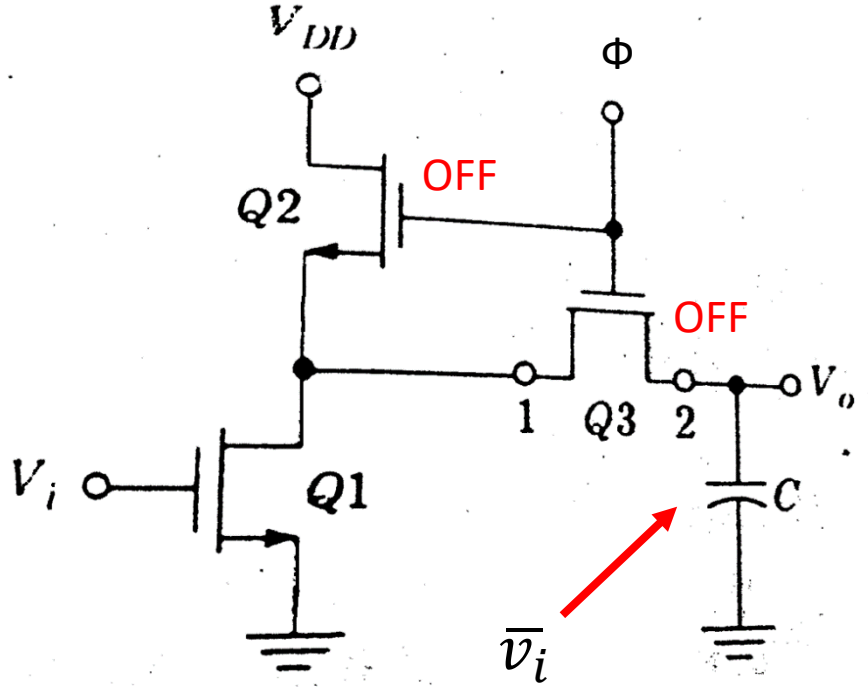


At t_5:

$\Phi = 0$ then Q_2 and Q_3 are OFF

$v_0 = \overline{v_i}$ *and* $C = \overline{v_i}$





At $t_6 = t_3$, repetition will start.

Why is it called ratioed inverter?

The inverter discussed above is called a *ratioed inverter*. The name derives from the fact that when the input is high and the clock is high, transistors $Q1$ and $Q2$ form a voltage divider between V_{DD} and ground. Therefore the output voltage V_o depends on the ratio of the ON resistance of $Q1$ and the effective load resistance of $Q2$ (typically, $< 1 : 5$). This ratio is related to the physical size of $Q1$ and $Q2$ and is often referred to as the *aspect ratio*.

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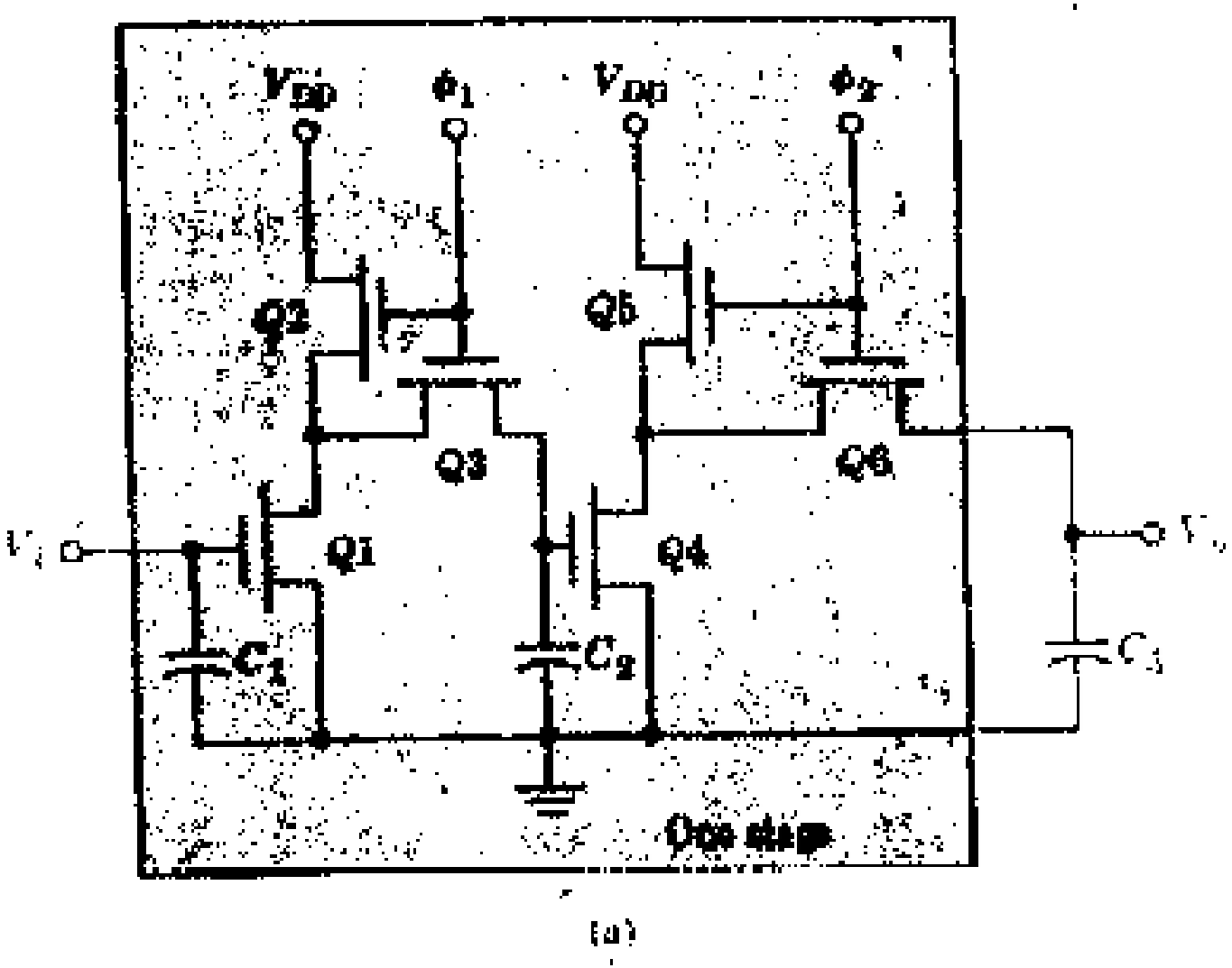
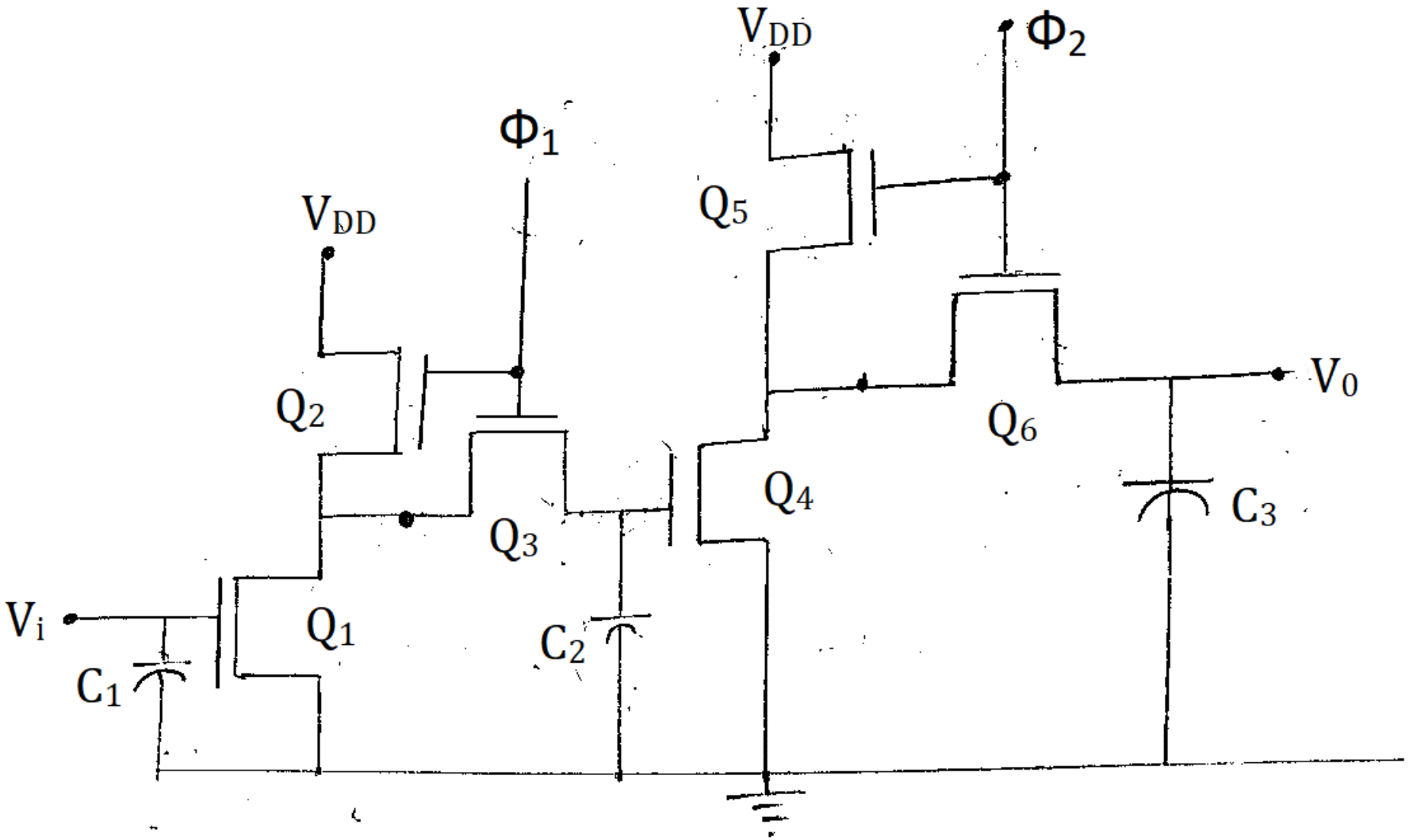
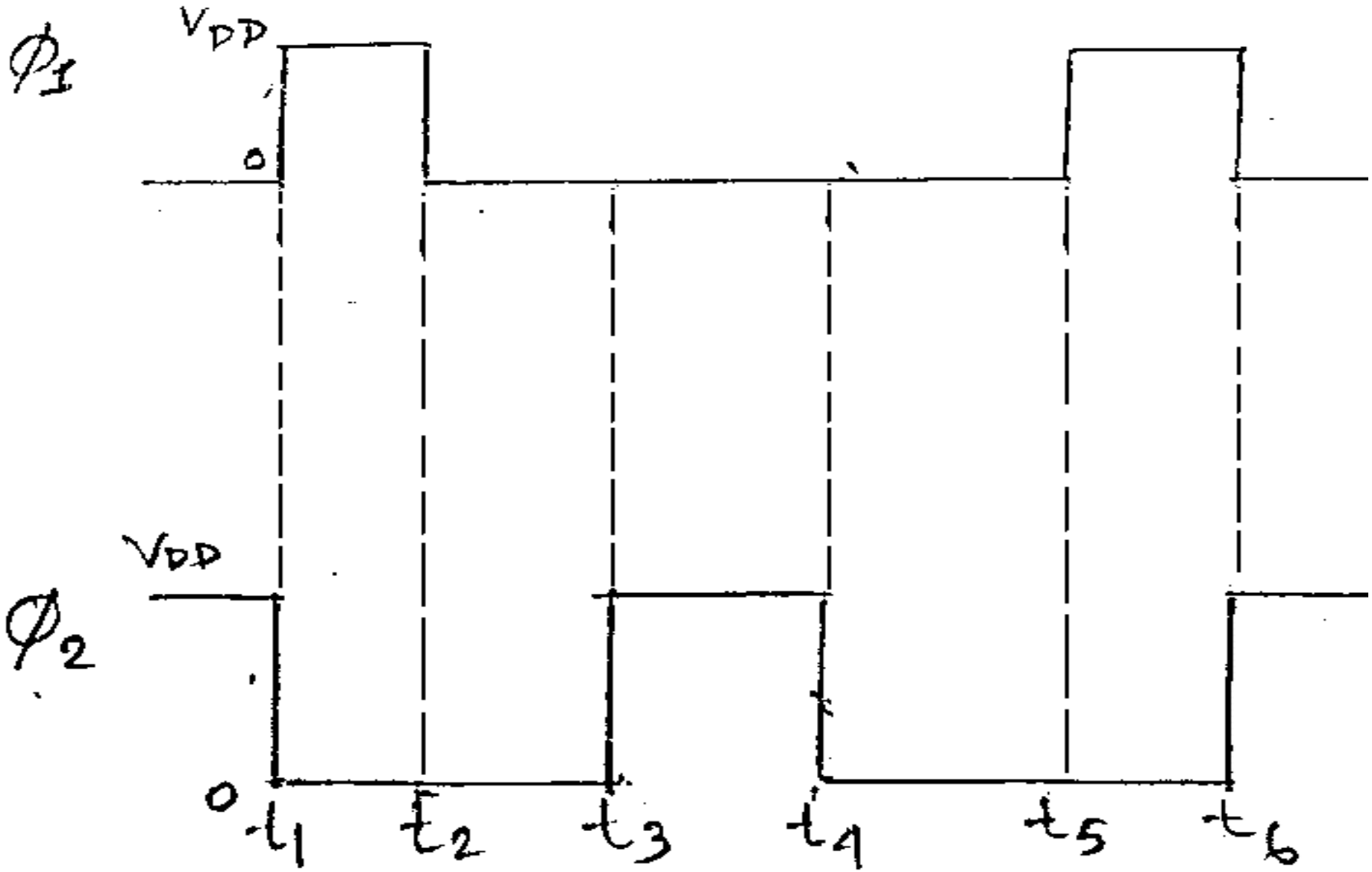
Two Phased Ratioed Dynamic NMOS Shift Register

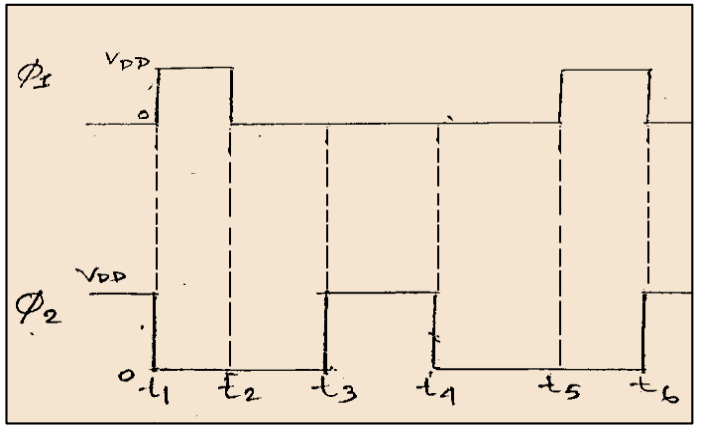
Cascading two dynamic inverters allows each bit of information which is stored on first capacitor C_0 connected to the gate of Q_1 to be transferred to the following inverter by applying second clock pulse out of phase with first clock pulse.




V_{DD}
Φ_2
Φ_1
V_{DD}
Q_5
Q_2
Q_6
V_0
Q_4
Q_3
C_3
V_i
Q_1
C_2
C_1


ϕ_1
V_{DD}
0
V_{DD}
ϕ_2
0
t_1
t_2
t_3
t_4
t_5
t_6

At t_1 :

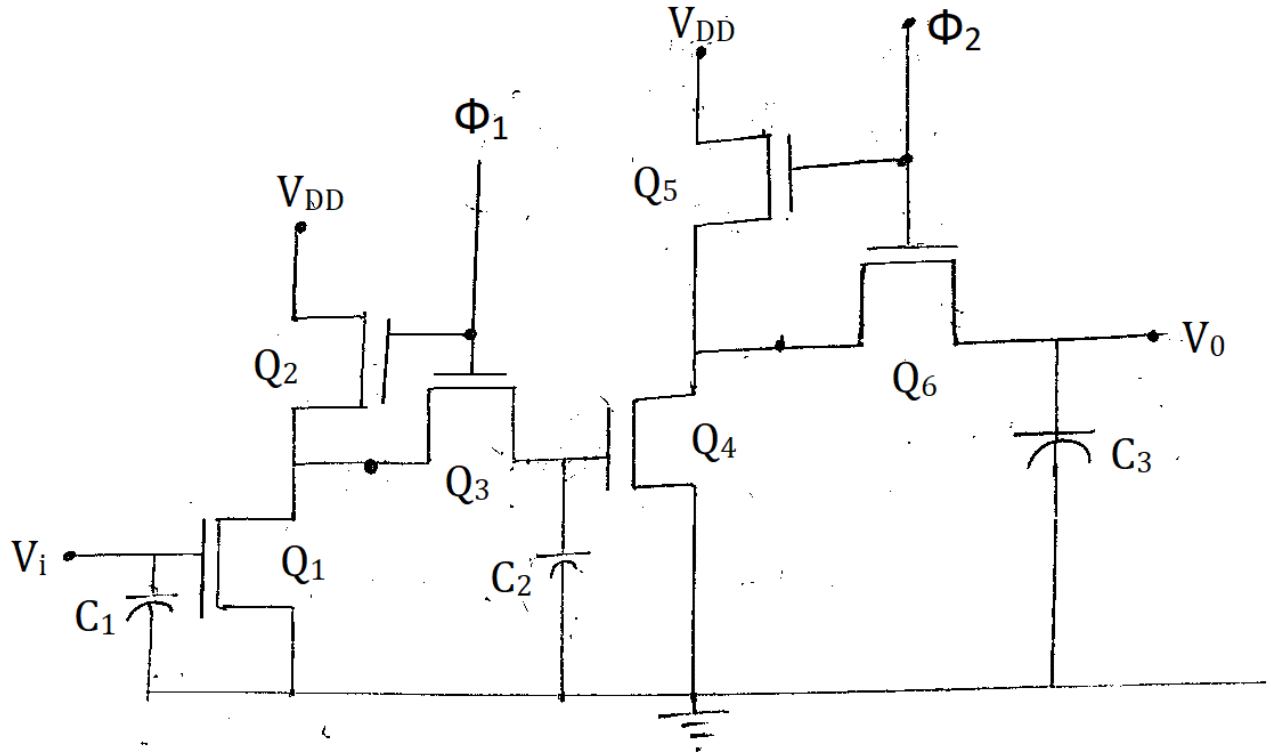


$\Phi_1 = V_{DD}$ then Q_2 and Q_3 are ON

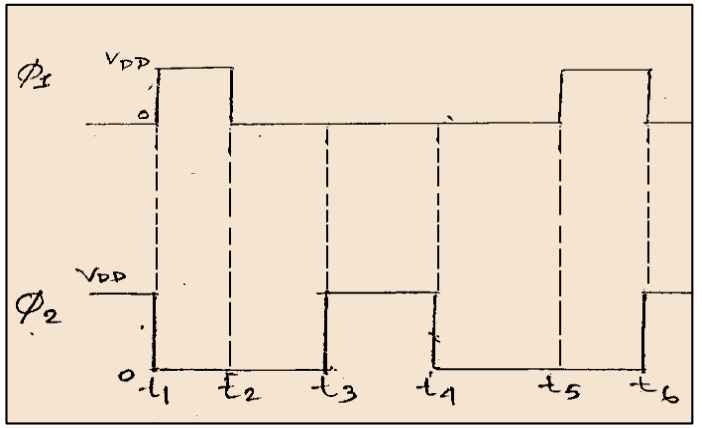
$\Phi_2 = 0$ then Q_5 and Q_6 are OFF

$C_1 = v_i$

$C_2 = \overline{v_i}$



At t_2 :

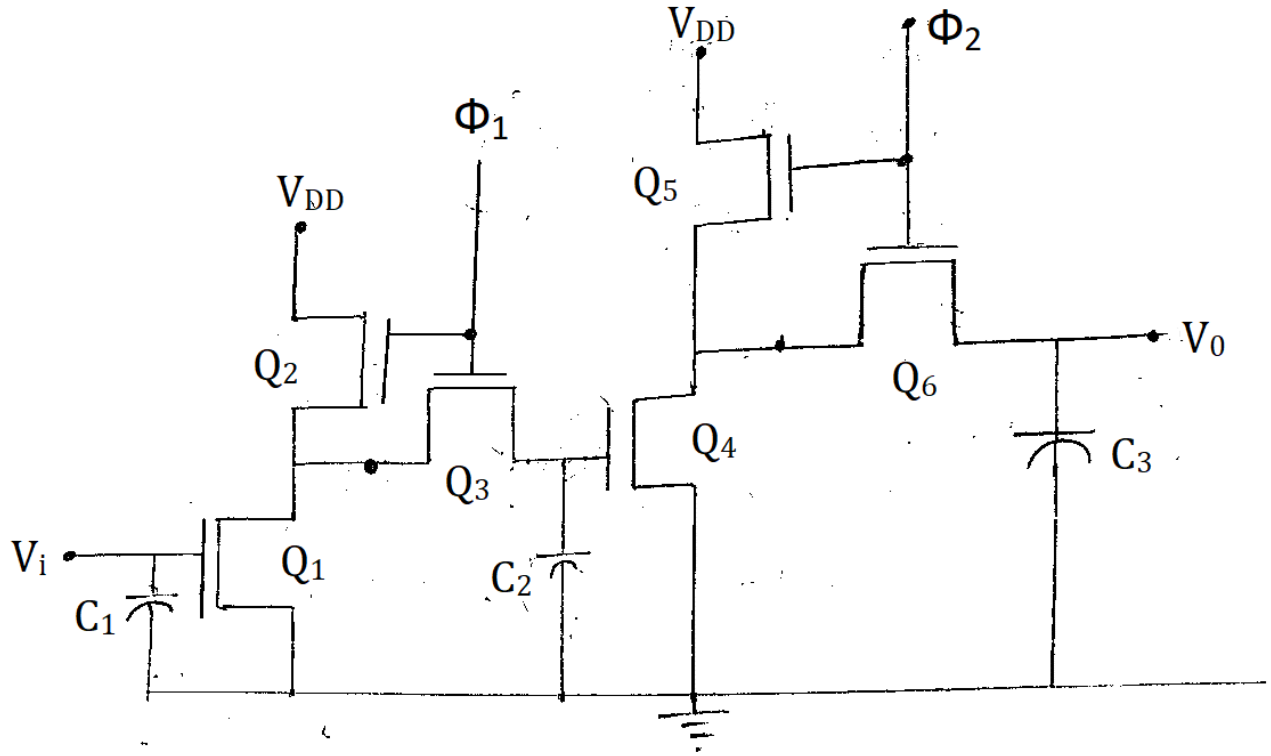


$\Phi_1 = 0$ then Q_2 and Q_3 are OFF

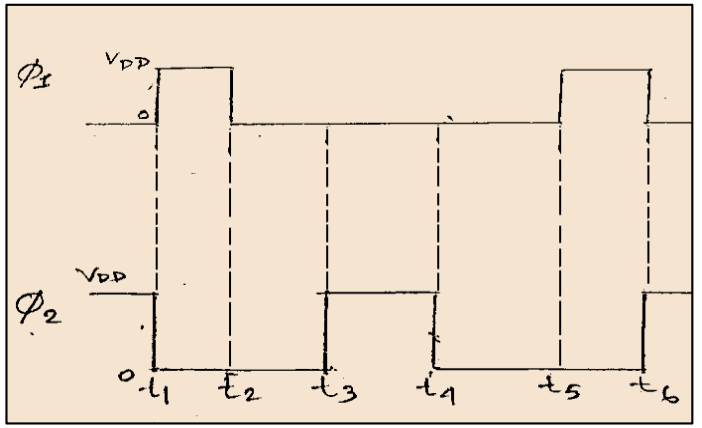
$\Phi_2 = 0$ then Q_5 and Q_6 are OFF

$C_1 = v_i$

$C_2 = \overline{v_i}$



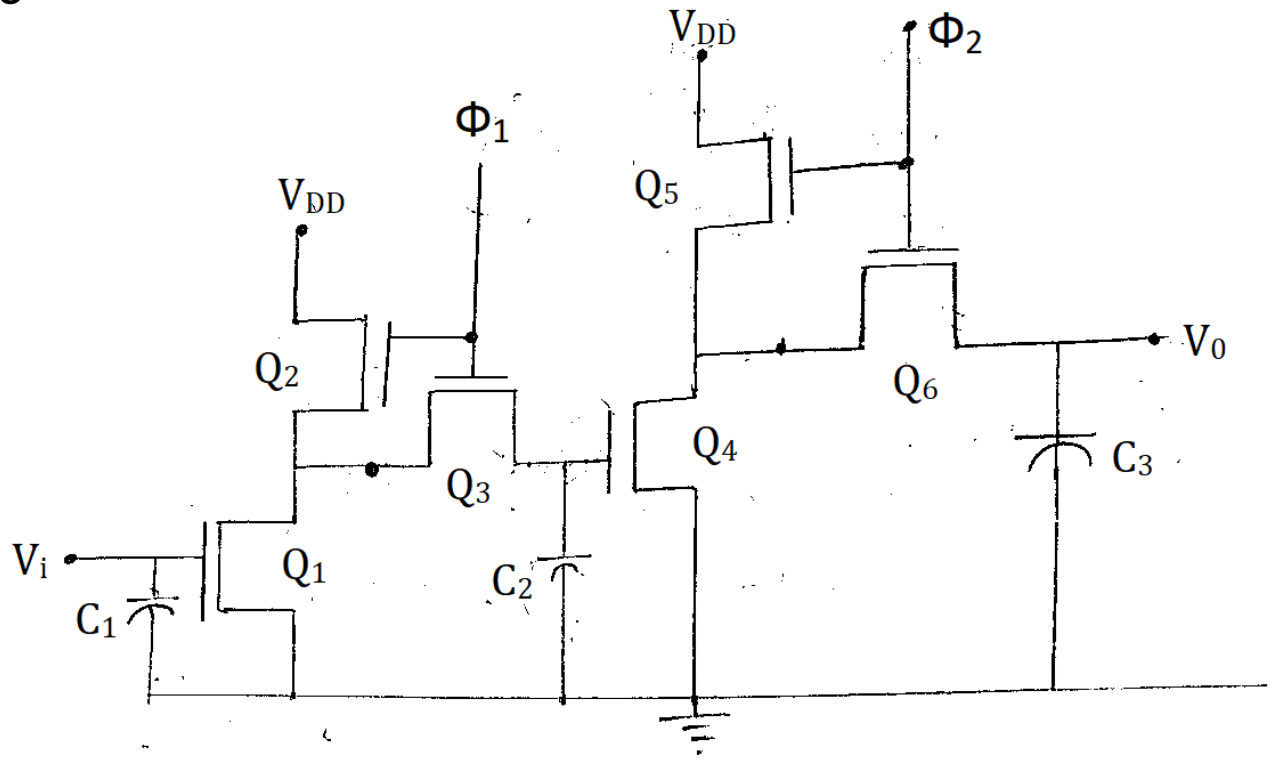
At t_3 :



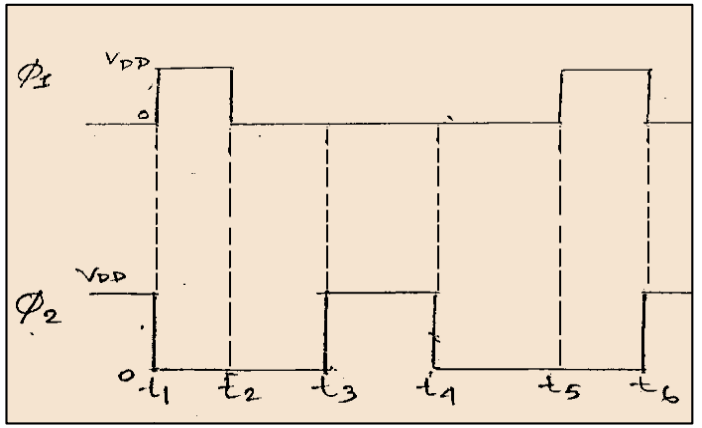
$\Phi_1 = 0$ then Q_2 and Q_3 are OFF

$\Phi_2 = V_{DD}$ then Q_5 and Q_6 are ON

$C_1 = v_i$
$C_2 = \overline{v_i}$
$C_3 = v_i$
$V_0 = v_i$



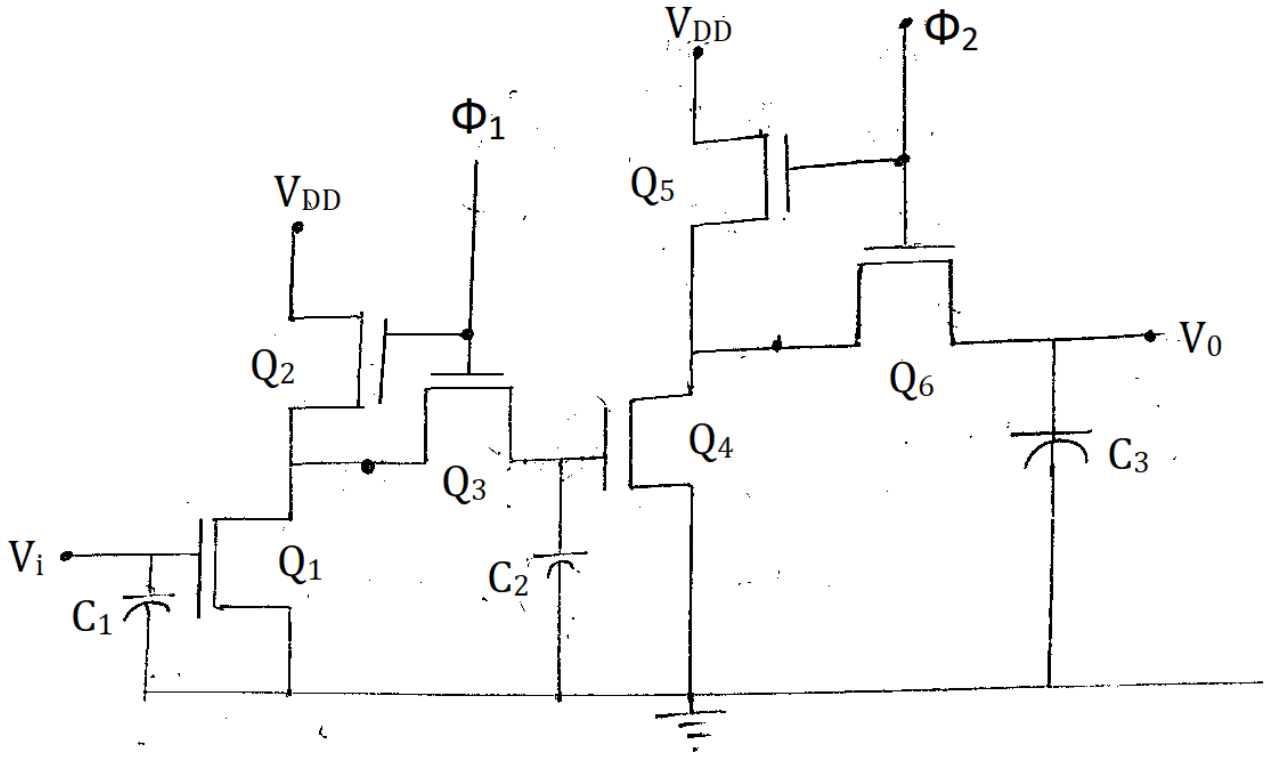
At t_4 :



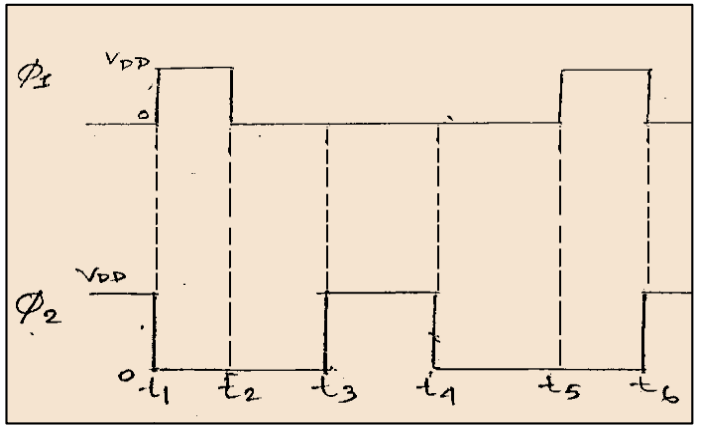
$\Phi_1 = 0$ then Q_2 and Q_3 are OFF

$\Phi_2 = 0$ then Q_5 and Q_6 are OFF

$C_1 = v_i$
$C_2 = \overline{v_i}$
$C_3 = v_i$
$V_0 = v_i$



At t_5 :



$\Phi_1 = V_{DD}$ then Q_2 and Q_3 are ON

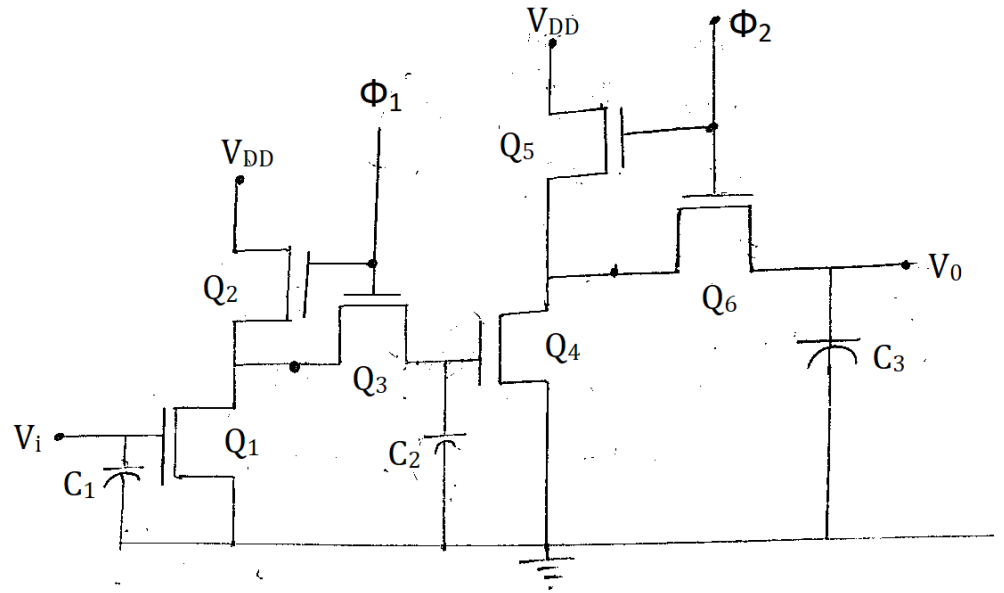
$\Phi_2 = 0$ then Q_5 and Q_6 are OFF

$C_1 = v_i$

$C_2 = \overline{v_i}$

$C_3 = v_i$

$V_0 = v_i$

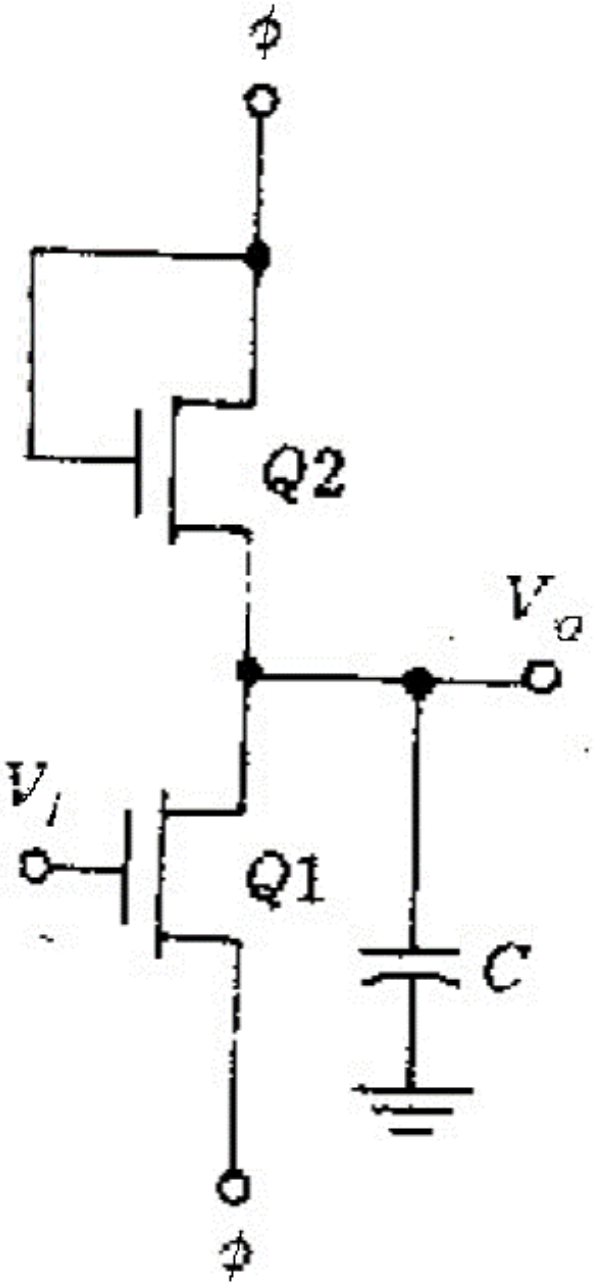


At t_6 repetition will start

Dynamic Ratioless Inverter

- The ratioed invertor limits the speed of operation of the register and had more power dissipation. As such, a ratioless invertor is given here.

- No power supply is used here. The clock pulse ϕ will supply the required energy to the circuit. Here, the power dissipation is proportional to the clocking frequency.



Two Phase Ratioless Dynamic NMOS Shift Register

By cascading two ratioless dynamic inverters we obtain the ratioless dynamic shift register. The first inverter is powered by pulse ϕ_1 and the second by pulse ϕ_2.

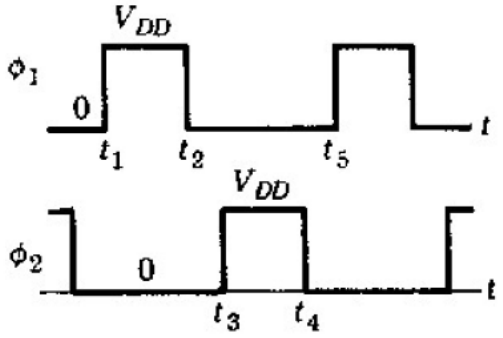
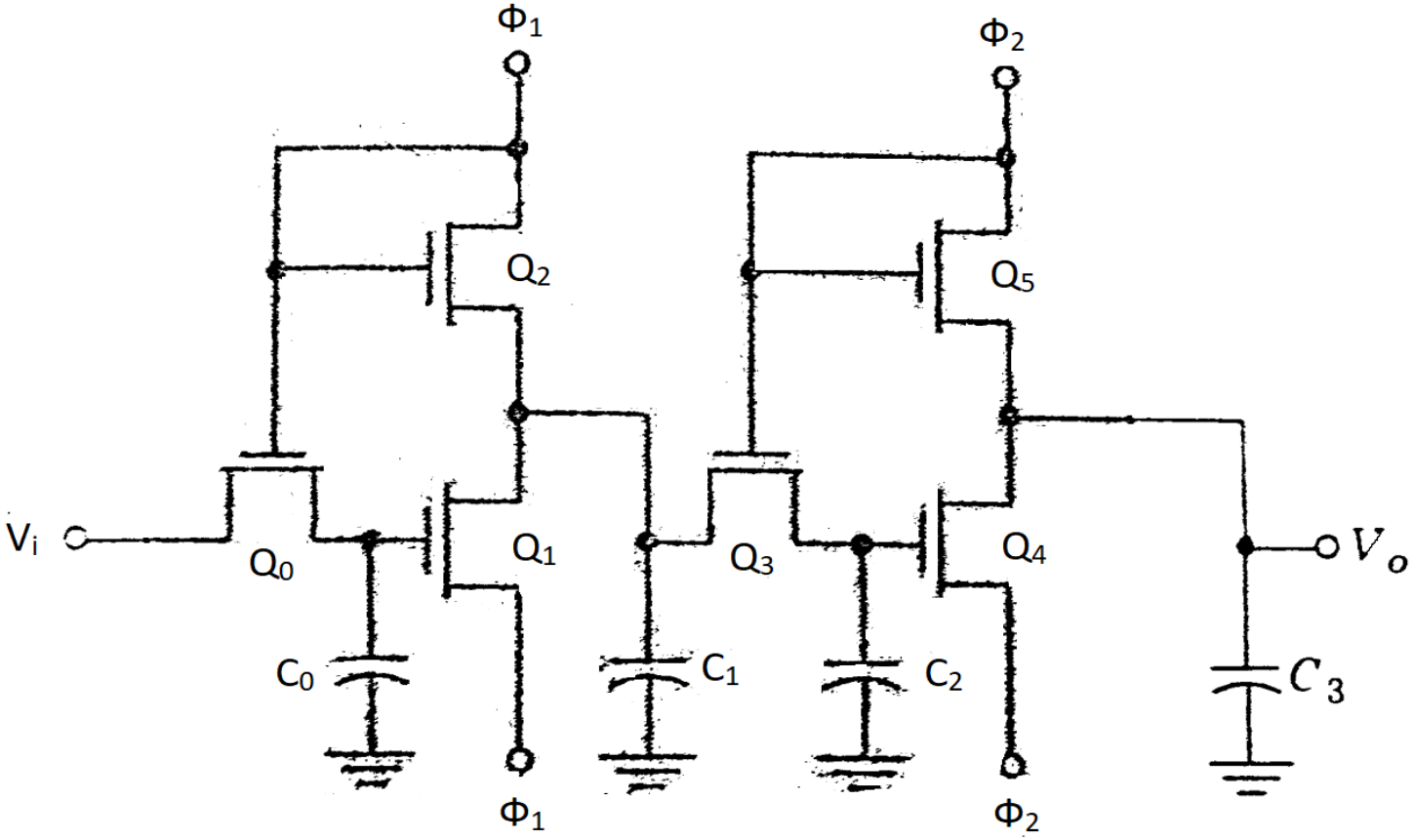


Fig: 9.5 (Book PG. 275)



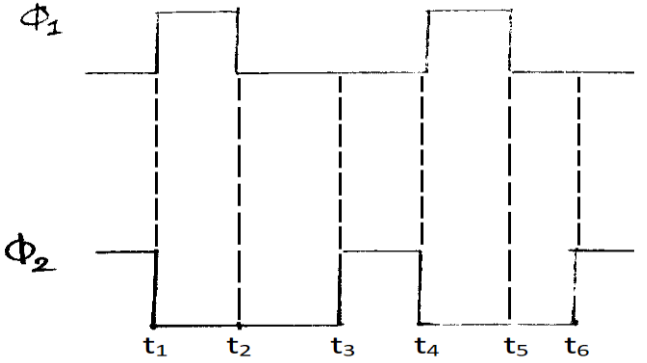
At t_1 :

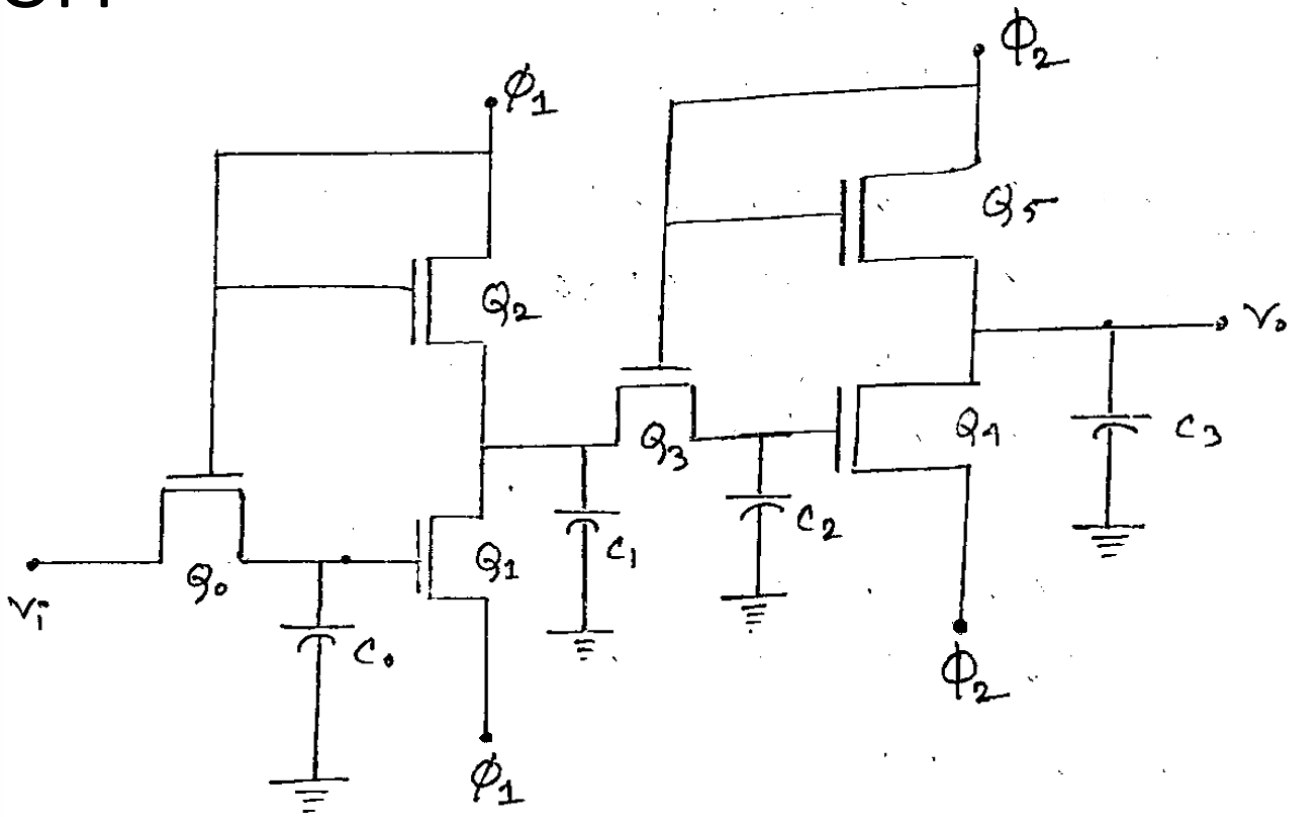
$\Phi_1 = V_{DD}$ then Q_0 and Q_2 are ON

$\Phi_2 = 0$ then Q_3 and Q_5 are OFF

$C_0 = v_i$

$C_1 = \overline{v_i}$





$V_i = 0$, Q_1 off C_1 charges to V_{DD} through Q_2
$V_i = V_{DD}$, C_0 charges and Q_1 is on
At the end of phase t1 when Φ_1 goes to 0, Q_2 turns off but V_i is still V_{DD} as such C_1 discharges the charge through Q_1 at the end of the phase.

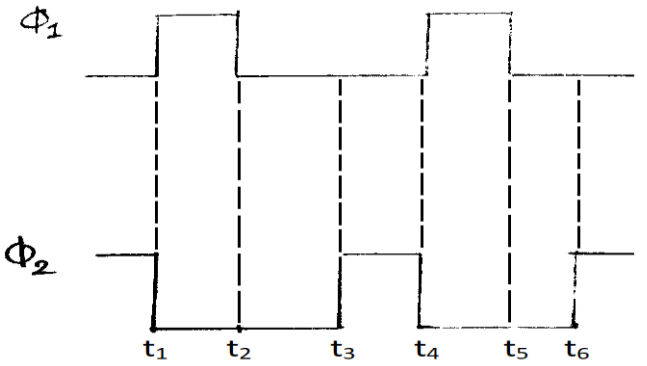
At t_2 :

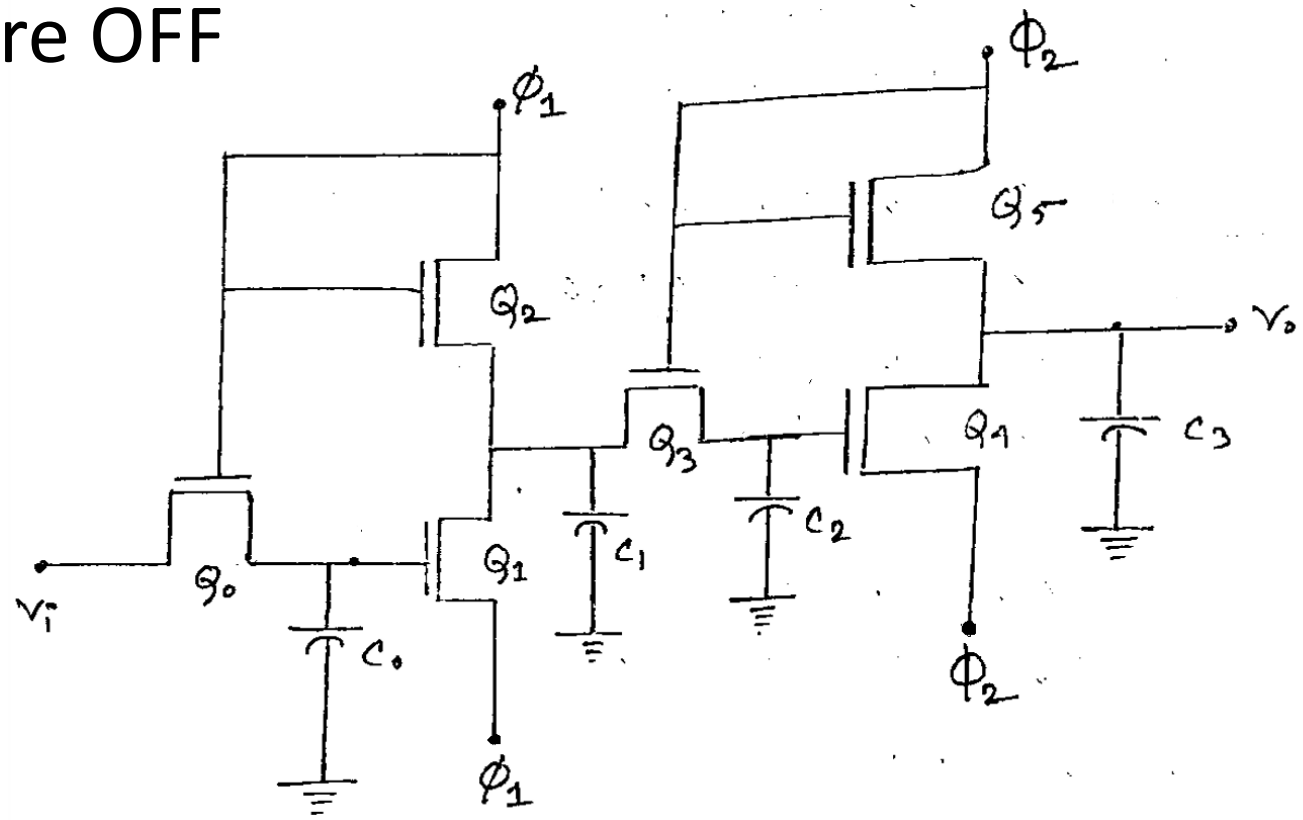
$\Phi_1 = 0$ then Q_0 and Q_2 are OFF

$\Phi_2 = 0$ then Q_3 and Q_5 are OFF

$C_0 = v_i$

$C_1 = \overline{v_i}$





At t_3 :

Φ_1 = 0 then Q_0 and Q_2 are OFF

$\Phi_2 = V_{DD}$ then Q_3 and Q_5 are ON

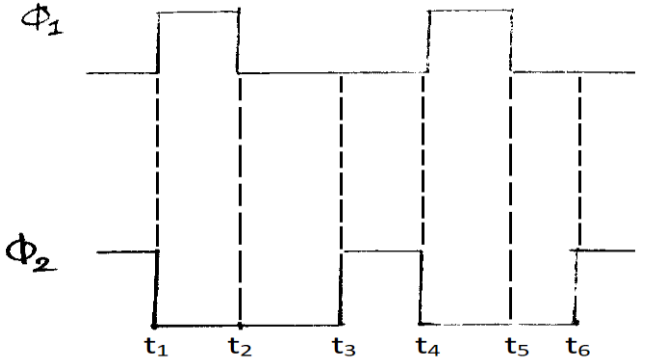
$C_0 = v_i$

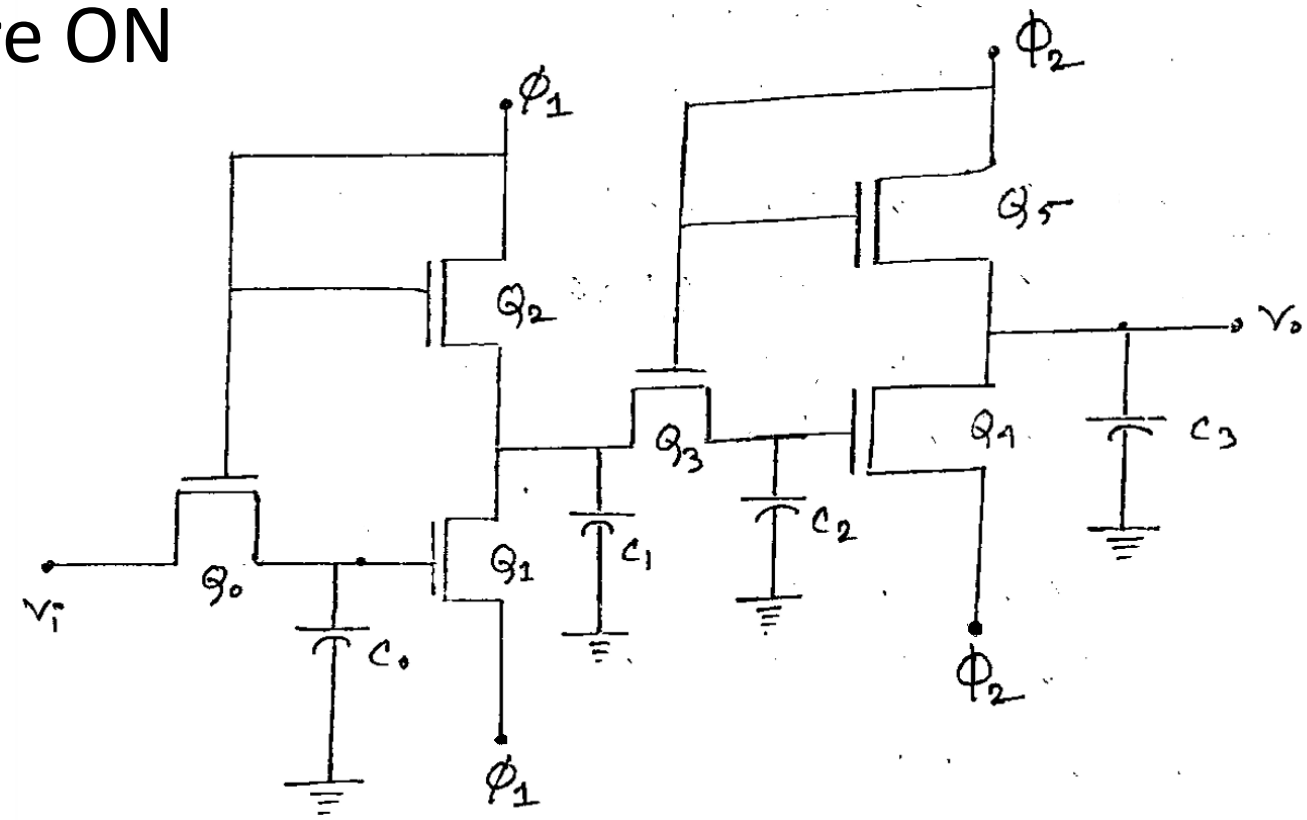
$C_1 = \overline{v_i}$

$C_2 = C_1 = \overline{v_i}$

$C_3 = \bar{C}_2 = \bar{C}_1 = \overline{\overline{C_0}} = \overline{\overline{V_i}} = V_i$

$V_0 = v_i$





At t_4 :

$\Phi_1 = V_{DD}$ then Q_0 and Q_2 are ON

$\Phi_2 = 0$ then Q_3 and Q_5 are OFF

$C_0 = v_i$

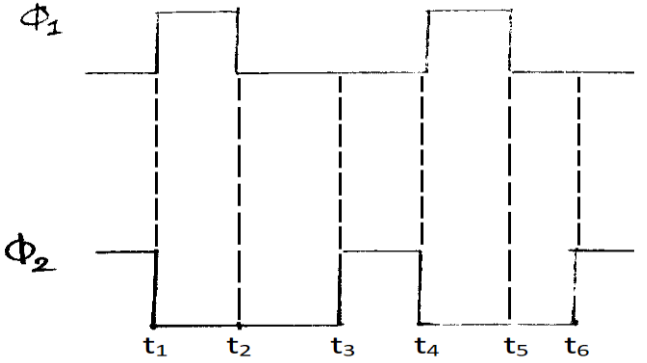
$C_1 = \overline{v_i}$

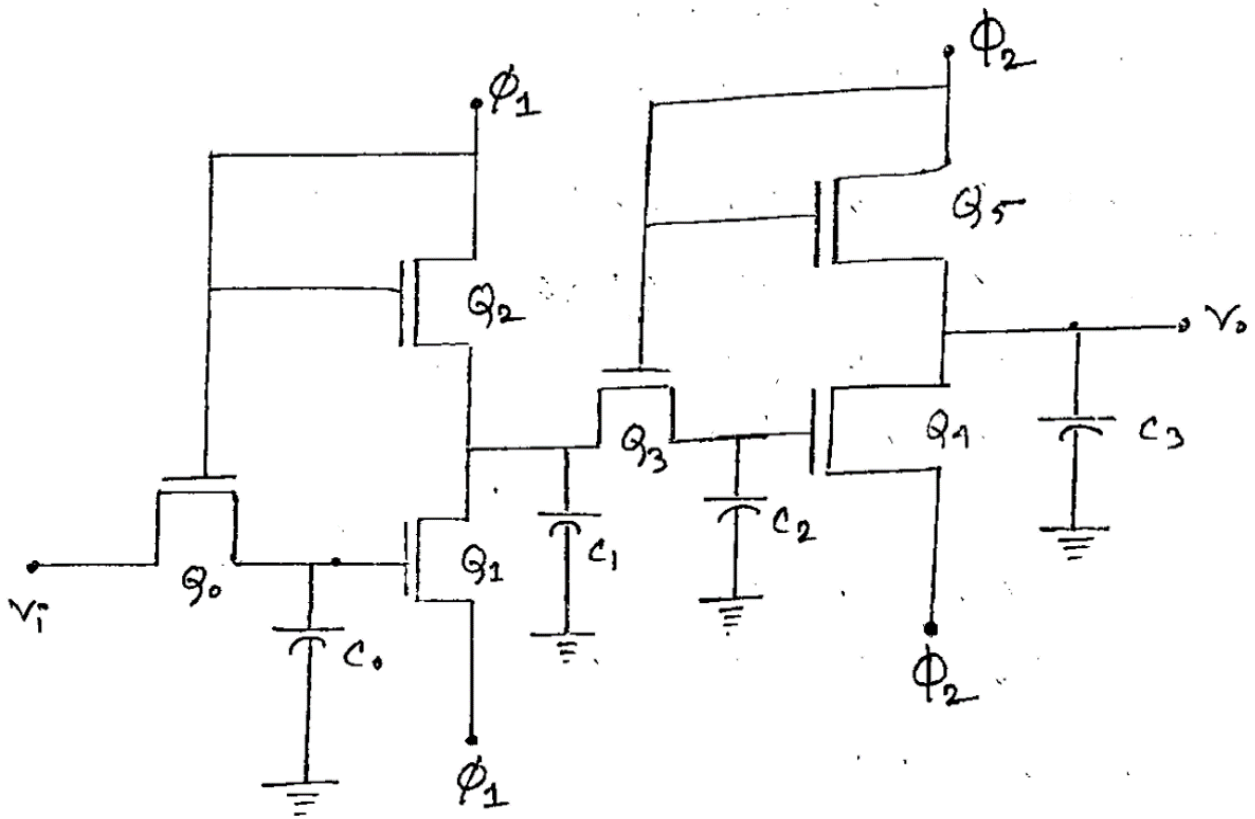
$C_2 = C_1 = \overline{v_i}$

$C_3 = v_i$

$V_0 = v_i$

From t_5 repetition will continue.





- You do not need to draw circuits for each clock pulse during the exam. You can draw the clock pulse and circuits once and then explain all the steps.