AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Department of Computer Science and Engineering

DIGITAL LOGIC DESIGN LAB

CSE 2106

Experiment No : 10

Experiment Name : (a) Design a switch controlled Binary Random Up-Down counter using J-K Flip-Flop for the following sequence: 3 → 5 → 2 → 0 → 1

(b) Design a 4-Bit Synchronous Counter Using T Flip-Flop.

Submitted by

Name : S.M. Tasnimul Hasan

ID : 18.02.04.142

Department : CSE

Section : B (B2)

Group : 02(8)

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a) Experiment Name :

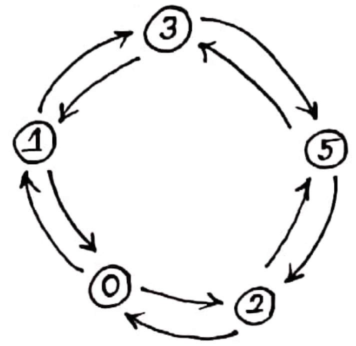
Design a switch controlled binary random up-down counter using JK Flip Flop for the following sequence :

$$3 \rightarrow 5 \rightarrow 2 \rightarrow 0 \rightarrow 1$$

Objective :

Counters are used for the purpose of counting which can increment or decrement a count by 1. An up counter may be made by connecting the clock inputs of positive edge triggered J-K flip flops to the Q' outputs of the preceding flipflops. Another way is to use negative edge triggered flip flops, connecting the clock inputs to the Q outputs of the preceding flip flops. The main objective of the experiment is to design a switch controlled binary random up down counter using J-K flipflops for the given sequence.

State Diagram :



State Table :

PS	NS	
	$x=0$ (up)	$x=1$ (down)
3	5	1
5	2	3
2	0	5
0	1	2
1	3	0

$\therefore$ Number of flip flops $= \lceil \log_2 5 \rceil$

$= 3$

Excitation Table :

	PS			NS ($x=0$)			NS ($x=1$)			FF's input ($x=0$)			FF's input ($x=1$)		
	Q_3	Q_2	Q_1	Q_3	Q_2	Q_1	Q_3	Q_2	Q_1	$J_3\ K_3$	$J_2\ K_2$	$J_1\ K_1$	$J_3\ K_3$	$J_2\ K_2$	$J_1\ K_1$
3	0	1	1	1	0	1	0	0	1	1 X	X 1	X 0	0 X	X 1	X 0
5	1	0	1	0	1	0	0	1	1	X 1	1 X	X 1	X 1	1 X	X 0
2	0	1	0	0	0	0	1	0	1	0 X	X 1	0 X	1 X	X 1	1 X
0	0	0	0	0	0	1	0	1	0	0 X	0 X	1 X	0 X	1 X	0 X
1	0	0	1	0	1	1	0	0	0	0 X	1 X	X 0	0 X	0 X	X 1

Common don't care, $d = \Sigma(4, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15)$

$= \Sigma(4, 6-15)$

Function Evaluation :

$J_3 = \Sigma(2, 3)$

$d = \Sigma(4-15)$

Q_3Q_2 \ Q_1x	$\overline{Q_1}\,\overline{x}$	$\overline{Q_1}x$	Q_1x	$Q_1\overline{x}$
$\overline{Q_3}\,\overline{Q_2}$			1	1
$\overline{Q_3}Q_2$	X	X	X	X
Q_3Q_2	X	X	X	X
$Q_3\overline{Q_2}$	X	X	X	X

$\therefore J_3 = Q_1$

$K_3 = \Sigma(5)$

$d = \Sigma(0, 1, 2, 3, 4, 6-15)$

Q_3Q_2 \ Q_1x	$\overline{Q_1}\,\overline{x}$	$\overline{Q_1}x$	Q_1x	$Q_1\overline{x}$
$\overline{Q_3}\,\overline{Q_2}$	X	X	X	X
$\overline{Q_3}Q_2$	X	1	X	X
Q_3Q_2	X	X	X	X
$Q_3\overline{Q_2}$	X	X	X	X

$\therefore K_3 = 1$

$J_2 = \Sigma(0,1,5)$

$d = \Sigma(2,3,4,6-15)$

$Q_3Q_2 \backslash Q_1x$	$\bar{Q}_1\bar{x}$	$\bar{Q}_1x$	Q_1x	$Q_1\bar{x}$
$\bar{Q}_3\bar{Q}_2$	1	1	X	X
$\bar{Q}_3Q_2$	X	1	X	X
Q_3Q_2	X	X	X	X
$Q_3\bar{Q}_2$	X	X	X	X

$\therefore J_2 = 1$

$K_2 = \Sigma(2,3)$

$d = \Sigma(0,1,4-15)$

$Q_3Q_2 \backslash Q_1x$	$\bar{Q}_1\bar{x}$	$\bar{Q}_1x$	Q_1x	$Q_1\bar{x}$
$\bar{Q}_3\bar{Q}_2$	X	X	1	1
$\bar{Q}_3Q_2$	X	X	X	X
Q_3Q_2	X	X	X	X
$Q_3\bar{Q}_2$	X	X	X	X

$\therefore K_2 = 1$

$J_1 = \Sigma(0,2)$

$d = \Sigma(1,3,4-15)$

$Q_3Q_2 \backslash Q_1x$	$\bar{Q}_1\bar{x}$	$\bar{Q}_1x$	Q_1x	$Q_1\bar{x}$
$\bar{Q}_3\bar{Q}_2$	1	X	X	1
$\bar{Q}_3Q_2$	X	X	X	X
Q_3Q_2	X	X	X	X
$Q_3\bar{Q}_2$	X	X	X	X

$\therefore J_1 = 1$

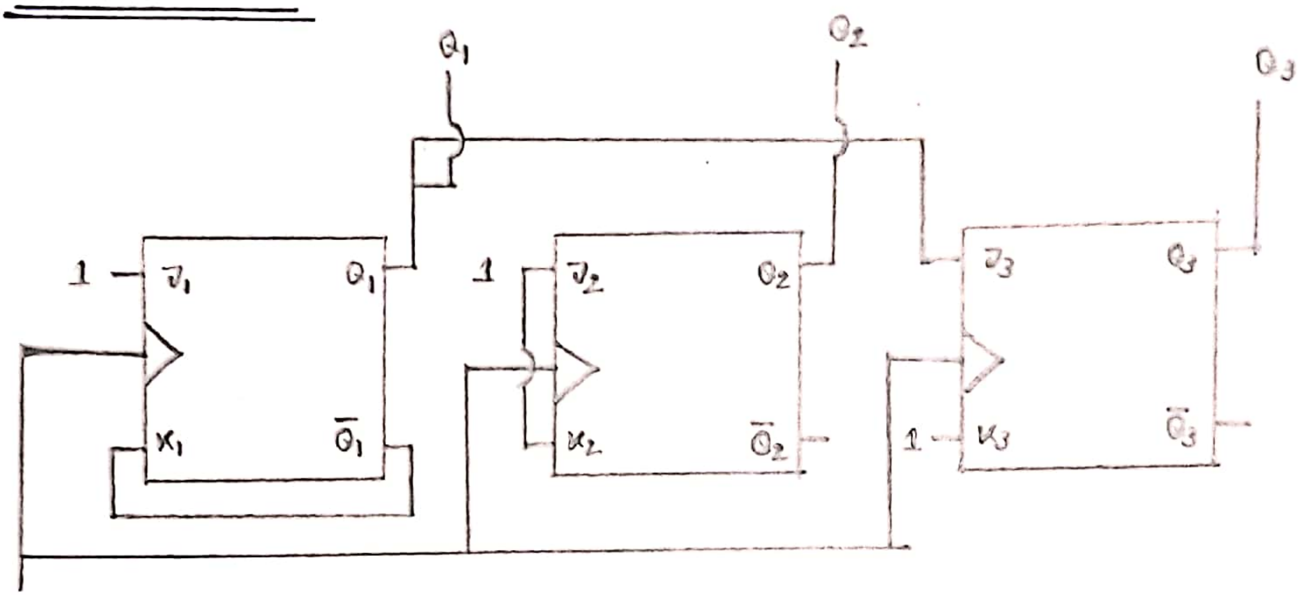
$K_1 = \Sigma(1,5)$

$d = \Sigma(0,2,4,6-15)$

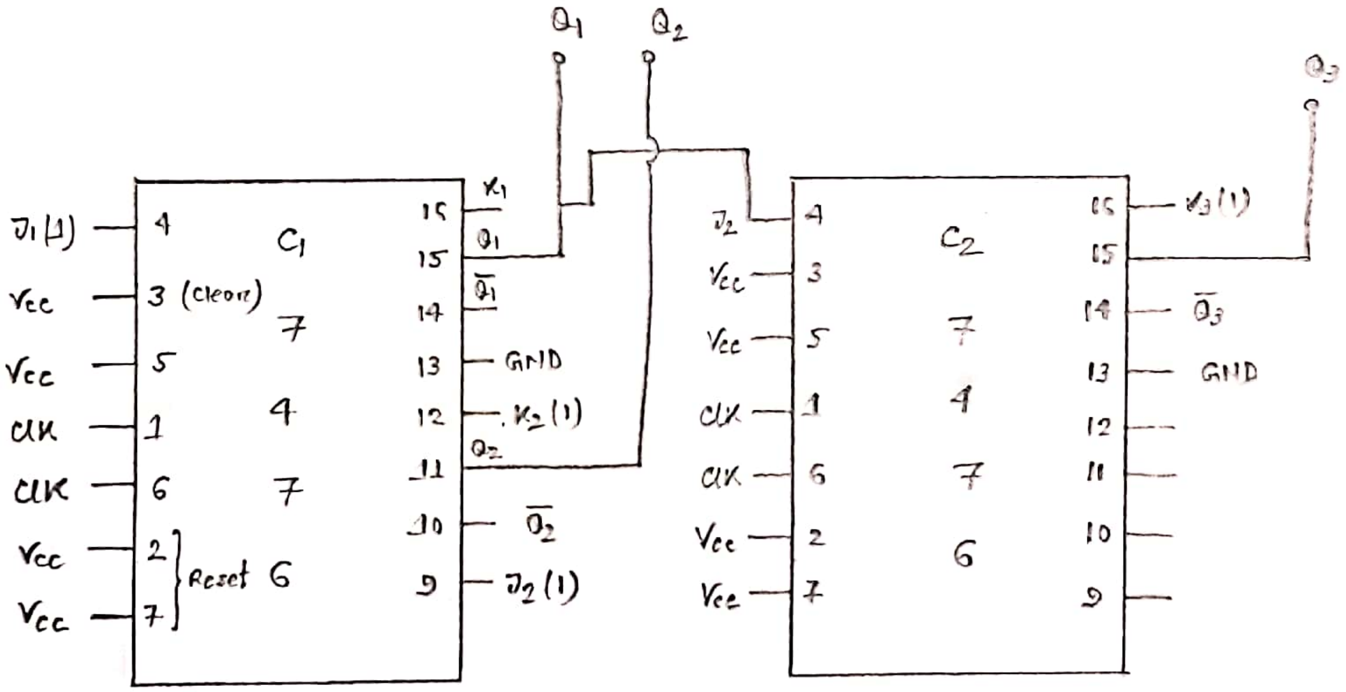
$Q_3Q_2 \backslash Q_1x$	$\bar{Q}_1\bar{x}$	$\bar{Q}_1x$	Q_1x	$Q_1\bar{x}$
$\bar{Q}_3\bar{Q}_2$	X	1		X
$\bar{Q}_3Q_2$	X	1	X	X
Q_3Q_2	X	X	X	X
$Q_3\bar{Q}_2$	X	X	X	X

$\therefore K_1 = \bar{Q}_1$

Block Diagram :



Circuit Diagram :



IC Requirements :

1. C_1, C_2 : 7476 – 2 piece

Conclusion :

From this experiment, it has been possible to design a switch controlled up down counter using JK Flip Flop. The JK Flip flop is one of the most versatile and widely used flip flops. The most prominent reason behind using it as a counter is its toggle operation. The JK Flip Flop is called universal flip flop. We have finished our experiment successfully,

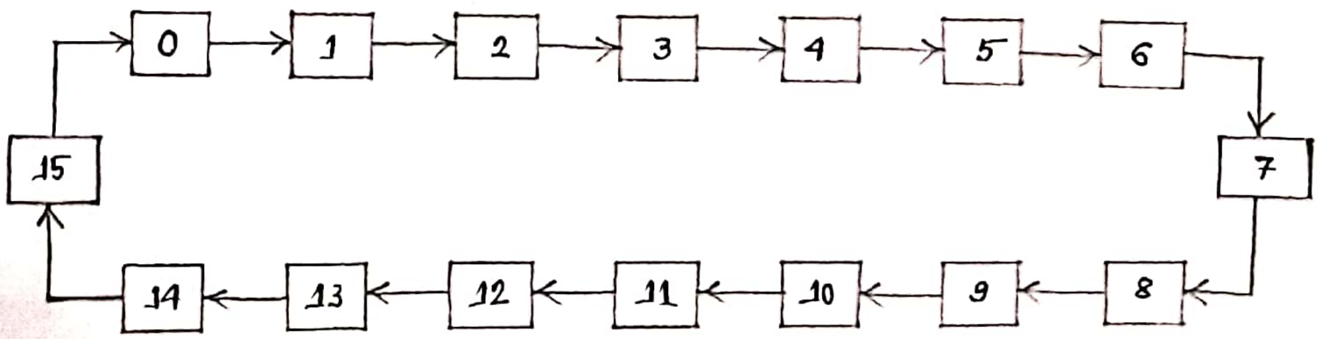
b) Experiment Name :

Design a 4-Bit Synchronous counter using T Flip Flop.

Objective :

Synchronous counter is the type of counter which is built by clocking all the flip-flops at the same time with a single clocking source. Synchronous counter receives the common clock as the pulse. The objective of this experiment is to design a 4-bit Synchronous counter using T Flip-Flop.

State Diagram :



State Table :

PS	NS
0	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	10
10	11
11	12
12	13
13	14
14	15
15	0

Number of flip flops :

$$\lceil \log_2 15 \rceil$$

$$= 4$$

Excitation Table :

PS				NS				FF's Input			
Q_4	Q_3	Q_2	Q_1	Q_4	Q_3	Q_2	Q_1	T_4	T_3	T_2	T_1
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	1	0	1	0	0	0	1	1
1	0	1	0	1	0	1	1	0	0	0	1
1	0	1	1	1	1	0	0	0	1	1	1
1	1	0	0	1	1	0	1	0	0	0	1
1	1	0	1	1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	1	0	0	0	1
1	1	1	1	0	0	0	0	1	1	1	1

Function Evaluation Using KMap :

$$T_4 = \Sigma(7, 15)$$

$Q_4Q_3 \backslash Q_2Q_1$	$\bar{Q}_2\bar{Q}_1$	$\bar{Q}_2Q_1$	Q_2Q_1	$Q_2\bar{Q}_1$
$\bar{Q}_4\bar{Q}_3$				
$\bar{Q}_4Q_3$			1	
Q_4Q_3			1	
$Q_4\bar{Q}_3$				

$$\therefore T_4 = Q_3Q_2Q_1$$

$$T_3 = \Sigma(3, 7, 11, 15)$$

$Q_4Q_3 \backslash Q_2Q_1$	$\bar{Q}_2\bar{Q}_1$	$\bar{Q}_2Q_1$	Q_2Q_1	$Q_2\bar{Q}_1$
$\bar{Q}_4\bar{Q}_3$			1	
$\bar{Q}_4Q_3$			1	
Q_4Q_3			1	
$Q_4\bar{Q}_3$			1	

$$\therefore T_3 = Q_2Q_1$$

$T_2 = \Sigma(1, 3, 5, 7, 9, 11, 13, 15)$

Q_4Q_3 \ Q_2Q_1	$\bar{Q}_2\bar{Q}_1$	$\bar{Q}_2Q_1$	Q_2Q_1	$Q_2\bar{Q}_1$
$\bar{Q}_4\bar{Q}_3$		1	1	
$\bar{Q}_4Q_3$		1	1	
Q_4Q_3		1	1	
$Q_4\bar{Q}_3$		1	1	

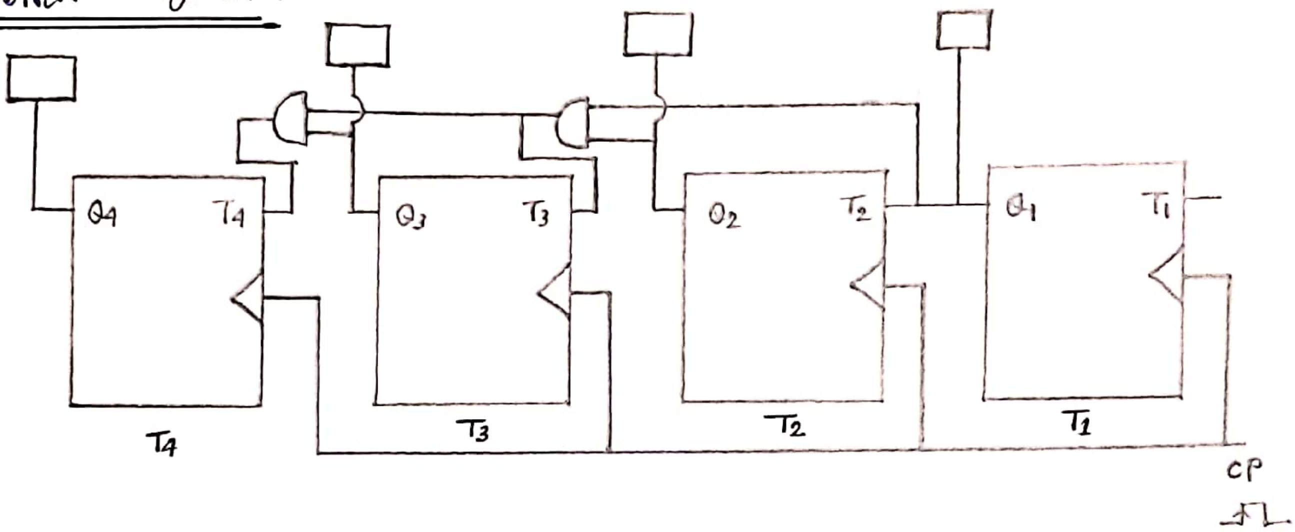
$\therefore T_2 = Q_1$

$T_1 = \Sigma(0-15)$

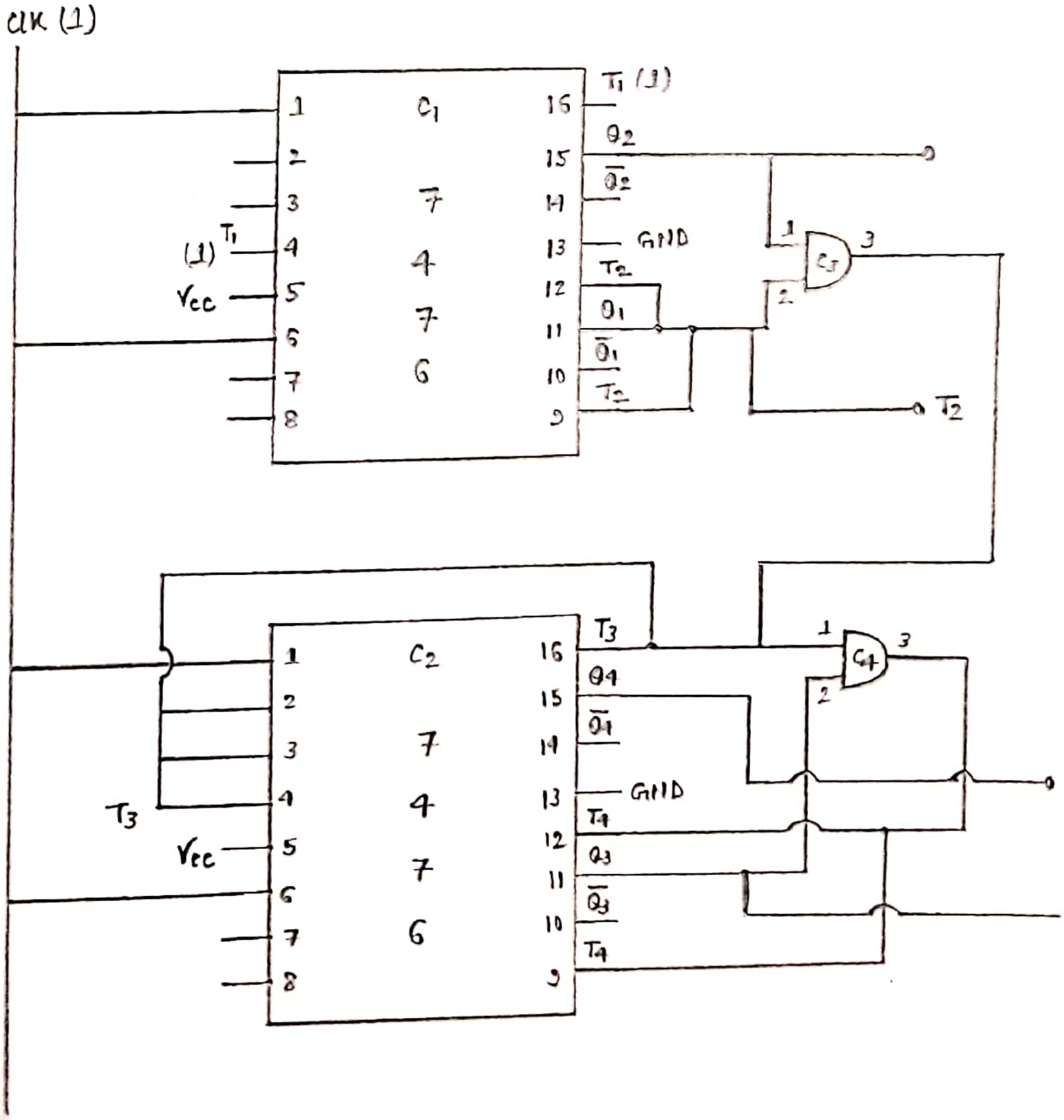
Q_4Q_3 \ Q_2Q_1	$\bar{Q}_2\bar{Q}_1$	$\bar{Q}_2Q_1$	Q_2Q_1	$Q_2\bar{Q}_1$
$\bar{Q}_4\bar{Q}_3$	1	1	1	1
$\bar{Q}_4Q_3$	1	1	1	1
Q_4Q_3	1	1	1	1
$Q_4\bar{Q}_3$	1	1	1	1

$\therefore T_1 = 1$

Block Diagram :



Circuit Diagram :



IC Requirements :

1. $C_1, C_2 \rightarrow$ 7476 (JK Flip Flop) – 2 piece

2. $C_3, C_4 \rightarrow$ 7408 (AND Gate) – 2 piece

Conclusion :

In this experiment, we have designed a 4 bit synchronous counter using T flip flop. It is easier to design than the asynchronous counter as it acts simultaneously. It is also faster than the asynchronous counter as no propagation delay associated with it.

We have finished our experiment successfully.