Ahsanullah University of Science and Technology (AUST)
Department of Computer Science and Engineering

LAB REPORT

Course No. : CSE2210

Course Title: Digital Electronics and Pulse Techniques Lab

Experiment Number: 05

Name of the Experiment: Implementation of clocked SP Flip Flop using RTL NOR gates.

Submitted By:

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Name of the Experiment :

Implementation of clocked SR Flip Flop using RTL NOR gates.

Objective :

The objective of this experiment is to implement a clocked SR flip flop using RTL NOR gates.

Circuit Diagram :

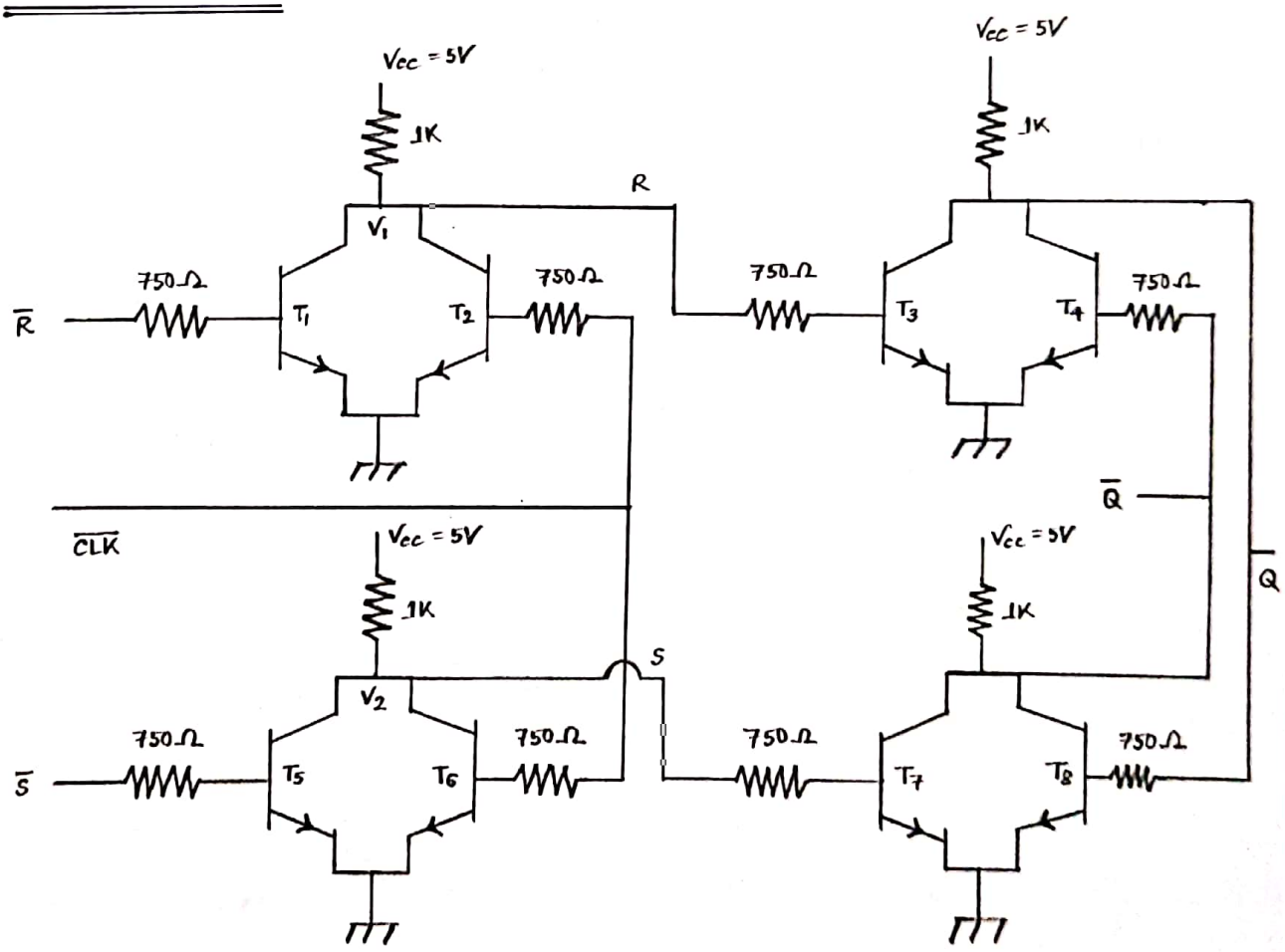

Figure : Experiment 5

Ans to the Questions :

① Analyze the operation of SR FF with the experimental data.

Ans: If we analyze the experimental data then -

$\bar{S}$	$\bar{R}$	Q_t	Q_{t+1}
5.00	0.00	0.04	2.48
5.00	5.00	0.04	2.48
0.00	5.00	2.48	0.04
5.00	5.00	2.48	0.04

$\bar{S}$	$\bar{R}$	Q_t	Q_{t+1}
5.00	0.00	0.04	2.48
0.00	0.00	0.65	0.65
0.00	5.00	2.48	0.04
0.00	0.00	0.65	0.65

Here if the $\bar{S}$ is in high voltage and $\bar{R}$ is in low voltage output at Q_t come out as a low voltage of 0.04 volts and low voltage of 2.48 at Q_{t+1} and this means reset state of the flip flop. In case of again having two different combination of voltage in $\bar{S}$ and $\bar{R}$ for example $\bar{S}$ having low voltage 0.00 and $\bar{R}$ having high voltage 5.00

the output of Q_t comes to 2.18V and Q_{t+1} 0.04V which refers to the set condition of the flip flop. In case of $\bar{S}$, $\bar{R}$ having both voltages at higher phase the output voltage shows the previous value of the output which means it holds the previous value. And lastly when the combination of $\bar{S}$ and $\bar{R}$ holds the low voltage the output shows to a race around condition where the value changes. All of these characteristics of this circuit concludes that it is a SR flip flop.

② What is the race around condition in SR FF? Discuss with respect to the internal circuit.

Ans: Whenever the S and R inputs of all SR flipflop are at high voltages, the output becomes suddenly unstable and it is known as a Race

Around Condition. In this race around condition the state of flipflop keeps toggling which leads to an uncertainity to determine the output of the flip flop. This state is called Race Around Condition.

In this circuit if we consider the input of $(\bar{S}, \bar{R})$ we can see the output keeps toggling and thus we can find the race around state when each of the input voltages are at low scale. And thus the race around state shows uncertainity.

Experimental Data :

Table-1

$\bar{S}$	$\bar{R}$	Q_t	Q_{t+1}
5.00	0.00	0.04	2.48
5.00	5.00	0.04	2.48
0.00	5.00	2.48	0.04
5.00	5.00	2.48	0.04

Table- 2

$\bar{S}$	$\bar{R}$	Q_t	Q_{t+1}
5.00	0.00	0.04	2.48
0.00	0.00	0.65	0.65
0.00	5.00	2.48	0.04
0.00	0.00	0.65	0.65

Discussion of the findings :

From this experiment we learned about the characteristics of SR flip flop. We learned about the implementation of SR Flip flop with the help of RTL NOR Gate. As it was a clocked flip flop we get to know about the variations of clock pulse as well. We have experimented the different outputs in various combination and learned about the steps of it.