Date of Examination: 25/10/2021

## AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Department/School: Computer Science and Engineering Program: B.Sc. in Computer Science and Engineering Semester Final Examination: Fall 2020

Year: 3<sup>rd</sup> Semester: 1<sup>st</sup>

Course Number: CSE3109
Course Name: Digital System Design

Time: 02(Two) Hours Full Marks: 50

## Use single answer script

Instructions:	i)	Answer script should be hand written and should be written in A4 white paper. You must submit the hard copy of this answer script to the Department when the university reopens.				
	ii)	You must write the following information at the top page of each answer script:				
			_			
		Department:	Program:			
		Course no:	Course Title:			
		Examination:	<b>Semester (Session):</b>			
		Student ID:	Signature and Date:			
	iii)	Write down Student ID, Course	number and put your signature on top of every single page			
	of the answer script.					
	iv)	Write down page number at the	bottom of every page of the answer script.			
	v)	Upload the scan copy of your answer script in PDF format through provided google form				
			e., google classroom) using institutional email within the			
			lear and readable scan copy (uncorrupted) is your			
			he full page of your answer script. However, for clear and			
		~ -	wer script student should use only one side of a page for			
	• `	answering the questions.				
	vi)		maintain academic integrity, and ethics. You are not			
			n another individual and if taken so can result in stern			
	vii)	disciplinary actions from the un Marks allotted are indicated in t				
			ached at the end of the question paper. You may use graph			
	viii)	papers where necessary.	ached at the end of the question paper. Tou may use graph			
	ix)	Assume any reasonable data if i	needed			
	x)	Symbols and characters have th				
	xi)		OF file as CourseNo_StudentID.pdf			
	, AI)	For example, CSE 3109_18020	<u>=</u>			
	xii		pdf file) must be uploaded at designated location in the			
		provided <b>google form link</b> avai	lable in the google classroom.			

## There are 6 (Six) Questions. Answer any 4 (Four).

Ques	stion 1. [Mar	ks: 12.5]				
a)	Design an arithmetic circuit with two selection variables, $S_1$ and $S_0$ , which generates the following arithmetic operations. Draw the logic diagram of one typical stage.					[6]
		S <sub>1</sub>	S <sub>0</sub>	C <sub>in</sub> = 0	Cin = 1	
		0	0	F = A + B	F = A - B	
		0	1	F = A - 1	F = A + 1	
		1	0	F = B' - 1	F = B' + 1	
		1	1	F = A + B'	F = A + B' +1	
<b>b</b> )	Write short	notes on t	he followi	ng tonics:		[3]
ω,		erflow Fla		ing topics.		[0]
	ii. Zer	o Flag				
c)					e final carry bit if the operand is zero.	[3.5]
			m? Explaii	n with proper examples.		
	stion 2. [Mar					FA #3
a)	The circuit	output is e	equal to 1 i		umbers to check if they are equal. ual and 0 otherwise. Derive the	[2.5]
1 \	equation of			Cl. Cl. C. 1 1'	1 ' 17' 4 11 17	[7]
b)	to derive the			flip-flops for the state dia	ngram shown in <b>Figure 1</b> . Use K-maps	[6]
	x = 0 $y = 1$ $y = 0$ $y = 0$					
			x = 1 $y = 1$ Figu	x = 1, y = 0  11 $x = 1, y = 1$ The 1: State Diagram for parts of the parts of	x = 1 $y = 0$	
<b>c</b> )	What are th	ne differer	ices hetwe	en SRAM and DRAM9	Design a combinational circuit using a	[4]
c)			-Invert Ga	tes that generates the following $F_1(X, Y, Z) = \Sigma(0, 1, 2, F_2(X, Y, Z)) = \Sigma(1, 3, 6, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4,$	owing output: 4, 5)	[ <del>4</del> ]

Que	stion 3. [Marks: 12.5]				
<b>a</b> )	Why Double Handshake I/O is better than Single Handshake I/O? Write a control word for 8255 PPI configuring Port B and Port C <sub>L</sub> as an output port and Port A and Port C <sub>u</sub> as an input port and 8255 working in mode 0. Mention the significance of each bit position.				
<b>b</b> )	If we want to display the number: 74082, what will be the current required to drive the LEDs and the decoders in a directly driving seven segment LED?				
c)	Assume that SAP-2 has a clock frequency of 2 MHz. How much delay will the following SAP-2 subroutine produce? The required number of T-states for MVI = 7, DCR = 4, JZ = JNZ = 10 or 7, RET = 10.  MVI A, 0AH LOOP1: MVI B, 64H				
	LOOP2: MVI C, 47H  LOOP3: DCR C  JNZ LOOP3	[5.5]			
	DCR B JNZ LOOP2 DCR A				
	JNZ LOOP1  RET				
Que	stion 4. [Marks: 12.5]				
a)	Perform Modified Booth multiplication on 1010110011 x 1010110011.	[8] [4.5]			
<b>b</b> )	Write a program for SAP-1 to solve the following arithmetic problem: $18-16+25+30$ The numbers are in decimal form. Consider these numbers stored from memory address 9H.				
Que	stion 5. [Marks: 12.5]				
a)	Hand assemble the following program in SAP-2 starting from address 1162H.  MVI B, AFH DCR B JNZ 2000H JMP 1105H HLT	[4]			
<b>b</b> )	Write a program that subtracts (865) <sub>10</sub> from (2897) <sub>10</sub> and stores the answer in the H and L registers.				
c)	What is the purpose of using PORT C of 8255PPI? Write the steps of the data transfer in Input Mode 1 on Port B of 8255PPI. Mention necessary pin numbers, also draw the appropriate timing diagram.				
Que	stion 6. [Marks: 12.5]				
a)	Consider a sequential circuit with two T flip-flops A and B, two inputs x and y, and one output z is specified by the following next-states and output equation: $A\ (t+1) = x\ y + xB$ $B\ (t+1) = x\ A + yB$ $z = AB$	[6.5]			
	1	Page 3 of 4			

	Design a state table for the two T flip-flops and determine the functions of these two T FFs. You must simplify the functions using K-map.	
<b>b</b> )	The state diagram of a control unit is shown in <b>Figure 2</b> . It has four states and two inputs I and R. You must represent the 00 state as T <sub>0</sub> , 01 state as T <sub>1</sub> , 10 state as T <sub>2</sub> , and 11 state as T <sub>3</sub> . Design the control using a PLA.  I=R=0  I=R=0  I=R=0  I=R=0  Figure 2: State Diagram for problem 6(b)	[6]