AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Department of Computer Science and Engineering

DIGITAL LOGIC DESIGN LAB

CSE 2106

Experiment No : 08

Experiment Name : (a) Design a 4-Bit CLA (Carry Look Ahead) Adder circuit.

(b) Design a Magnitude Comparator for 4-Bit Using Logic Gates.

Submitted by

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Experiment Name :

(a) Design a 4 bit CLA (Carry Look Ahead) Adder circuit.

Objective :

A carry look ahead adder improves speed by reducing the amount of time required to determine carry bits. It can be constructed with the simpler, but usually slower, ripple carry adder (RCA), for which the carry bit is calculated along side the sum bit and each stage must wait until the previous carry bit has been calculated to begin calculating its own sum and carry bit. The carry look ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the longer value bits of the adder.

Truth Table :

Full Adder

Input			Output	
A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Function Evaluation using K-map :

$$S = \Sigma(1,2,4,7)$$

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$		1		1
A	1		1	

$$\therefore \quad S = A\bar{B}\bar{C} + \bar{A}\bar{B}C + ABC + \bar{A}B\bar{C}$$

$$= \bar{A}(\bar{B}C + B\bar{C}) + A(BC + \bar{B}\bar{C})$$

$$= \bar{A}(B \oplus C) + A(\overline{B \oplus C})$$

$$= A \oplus B \oplus C$$

$$= A \oplus B \oplus C_{in}$$

$C_{out} = \Sigma(3,5,6,7)$

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$			1	
A		1	1	1

$$\therefore \; C_{out} = AC + BC + AB$$

$$= AB + ABC + A\bar{B}C + ABC + \bar{A}BC$$

$$= AB + ABC + C(A\bar{B} + \bar{A}B)$$

$$= AB(C+1) + C(A \oplus B)$$

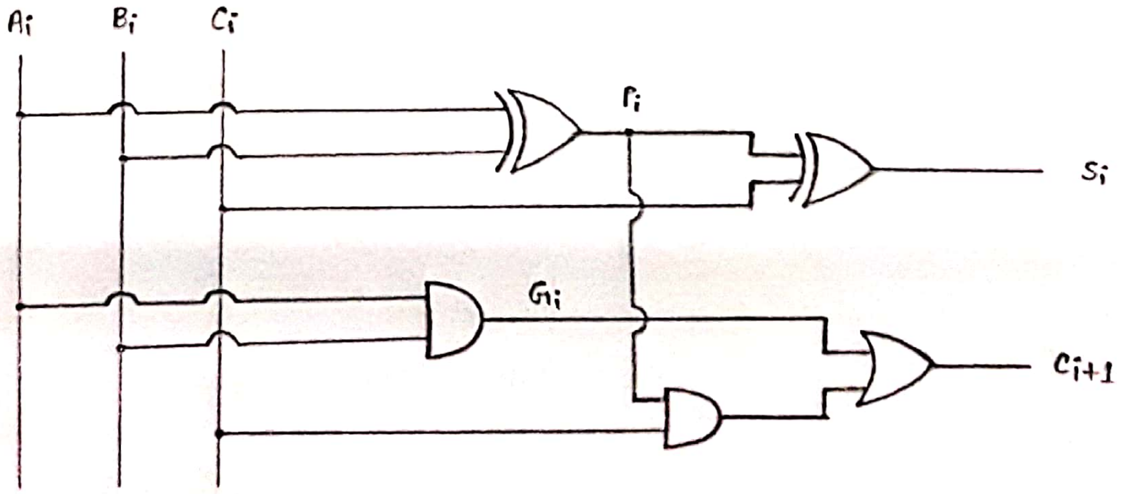
$$= AB.1 + C(A \oplus B)$$

$$= AB + C_{in}(A \oplus B)$$

Now,

$$S = A_i \oplus B_i \oplus C_{in}$$

$$C_{out} = AB + C_i(A \oplus B)$$



Here,

$P_i = A_i \oplus B_i$ $\qquad$ $S_i = P_i \oplus C_i$

$G_i = A_i B_i$ $\qquad$ $C_{i+1} = G_i + P_i C_i$

Now,

1st bit :-

$P_1 = A_1 \oplus B_1$

$G_1 = A_1 B_1$

$S_1 = P_1 \oplus C_1 = A_1 \oplus B_1$

$C_1 = 0$

2nd bit :-

$P_2 = A_2 \oplus B_2$

$G_2 = A_2 B_2$

$C_2 = G_1 + P_1 C_1$

$= A_1 B_1 + (A_1 \oplus B_1) . 0$

$= A_1 B_1$

$S_2 = P_2 \oplus C_2$

$= (A_2 \oplus B_2) \oplus A_1 B_1$

3rd bit :-

$P_3 = A_3 \oplus B_3$

$G_3 = A_3 B_3$

$C_3 = G_2 + P_2 C_2$

$= A_2 B_2 + (A_2 \oplus B_2) A_1 B_1$

$S_3 = P_3 \oplus C_3$

$= A_3 \oplus B_3 \oplus (A_2 B_2 + (A_2 \oplus B_2) . A_1 B_1)$

4th bit :-

$$P_4 = A_4 \oplus B_4$$

$$G_4 = A_4 B_4$$

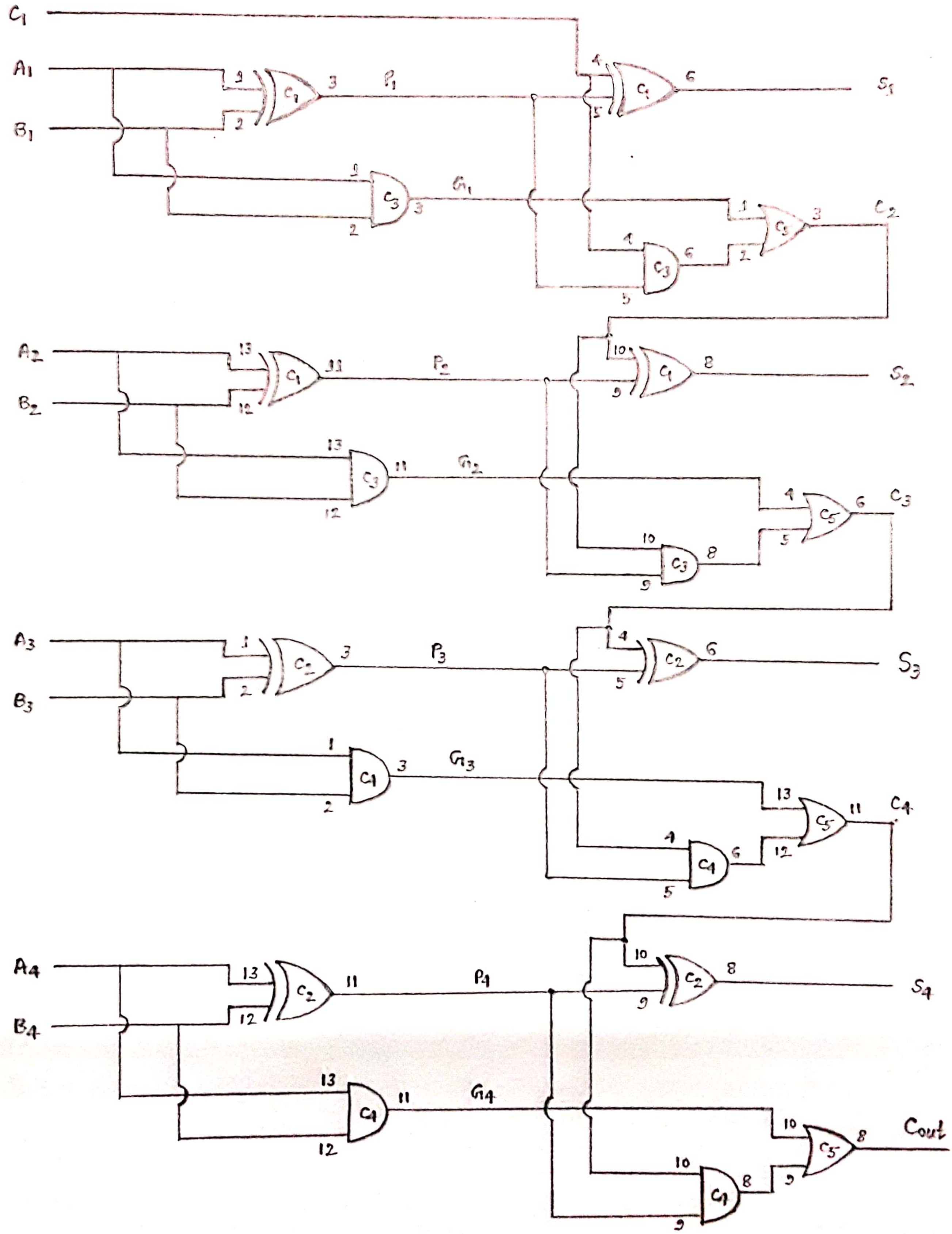
$$C_4 = G_3 + P_3 C_3$$

$$= A_3 B_3 + (A_3 \oplus B_3) \left[A_2 B_2 + (A_2 \oplus B_2) . A_1 B_1 \right]$$

$$S_4 = P_4 \oplus C_4$$

$$= A_4 \oplus B_4 \oplus \left[A_3 B_3 + (A_3 \oplus B_3) . \left[A_2 B_2 + (A_2 \oplus B_2) . A_1 B_1 \right] \right]$$

Circuit Diagram :



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Truth Table :

For checking our constructed circuit the following truth table will be used :

Input									Output				
A_4	A_3	A_2	A_1	B_4	B_3	B_2	B_1	C_0	C_{out}	S_4	S_3	S_2	S_1
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0	0	0	0	0	1
1	0	0	0	1	0	0	0	0	1	0	0	0	0
1	0	1	1	0	1	0	0	0	0	1	1	1	1
1	1	1	1	1	1	1	1	0	1	1	1	1	0

IC Requirements :-

1. C_1, C_2 → 7486 → XOR Gate – 2 piece
2. C_3, C_4 → 7408 → AND Gate – 2 piece
3. C_5 → 7432 → OR Gate – 1 piece

Conclusion :

In this experiment we came to know that the carry look ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits of the adder. We had G_i which is a carry generator and produces output carry and P_i is called carry propagation which propagates the carry from previous stage. The experiment was done successfully.

(b) Design a Magnitude Comparator for 4-Bit Using Logic Gates.

Objective :

A magnitude comparator circuit is a combinational circuit that compares two digital or binary numbers in order to find out whether one binary number is equal or less than or greater than the other binary numbers.

We logically design a circuit for which we will have two inputs one for A and other for B and have three output terminals, one for $A > B$ condition, one for $A = B$ condition and one for $A < B$ condition. The main objective of this experiment is to design a magnitude comparator for 4 bit using logic gates.

Truth Table :

Input		Output		
A	B	A>B	A=B	A<B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

∴ Expression,

$$A > B \Rightarrow A_i \overline{B_i}$$

$$A = B \Rightarrow \overline{A_i}\,\overline{B_i} + A_i B_i \quad = \overline{A_i \oplus B_i}$$

$$A < B \Rightarrow \overline{A_i} B_i$$

For 1 bit :-

$$A = A_1 , \quad B = B_1$$

$$A > B \Rightarrow A_1 > B_1$$

$$= A_1 \overline{B_1}$$

For 2 bit :-

$$A = A_2A_1 \quad , \quad B = B_2B_1$$

$$A>B \Rightarrow (A_2>B_2) + (A_2=B_2)\,(A_1>B_1)$$

$$= A_2\overline{B_2} + \overline{A_2 \oplus B_2} \cdot (A_1\overline{B_1})$$

$$A=B \Rightarrow (A_2=B_2) \cdot (A_1=B_1)$$

$$= (\overline{A_2 \oplus B_2}) \cdot (\overline{A_1 \oplus B_1})$$

$$A<B \Rightarrow (A_2<B_2) + (A_2=B_2)\,(A_1<B_1)$$

$$= \overline{A_2}B_2 + \overline{A_2 \oplus B_2} \cdot \overline{A_1}B_1$$

For 3 bit :-

$$A = A_3A_2A_1 \quad , \quad B = B_3B_2B_1$$

$$A>B \Rightarrow (A_3>B_3) + (A_3=B_3) \cdot (A_2>B_2) + (A_3=B_3)\,(A_2=B_2)\,(A_1>B_1)$$

$$= A_3\overline{B_3} + (\overline{A_3 \oplus B_3}) \cdot A_2\overline{B_2} + (\overline{A_3 \oplus B_3}) \cdot (\overline{A_2 \oplus B_2}) \cdot A_1\overline{B_1}$$

$$A=B \Rightarrow (A_3=B_3) \cdot (A_2=B_2) \cdot (A_1=B_1)$$

$$= (\overline{A_3 \oplus B_3}) \cdot (\overline{A_2 \oplus B_2}) \cdot (\overline{A_1 \oplus B_1})$$

$$A<B \Rightarrow (A_3<B_3) + (A_3=B_3)\,(A_2<B_2) + (A_3=B_3) \cdot (A_2=B_2)\,(A_1<B_1)$$

$$= \overline{A_3}B_3 + (\overline{A_3 \oplus B_3}) \cdot \overline{A_2}B_2 + (\overline{A_3 \oplus B_3}) \cdot (\overline{A_2 \oplus B_2}) \cdot \overline{A_1}B_1$$

For 4 bit :-

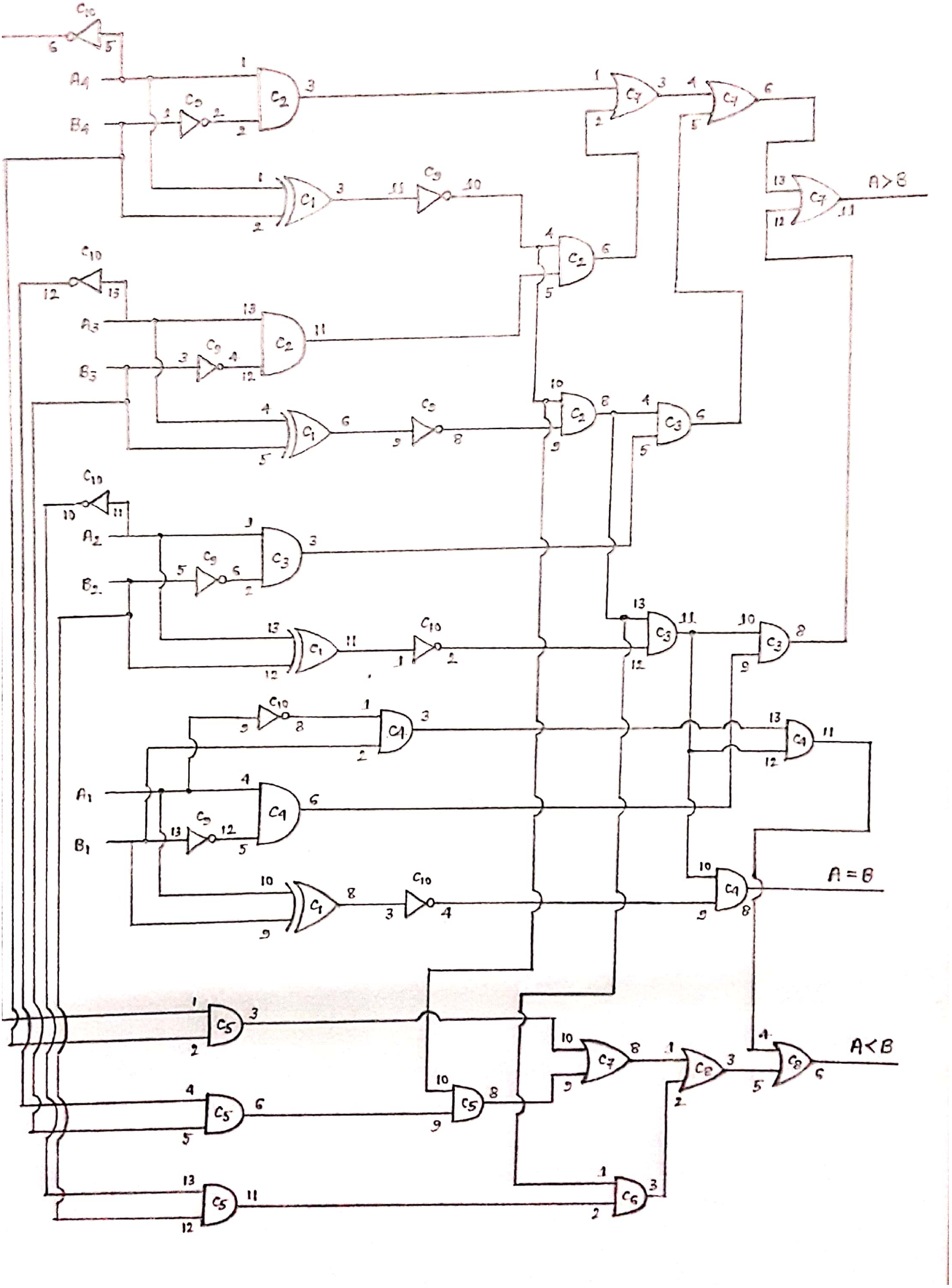
$$A = A_4A_3A_2A_1 \quad , \quad B = B_4B_3B_2B_1$$

$$A>B \Rightarrow (A_4>B_4) + (A_4=B_4).(A_3>B_3) + (A_4=B_4)(A_3=B_3)(A_2>B_2)$$
$$+ (A_4=B_4).(A_3=B_3).(A_2=B_2).(A_1>B_1)$$
$$= A_4\overline{B_4} + (\overline{A_4 \oplus B_4}).A_3\overline{B_3} + (\overline{A_4 \oplus B_4}).(\overline{A_3 \oplus B_3}).A_2\overline{B_2}$$
$$+ (\overline{A_4 \oplus B_4}).(\overline{A_3 \oplus B_3}).(\overline{A_2 \oplus B_2}).A_1\overline{B_1}$$

$$A=B \Rightarrow (A_4=B_4).(A_3=B_3).(A_2=B_2).(A_1=B_1)$$
$$= (\overline{A_4 \oplus B_4}).(\overline{A_3 \oplus B_3}).(\overline{A_2 \oplus B_2}).(\overline{A_1 \oplus B_1})$$

$$A<B \Rightarrow (A_4<B_4) + (A_4=B_4).(A_3<B_3) + (A_4=B_4)(A_3=B_3)(A_2<B_2)$$
$$+ (A_4=B_4).(A_3=B_3).(A_2=B_2).(A_1<B_1)$$
$$= \overline{A_4}B_4 + (\overline{A_4 \oplus B_4}).\overline{A_3}B_3 + (\overline{A_4 \oplus B_4}).(\overline{A_3 \oplus B_3}).\overline{A_2}B_2$$
$$+ (\overline{A_4 \oplus B_4}).(\overline{A_3 \oplus B_3}).(\overline{A_2 \oplus B_2}).\overline{A_1}B_1$$

Circuit Diagram :



IC Requirement :

1. C_1 → XOR Gate (7486) — 1 piece

2. C_2, C_3, C_4, C_5, C_6 → AND Gate (7408) — 5 piece

3. C_7, C_8 → OR Gate (7432) — 2 piece

4. C_9, C_{10} → NOT Gate (7404) — 2 piece

For checking our constructed circuit the following truth table will be used :

Input								Output		
A_4	A_3	A_2	A_1	B_4	B_3	B_2	B_1	$A>B$ (F_1)	$A=B$ (F_2)	$A<B$ (F_3)
0	0	0	1	0	0	0	0	1	0	0
0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	1	1	1	1	0	0	1
1	1	1	1	1	1	1	1	0	1	0

Conclusion :

In this experiment we had to use 10 IC's to design the magnitude comparator circuit. A proper connection must be ensured to get correct output as we used a good number of IC's. The experiment was done successfully.