CSE2209: Digital Electronics and Pulse Techniques

Course Conducted By:

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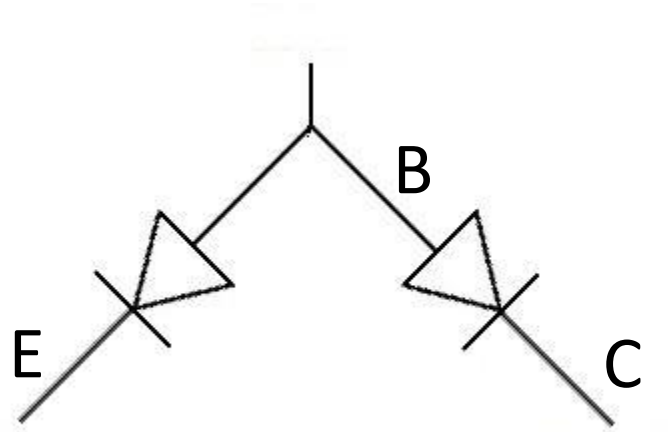
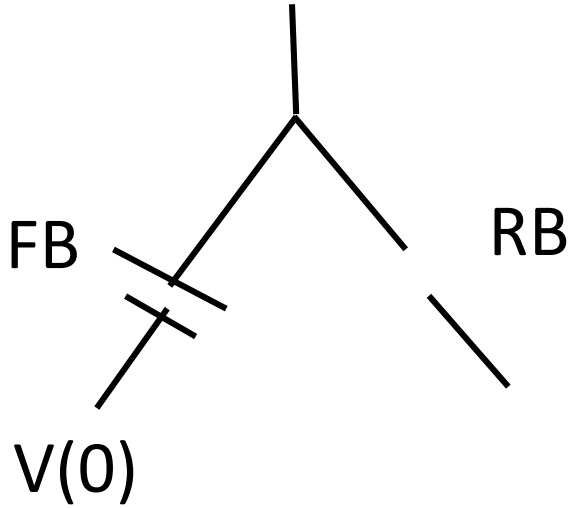
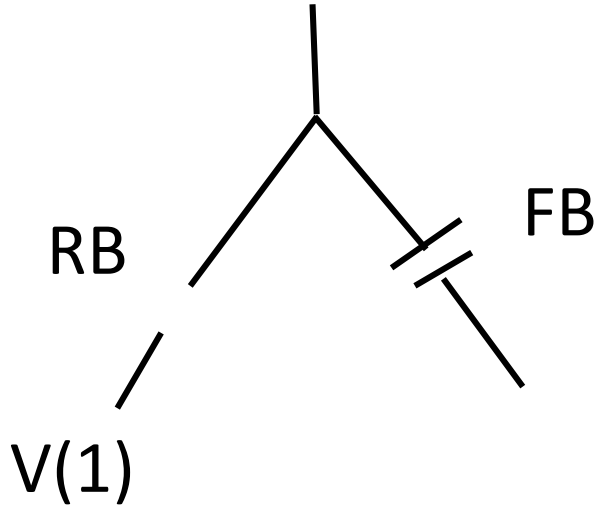
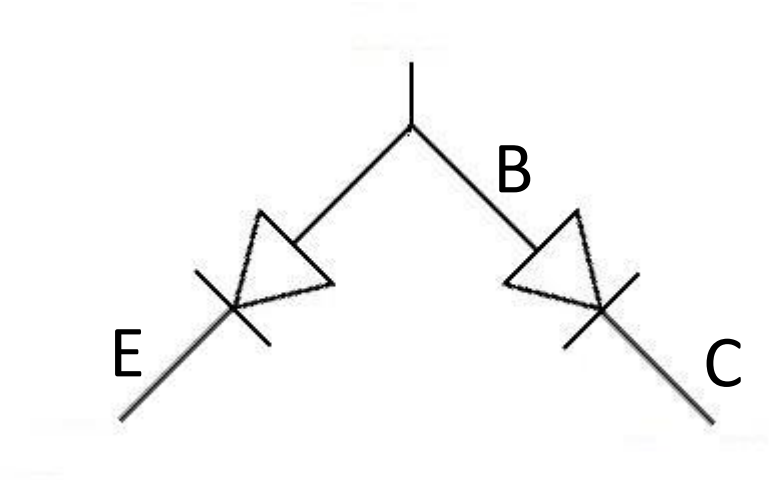
NPN Transistor

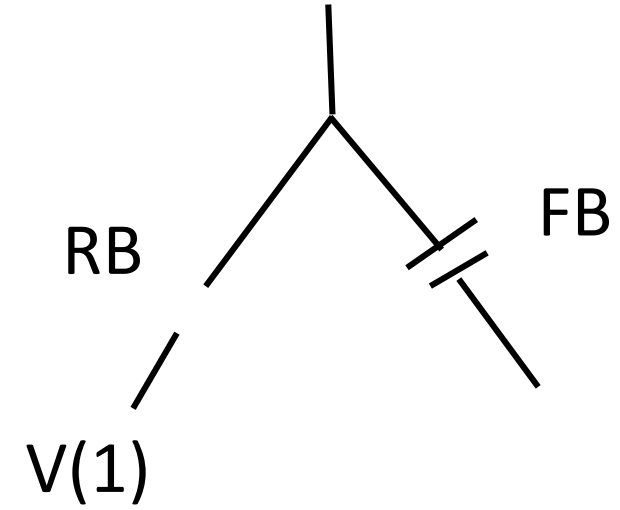






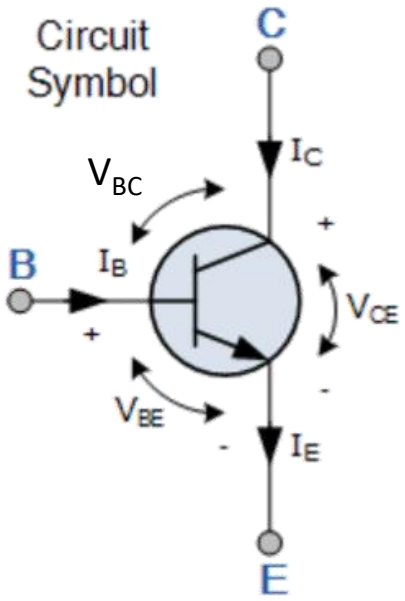
NPN Transistor Reverse Active Mode (h_{fe} <1)





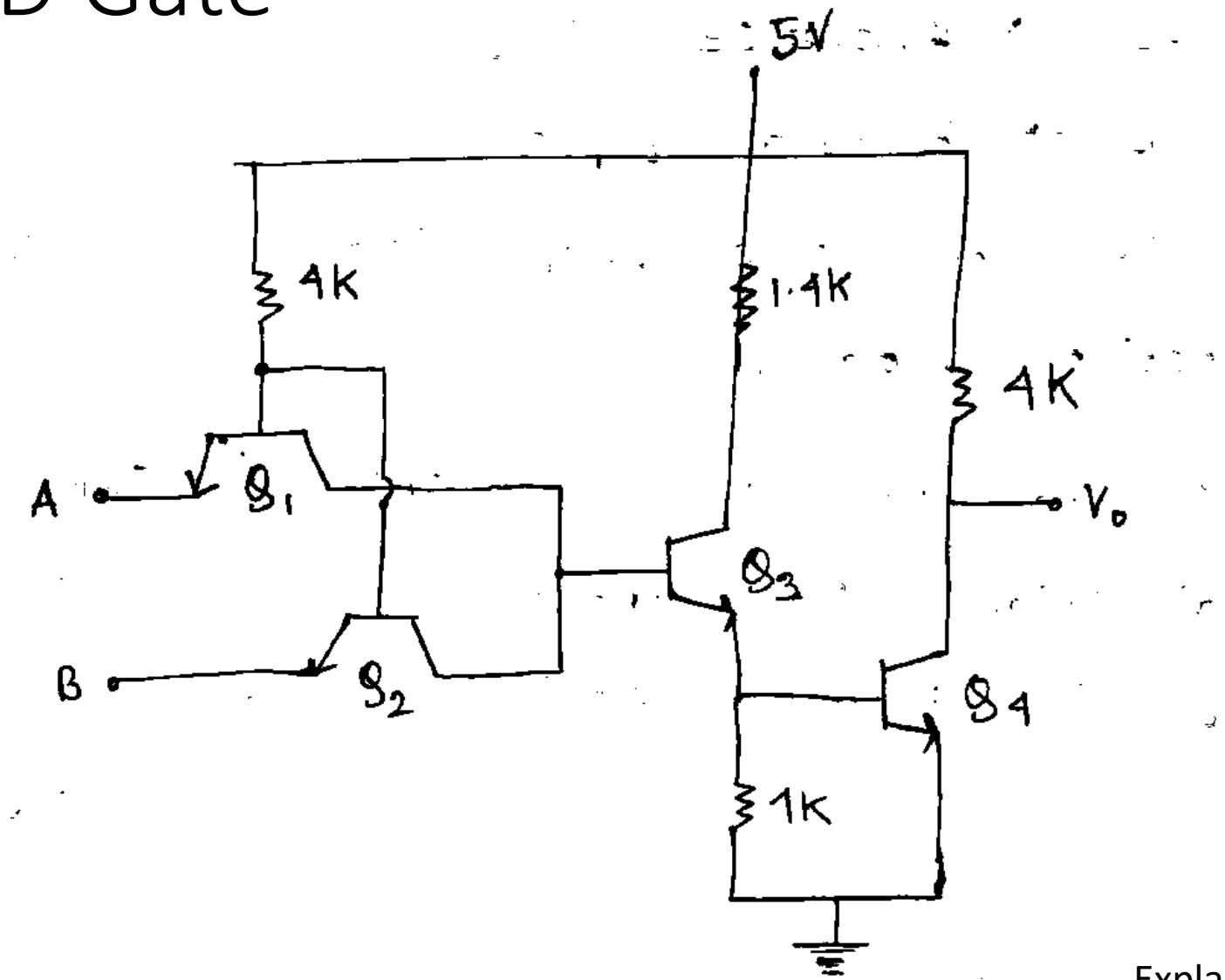
$$I_C = h_{fe} * I_B \quad \text{or} \quad I_B = \frac{I_C}{h_{fe}}$$

Collector becomes emitter and emitter becomes collector



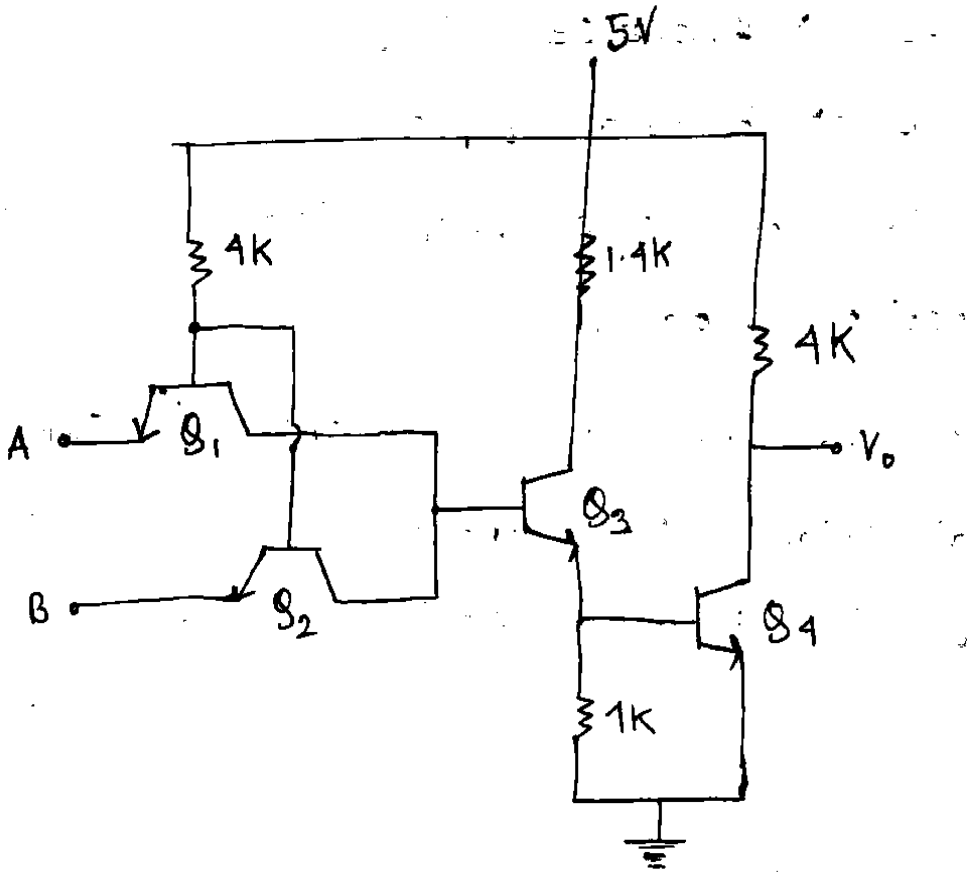
BE	BC	Transistor State
$(V_{BE} < 0.7V)$ R	$(V_{BC} < 0.7V)$ R	Cut off $I_C = I_B = I_E = 0$
$(V_{BE} > 0.7V)$ F	$(V_{BC} < 0.7V)$ R	Active $I_C = h_{fe} * I_B$
$(V_{BE} < 0.7V)$ R	$(V_{BC} > 0.7V)$ F	Inverse active $I_C = h_{fe} * I_B$
$(V_{BE} > 0.7V)$ F	$(V_{BC} > 0.7V)$ F	Saturation $I_C <= h_{fe} * I_B$ V_{CE} (sat) = 0.2V V_{BE} (sat) = 0.8V

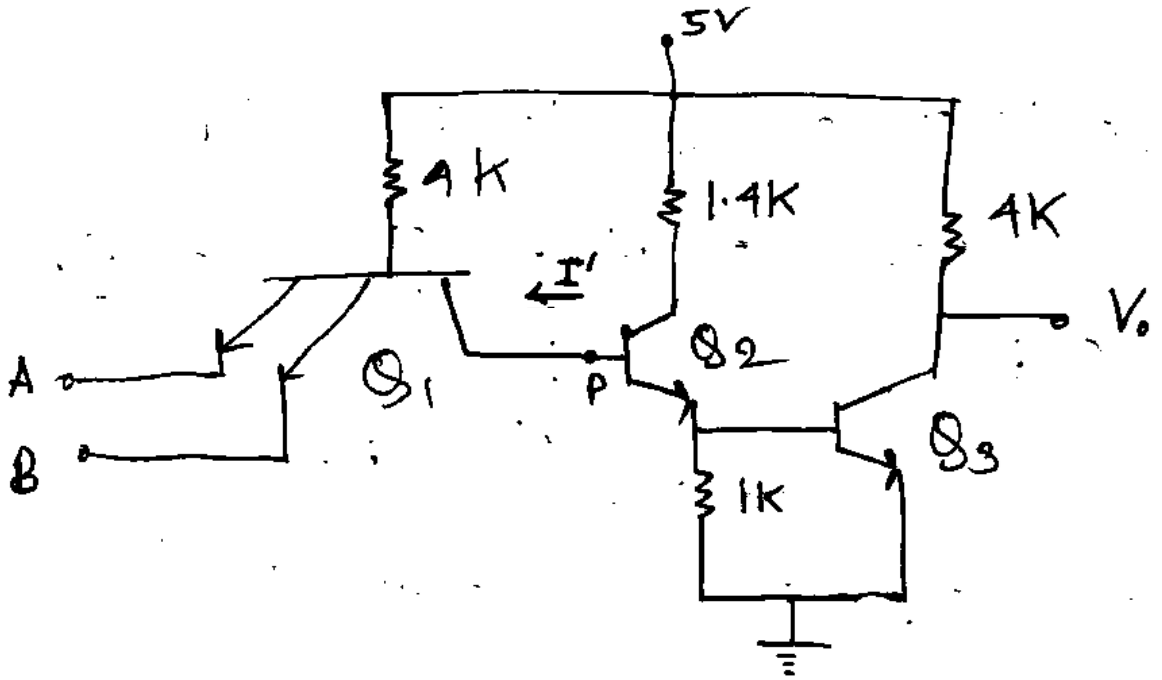
TTL NAND Gate



Explanation : 5.11 (Page 146)

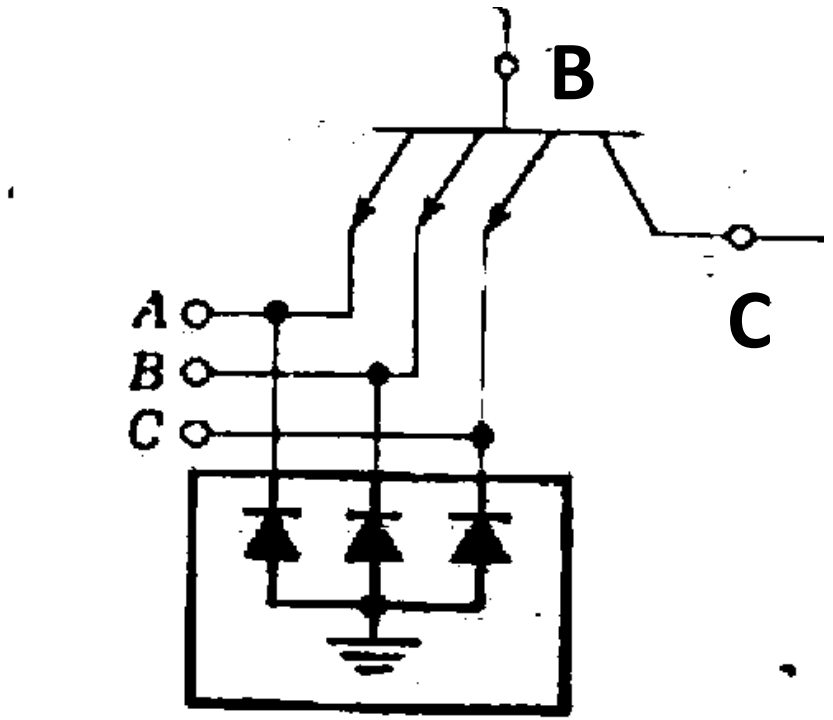
TTL NAND Equivalent Circuit





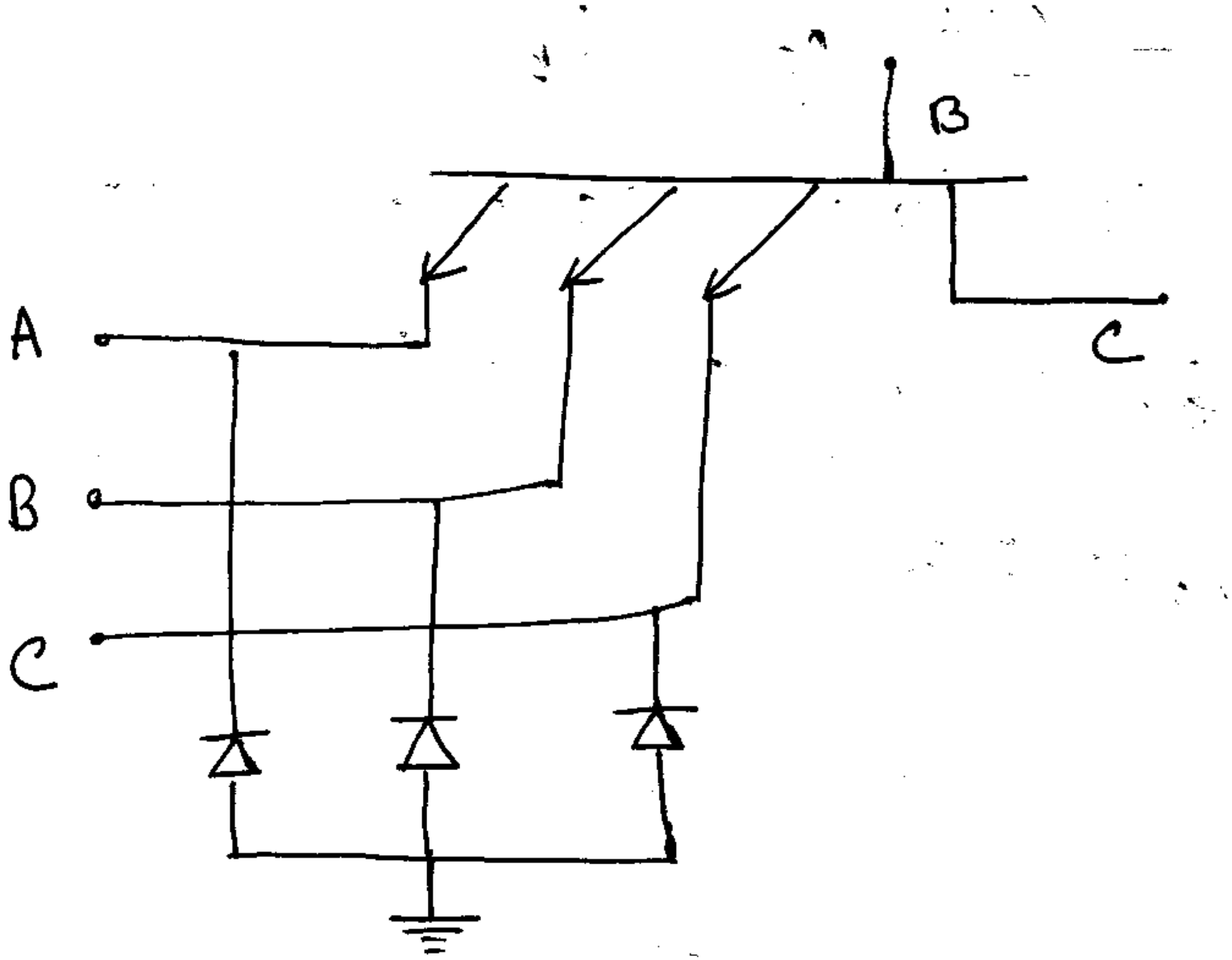
Clamping Diodes

PG - 147

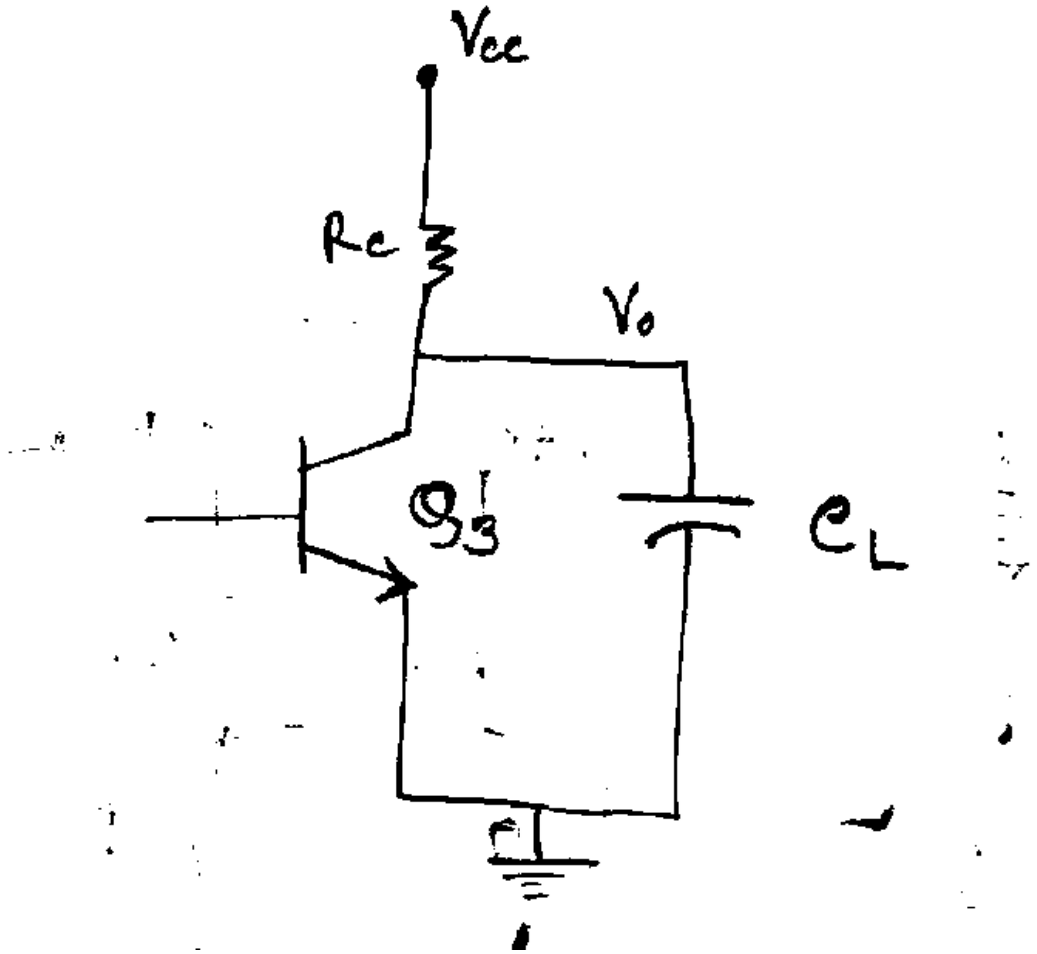


Input Clamping Diodes

These diodes (shown in the shaded block in Fig. 5-21) are often included from each input to ground, with the anode grounded. These diodes are effectively out of the circuit for positive input signals, but they limit negative voltage excursions at the input to a safe value. These negative signals may arise from ringing caused by lead inductance resonating with shunt capacitance.


B
A
B
C
C

Passive Pull Up Circuit



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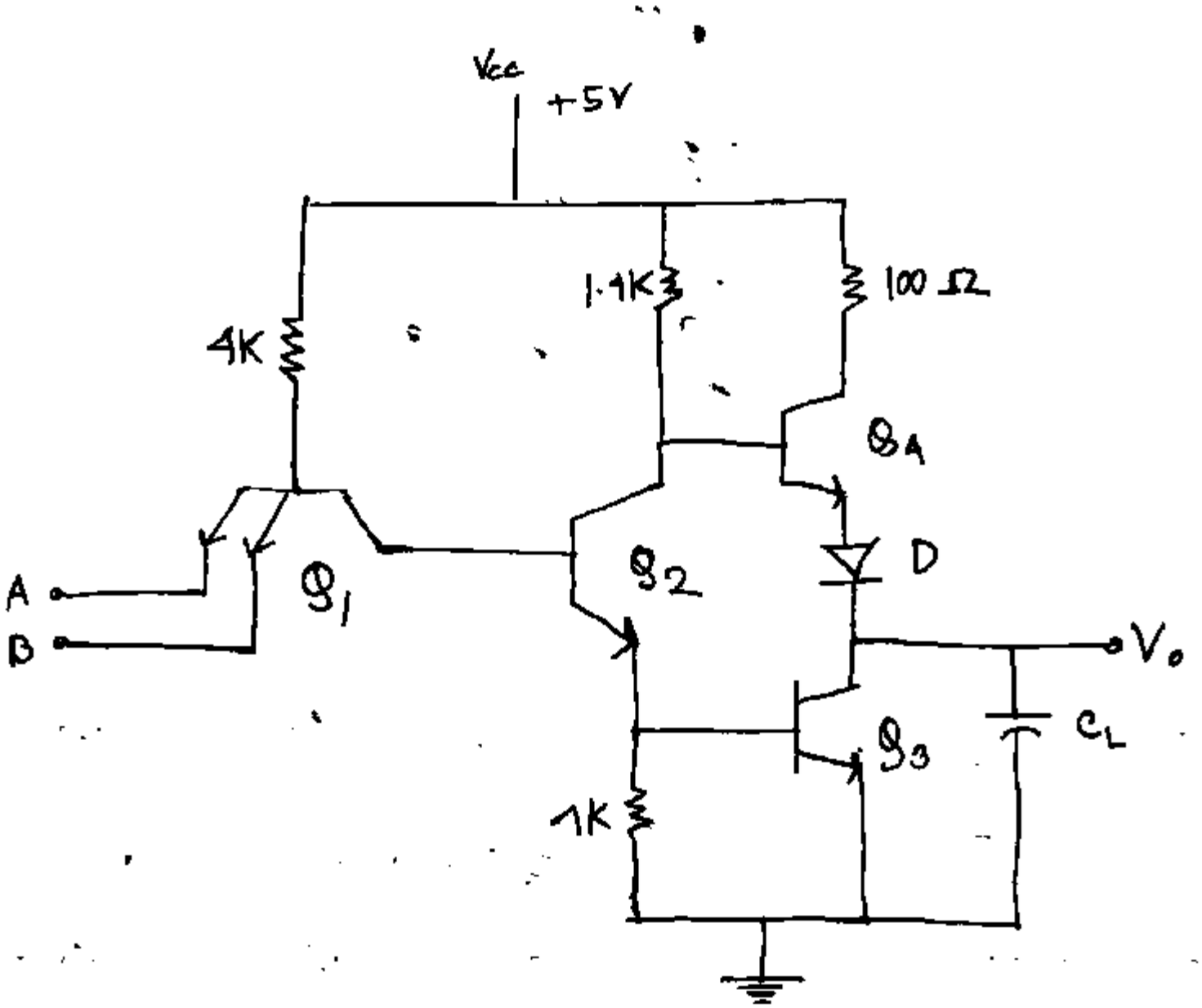
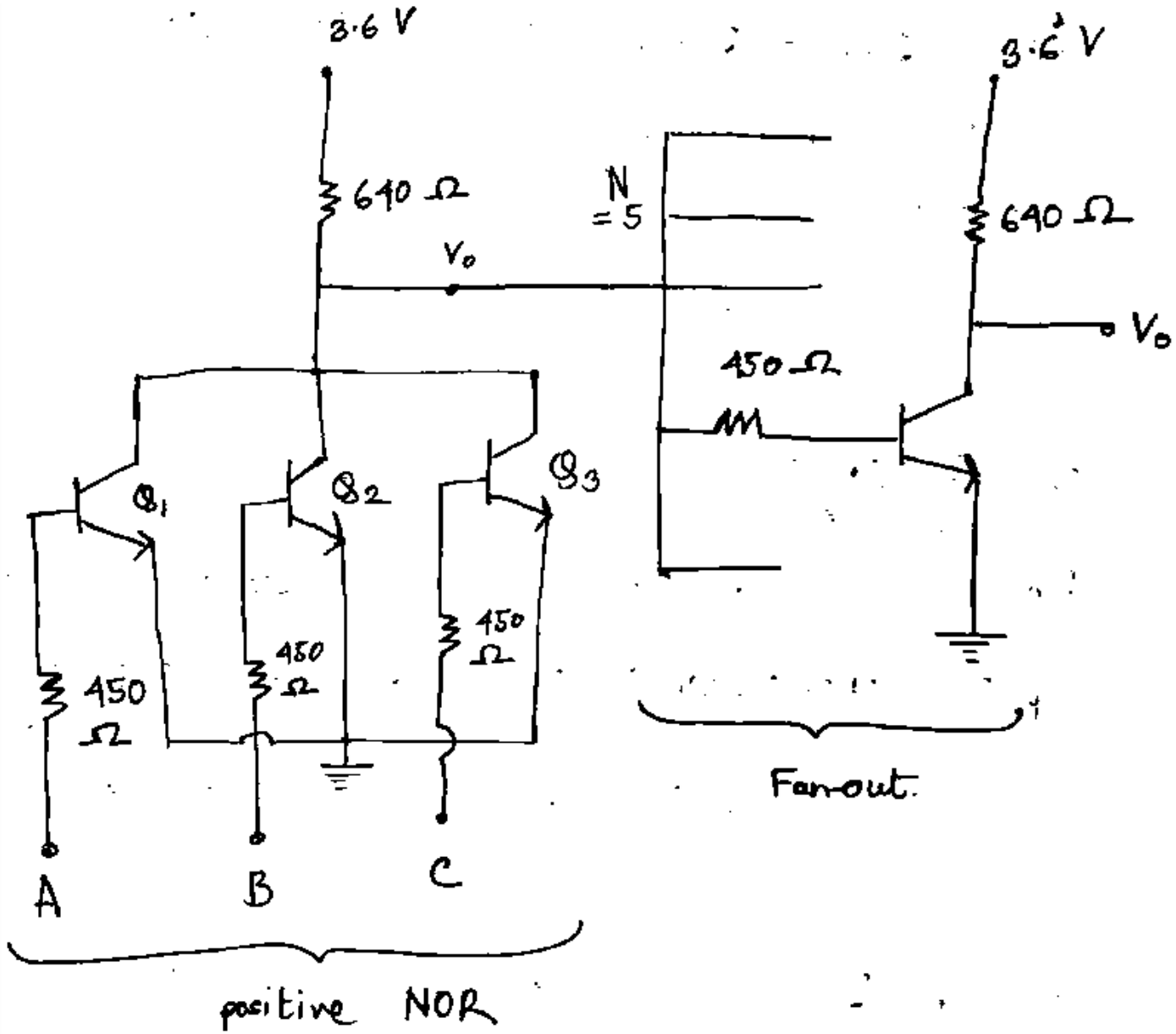
Wired End (Totem Pole)



Pg: 149-150

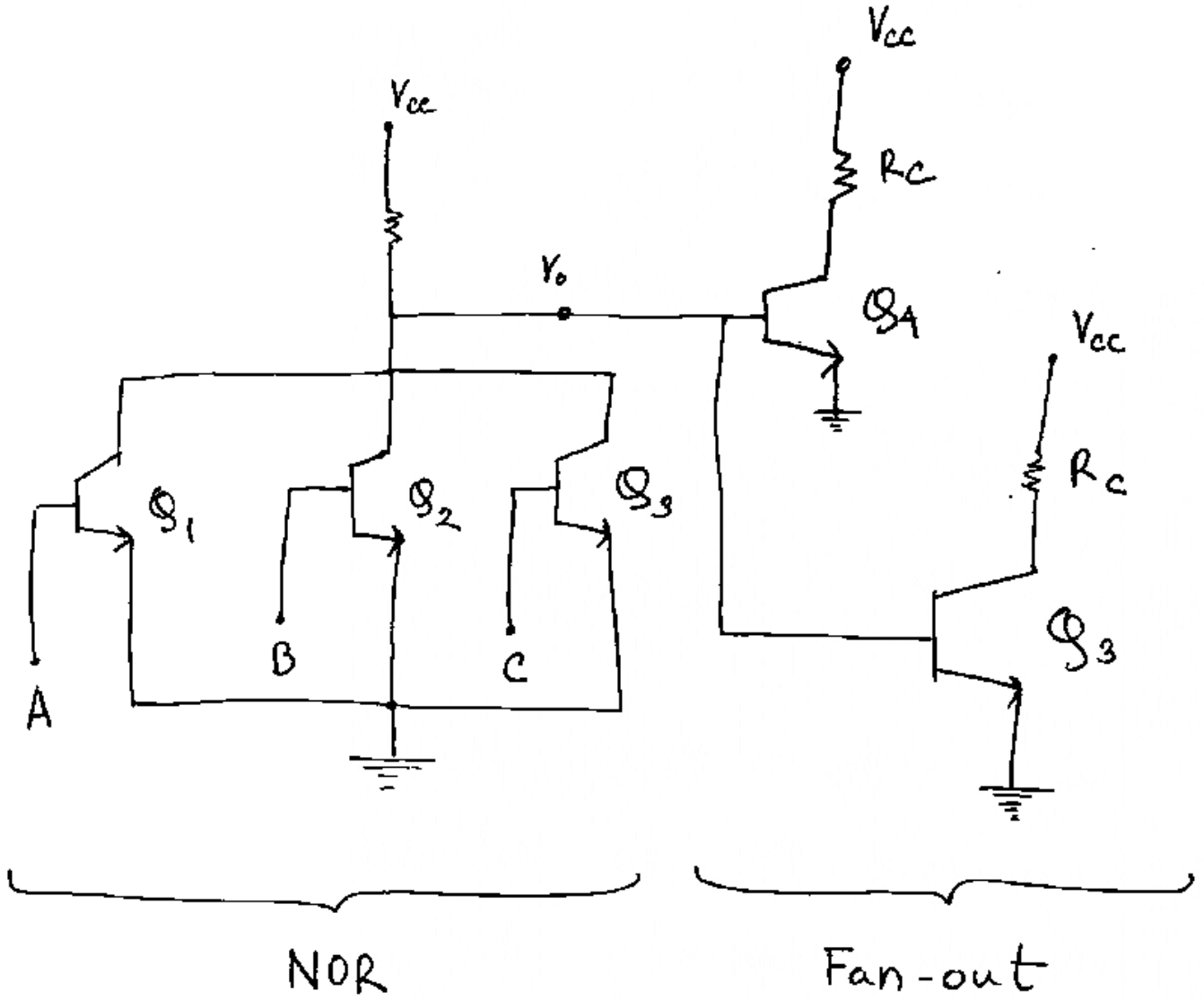
Resistor-Transistor Logic (RTL) NOR Gate (Positive Logic)

Pg. 152-153
(5.13)



Direct-coupled Transistor Logic (DCTL) NOR Gate (Positive Logic)

Pg. 152-155
(5.13)



DCTL

- Direct coupled transistor logic means inputs are directly coupled to the base of the transistor.
- DCTL circuits have fast switching speed.

Self Study:

- Advantages and Disadvantages of DCTL. (Pg. 154-155)