Ahsanullah University of Science and Technology (AUST)

Department of Computer Science and Engineering

LAB REPORT

Course No. : CSE2210

Course Title: Digital Electronics and Pulse Techniques Lab

Experiment Number: 02

Name of the Experiment: Study of a Transistorized NOT Gate.

Submitted By:

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Name of the Experiment :

Study of a transistorized NOT gate.

Objective :

The objective of this experiment is the study of a transistorized NOT gate and show the output voltage characteristics in graph by changing the values of resistances & V_i.

Circuit Diagram :

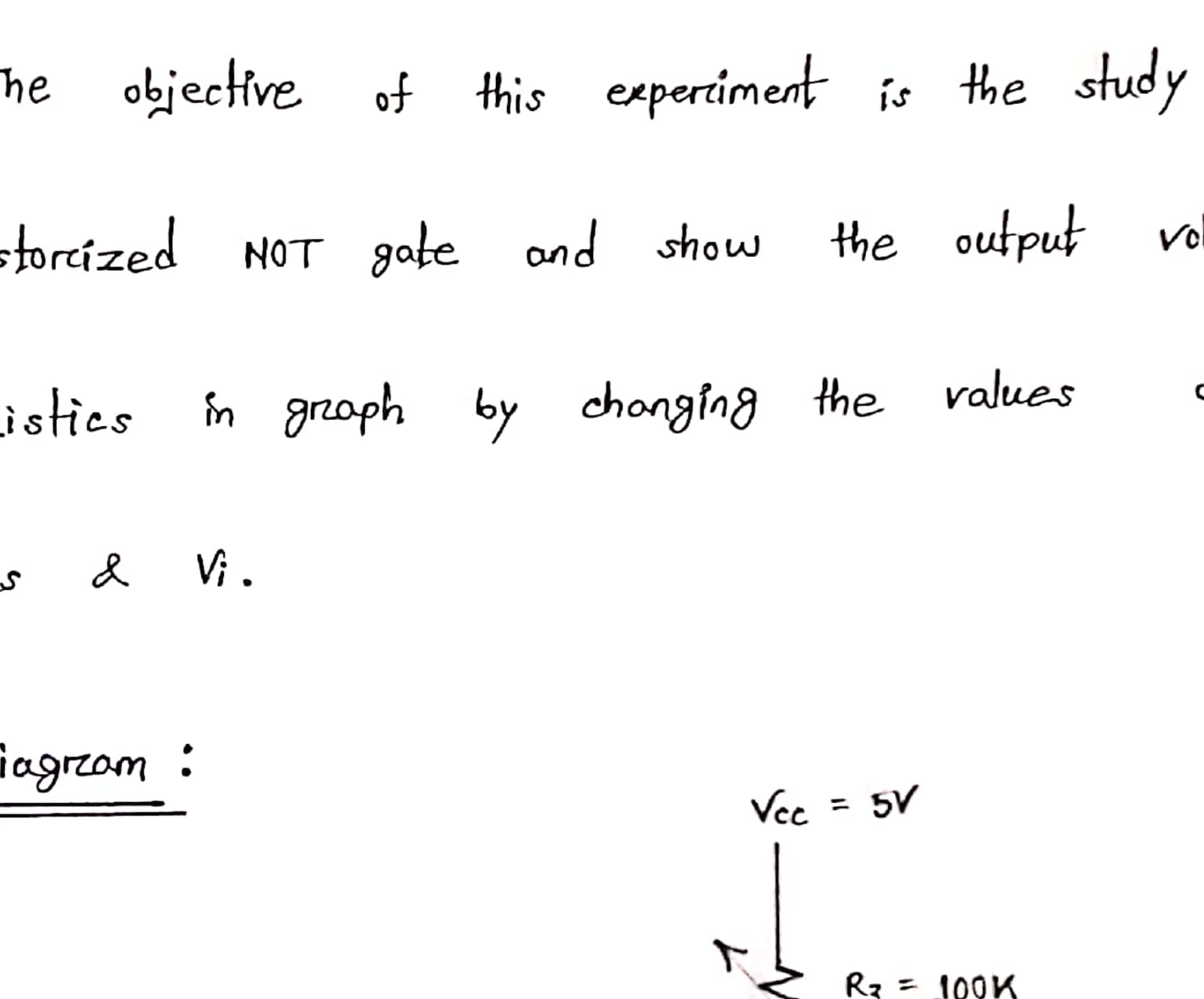


Fig : Circuit 1

Ans to the Questions :

① Which factors affect the switching speed of transistors and how ?

Ans : A transistors has an internal capacitive effect. When it is in transition from saturation mode to cut off mode, it does not happen immediately. That's because the internal capacity takes some time to discharge. After that the transistors will enters into the cut off mode. Also for this reason a non zero time is required for the interval capacity to charge up. So, this is how the interval capacitive effect affects the switching speed of the transistors.

② What is the effect of R1 ? Can it be very large ?

Ans: R_1 is mainly used as a current limiter for the given circuit. The optimum value of this resistance such that it doesn't affect the output (characteristic of NOT Gate) and the whole circuit is between 1.6KΩ to 3.2KΩ. If it becomes very large the circuit will lose its NOT gate property. In the given circuit input $V_i = 5V$ and $V_0 \approx 0V$ if it is to hold the NOT gate property.

If $R_1 = 2.5\,K\Omega$ when $R_2 = 90\,K\Omega$ and $V = -5V$

using superposition,

$$V_B = \frac{2.5}{2.5+90} \times (-5V) + \frac{90}{2.5+90} \times 5V$$

$$= 4.7297\ V$$

So, the transistor will be in saturation mode as it requires V_B to be at least 0.8V. As a result output V_o will be $V_o \approx 0V$ holding NOT gate property.

If $R_1 = 100\ K\Omega$ when $R_2 = 90K\Omega$ and $V = -5V$,

using superposition,

$$V_B = \frac{100}{100+90}(-5V) + \frac{90}{100+90} \times 5V$$

$$= 0.263\ V$$

So, the transistor will be in cut off mode with output voltage $V_o = 5V$ as $V_B < 0.5V$ which is required to be in cut in mode or $V_B < 0.8V$ which needs to be in saturation mode. Here, we get $V_o = 5V$ meaning V(1) output for V(1) input. So, NOT gate property is not holding in this case.

So, R_1 cannot be very large.

③ Are there any effects of temperature on circuit?

Ans: The change in temperature will effect the resistors in this circuit. If the temperature is increased then resistance is increased and resistance decreases for fall in temperature. Also the Q point of the transistor will change with respect to temperature change.

Experimental Data:

Procedure 01: vary R3 ⇒

V_i (V)	R_1 (KΩ)	R_2 (KΩ)	R_3 (KΩ)	V_0 (V)	V_B (V)
5V	2.5	90	0	4.99	0.64
5V	2.5	90	5	0.02	0.57
5V	2.5	90	20	0.02	0.57
5V	2.5	90	60	0.01	0.57
5V	2.5	90	80	0.01	0.57

Procedure 02: vary R_2 ⇒

V_i (V)	R_1 (KΩ)	R_2 (KΩ)	R_3 (KΩ)	V_c (V)	V_B (V)
5	2.5	0	40	5.00	-5.00
5	2.5	3	40	3.67	0.45
5	25	10	40	0.01	0.56
5	2.5	30	40	0.01	0.57
5	25	50	40	0.01	0.57
5	25	70	40	0.01	0.57

Procedure 03: vary R_1 ⇒

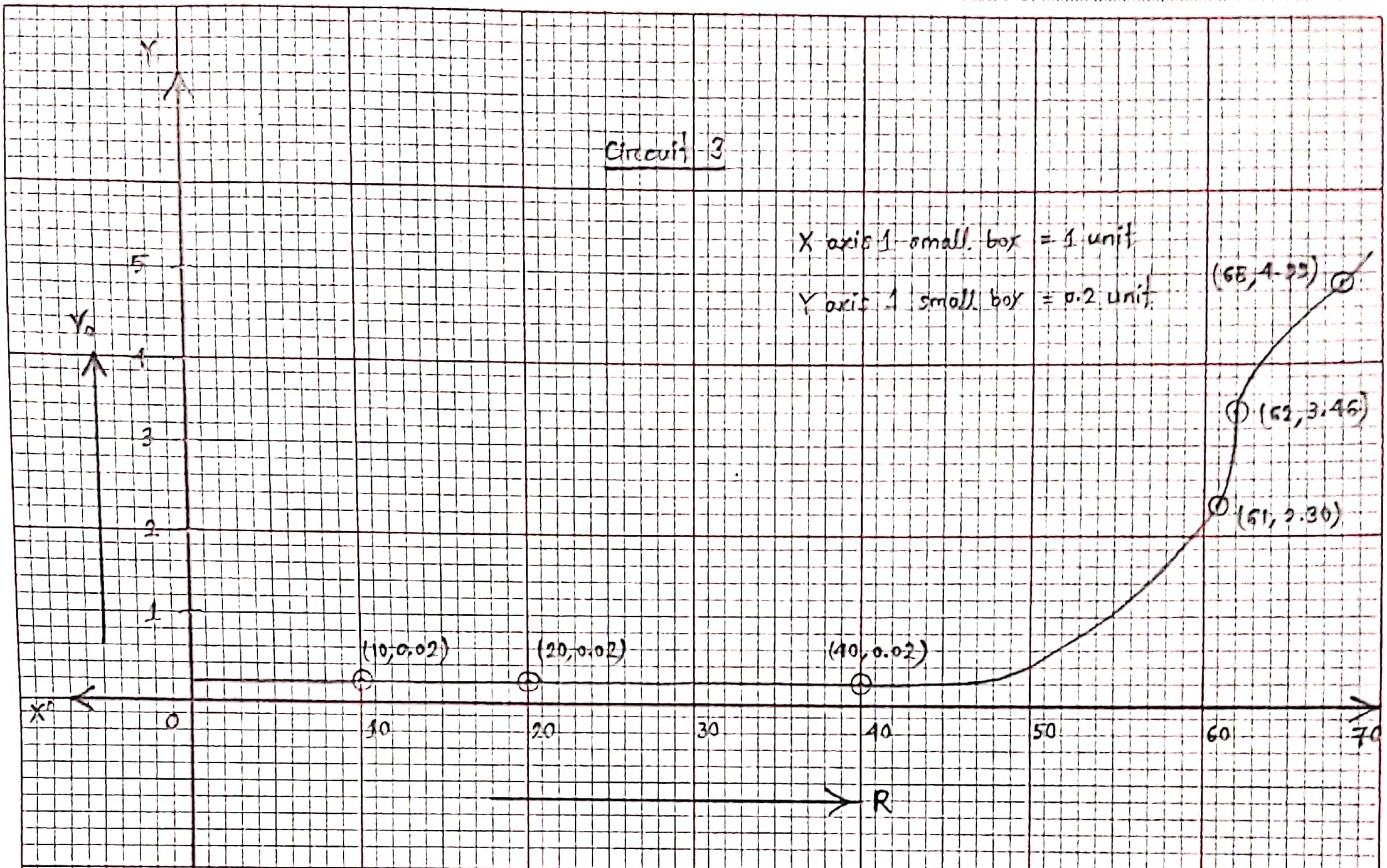
V_i (V)	R_1 (KΩ)	R_2 (KΩ)	R_3 (KΩ)	V_c (V)	V_B (V)
5	10	90	40	0.02	0.88
5	40	90	40	0.02	0.53
5	61	90	40	2.30	0.49
5	62	90	40	3.46	0.47
5	68	90	40	4.99	0.45
5	70	90	40	5.00	0.31
5	90	90	40	5.00	0.27

Roll No. .....

Circuit 3

X axis 1 small box = 1 unit

Y axis 1 small box = 0.2 unit



Circuit 4

X axis 1 small box = 0.1 unit

Y axis 1 small box = 0.2 unit

MICRO

Procedure 01 : vary V_i ⇒

V_i (V)	R_1 (KΩ)	R_2 (KΩ)	R_3 (KΩ)	V_o (V)	V_B (V)
0	2.5	90	40	5.00	−0.14
0.2	2.5	90	40	5.00	0.05
0.8	2.5	90	40	0.03	0.50
2	2.5	90	40	0.02	0.54
3	2.5	90	40	0.02	0.55
5	2.5	90	40	0.01	0.57

Discuss the findings :

In this experiment, the transistorized NOT gate has been implemented. The resistance of the circuit were fixed in a range to study about the characteristics of NOT gate. Then we changed the value of these resistance and measured the upper bound and lower bound of their value where the characteristics of NOT gate changed. The circuit was implemented carefully and measurements were taken accurately as possible.