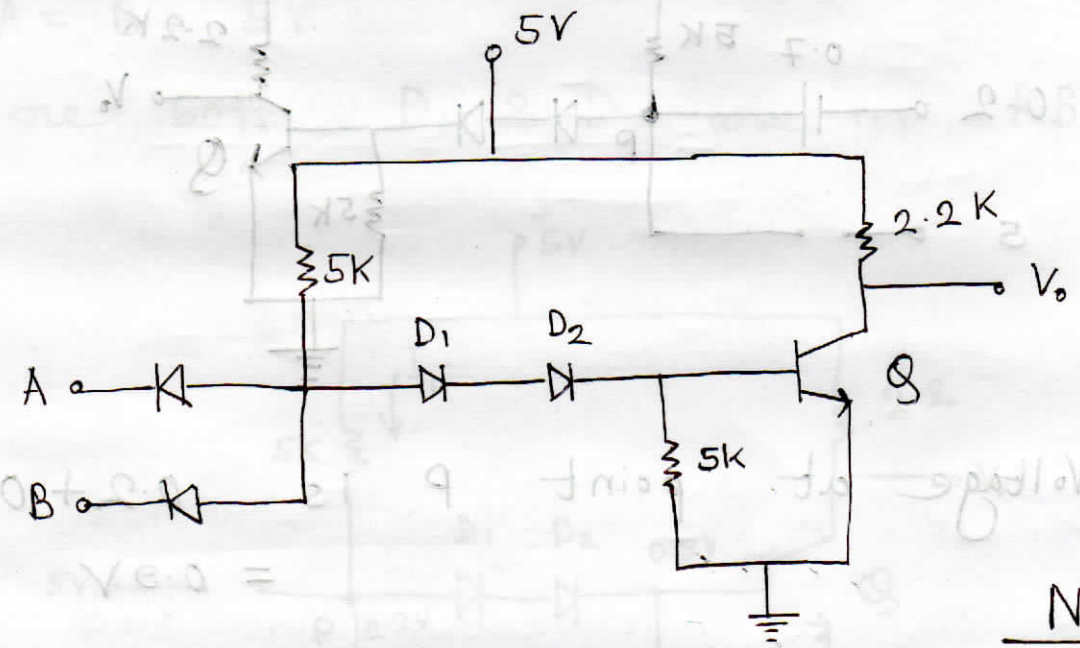
Integrated ckt DTL NAND gate : (positive logic)



NAND

A	B	V_o
0.2	0.2	5
0.2	5	5
5	0.2	5
5	5	0.2

Case 1 :

$A = B = 0.2V = V(0)$

For case 2 & 3,

$A = 0.2V = V(0)$, $B = 5V = V(1)$

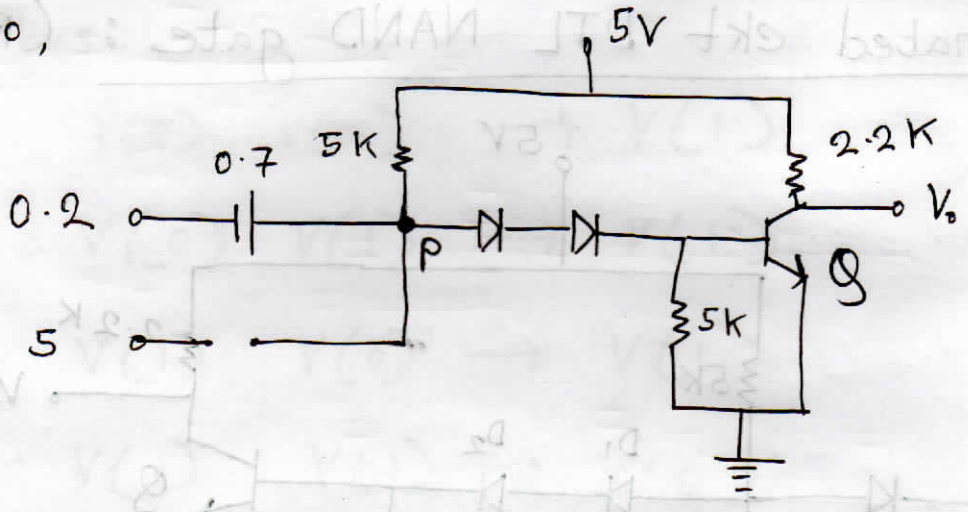
or, $A = 5V = V(1)$, $B = 0.2V = V(0)$

Let us do it for,

$A = 0.2V$ and $B = 5V$

So here diode across A input will be forward bias and B input will be reverse bias.

So,



Voltage at point P is $0.2 + 0.7$

$= 0.9V$

Minimum amount of voltage required at P to turn ON D_1 and D_2 is

$0.6 + 0.6 = 1.2V$

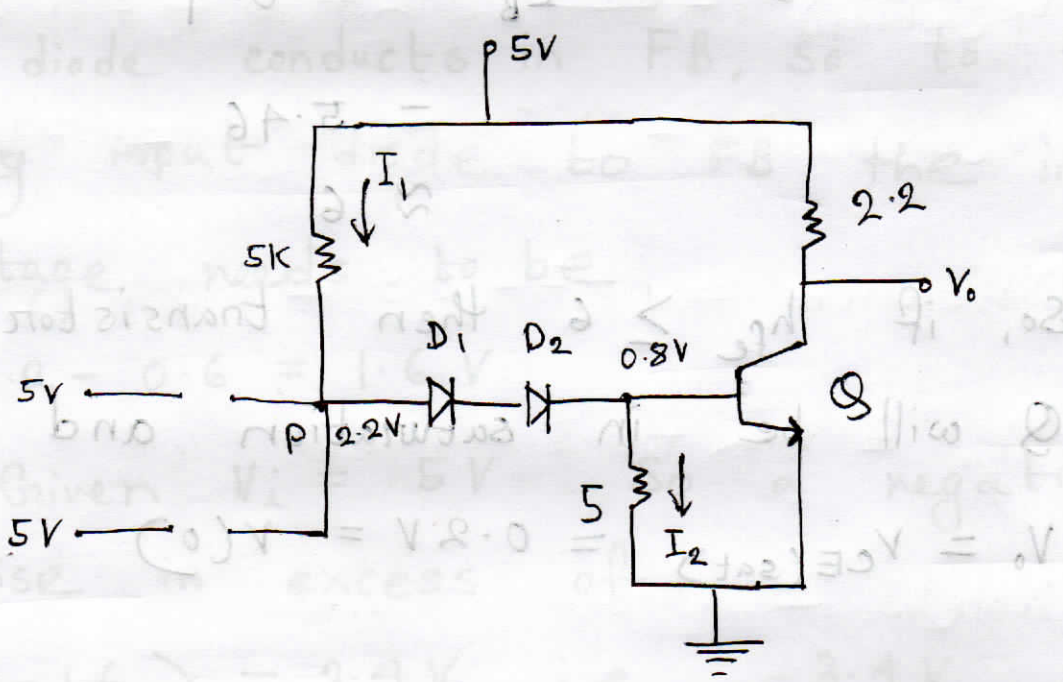
And, along with that to turn on Q we need 0.5 V. So at P we need total $(0.6 + 0.6 + 0.5) = 1.7V$

As, $V_{P(actual)} = 0.9V$ is not sufficient enough to turn on D_1, D_2 and transistor Q. So, $V_o = 5V = V(1)$

Case 2 :

A = B = 5V

Here both D_1 & D_2 are in RB.



Assuming that transistor Q is in saturation, Voltage at P,

$V_P = 0.8 + 0.7 + 0.7 = 2.2\,V$

$I_1 = \frac{5 - 2.2}{5} = 0.56\ mA$

$I_2 = \frac{0.8}{5} = 0.16\ mA$

$\therefore I_B = I_1 - I_2 = 0.56 - 0.16 = 0.4\,mA$

$$I_c = \frac{5 - 0.2}{2.2} = 2.182 \text{ mA}$$

$$\therefore h_{fe(min)} = \frac{I_c}{I_B} = \frac{2.182}{0.4}$$

$$= 5.46$$

$$\approx 6$$

So, if $h_{fe} \geq 6$ then transistor Q will be in saturation and

$$V_o = V_{CE(sat)} = 0.2\,V = V(0)$$

Noise Margin :

For the circuit of DTL NAND gate. Find NM(0) & NM(1).

NM(0) :

~~For~~ $\forall V_i = 5V$, output $V_o = 0.2\,V$

$= V(0)$

Then,

$V_p = 0.8 + 0.7 + 0.7 = 2.2\,V$

All input diodes are in reverse bias.

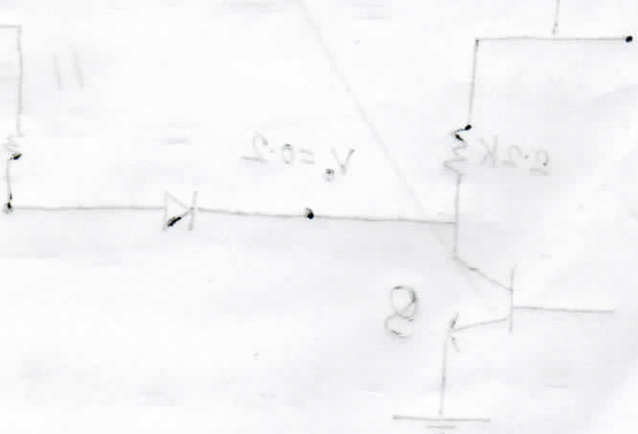
A diode conducts in FB, so to take any input diode to FB the input voltage needs to be,

$2.2 - 0.6 = 1.6\,V$

∵ Given $V_i = 5\,V$. So a negative noise in excess of

$(5 - 1.6) = 3.4\,V$ i.e $-3.4\,V$

must be present at input before ckt malfunctions. ∴ $NM(0) = -3.4\,V$



NM(1) :

If $\exists V_i = 0.2$ then $V_o = 5V = V(1)$

V_P (actual) = ~~0.9V~~ $0.2 + 0.7 = 0.9V$

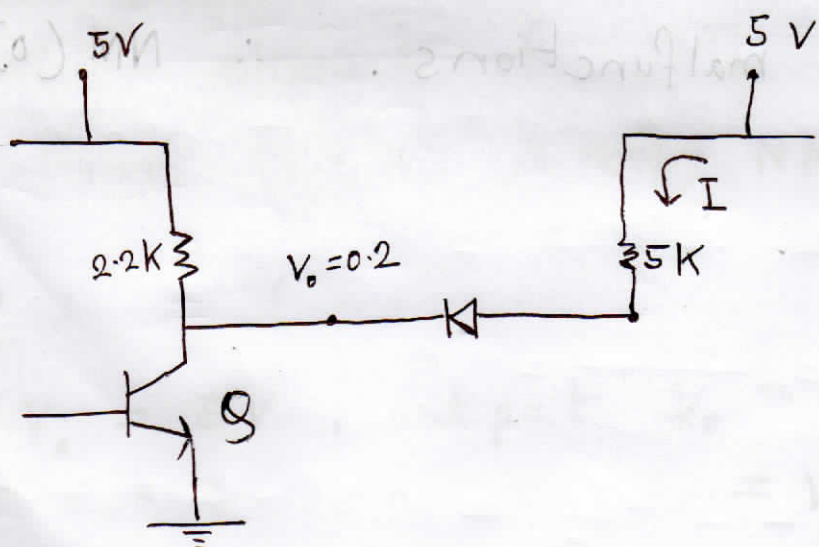
V_P (required) = $0.5 + 0.6 + 0.6 = 1.7V$

Difference = $1.7 - 0.9 = 0.8V$

$\therefore V_i = 0.2 + 0.8 = 1V$

NM(1) = $+0.8V$

Fan-out



$$I_{\bullet} = \frac{5 - 0.9}{5} = 0.82 \text{ mA}$$

We know, from case 2,

$I_B = 0.4$ mA and $I_C = 2.18$ mA

Let us consider, $h_{fe} = 30$

Then,

$$h_{fe} * I_B = 30 \times 0.4 = 12 \text{ mA}$$

So,

$$N * I + I_C < h_{fe} * I_B$$

or, $$N < \frac{h_{fe} * I_B - I_C}{I}$$

or, $$N < \frac{12 - 2.182}{0.82}$$

$\therefore N < 11.97$

So, $N_{(max)} = 11$

Power Dissipation :

$$P_{avg} = \frac{P(0) + P(1)}{2}$$

$P(0)$ = Power dissipation when $V_o = V(0)$

$P(1)$ = Power dissipation when $V_o = V(1)$

$P(0) = V \cdot I(0)$ and $P(1) = V \cdot I(1)$

When the ckt is in saturation mode,

$I(0) = I_1 + I_c = 0.56 + 2.182 = 2.742\,mA$

When in ~~sat~~ cut off,

$$I(1) = \frac{5 - 0.9}{5} = 0.82\,mA$$

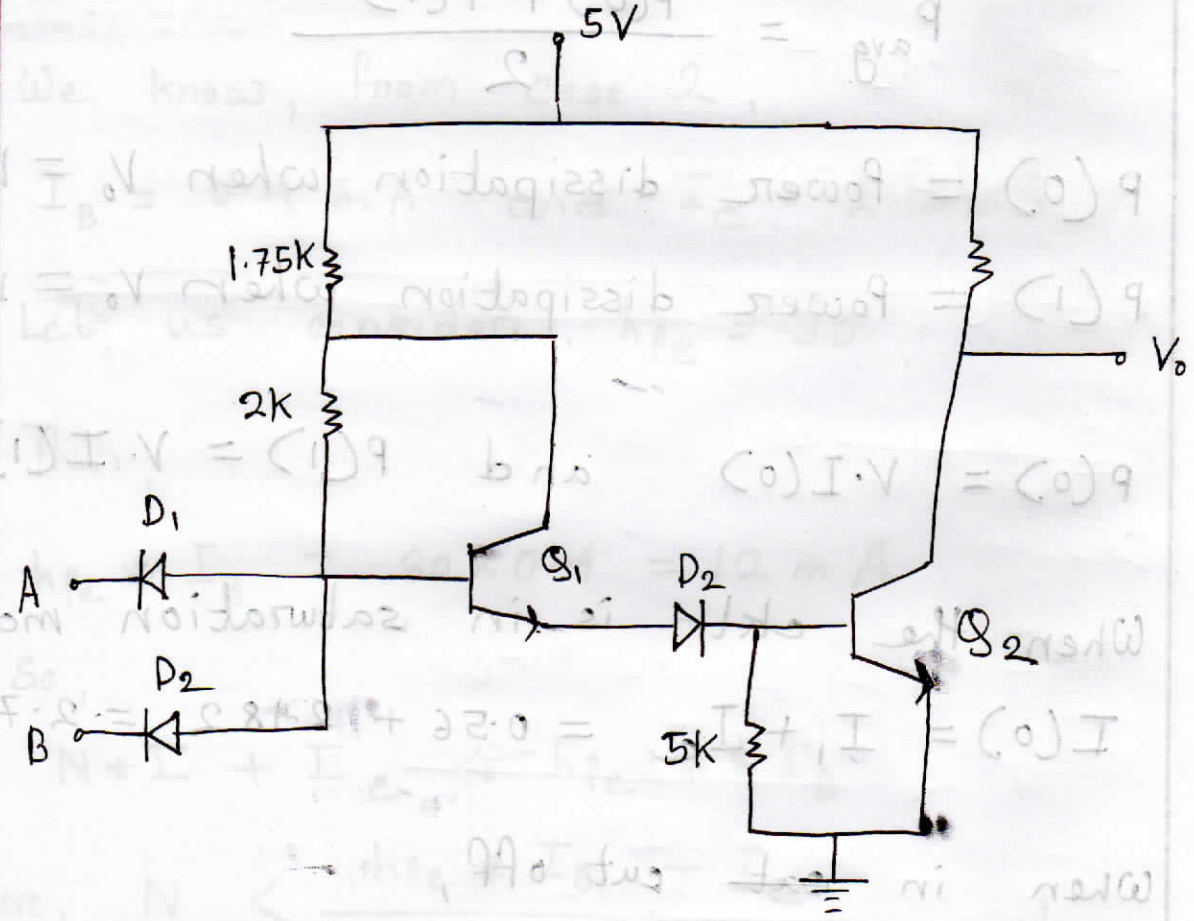
The highest voltage in a ckt is fixed & here $V = 5V$

$$\therefore P_{avg} = \frac{5(2.742 + 0.82)}{2}$$

$$= 8.905\,mW$$

DIY

DTL NAND Gate :



* Operations :
  - case 1
  - case 2
* Fan-in
* NM(0) / NM(1)
* Fan-out
* Power Dissipation