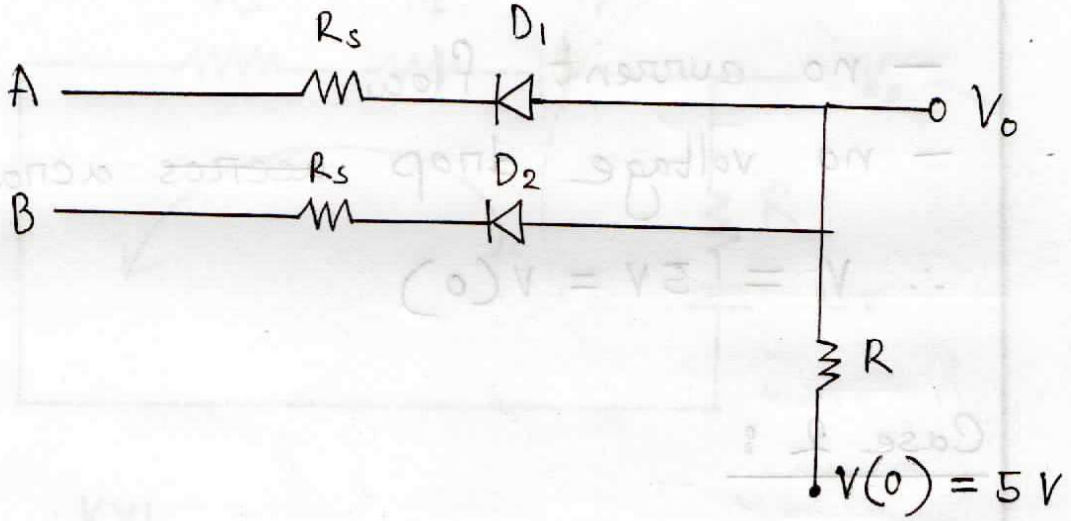
Negative Logic OR Gate

Negative logic means

$V(0) = 5V$

$V(1) = 0V$

A	B	V_o
V(0)	V(0)	V(0)
V(0)	V(1)	V(1)
V(1)	V(0)	V(1)
V(1)	V(1)	V(1)

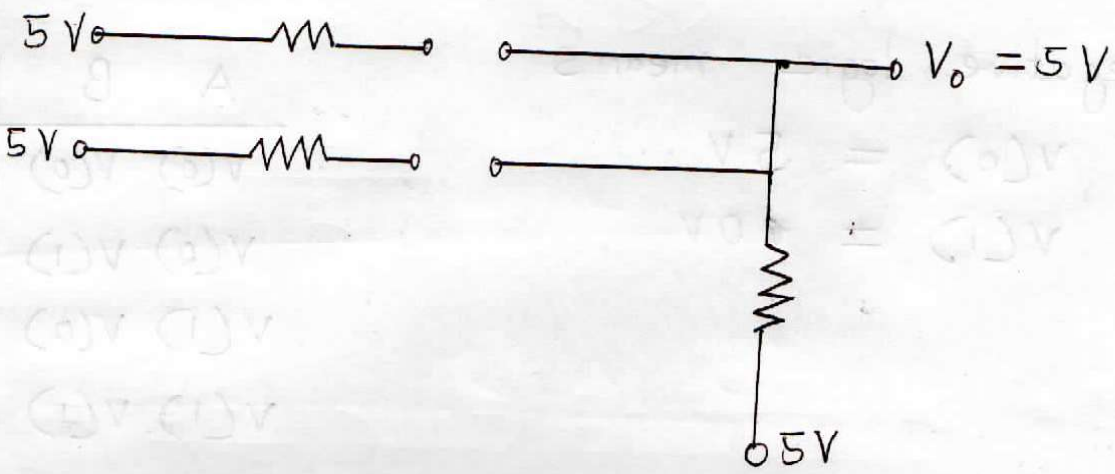


Case 1 :

$A = V(0) = 5V$

$B = V(0) = 5V$

Both D1 & D2 are in reverse bias.
So, the circuit will work like —



- no current flow
- no voltage drop ~~across~~ across R

$\therefore V_o = 5V = V(0)$

Case 2 :

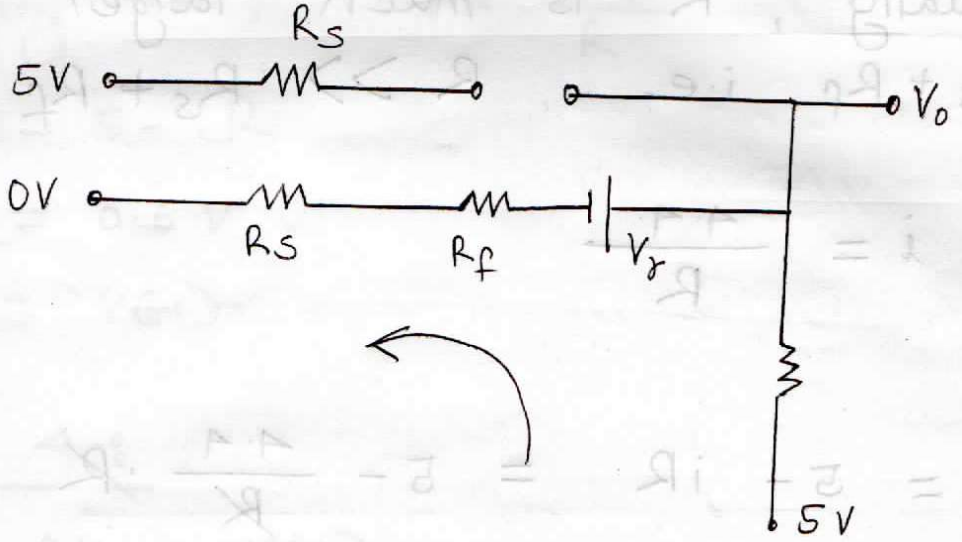
$A = V(0) = 5V$

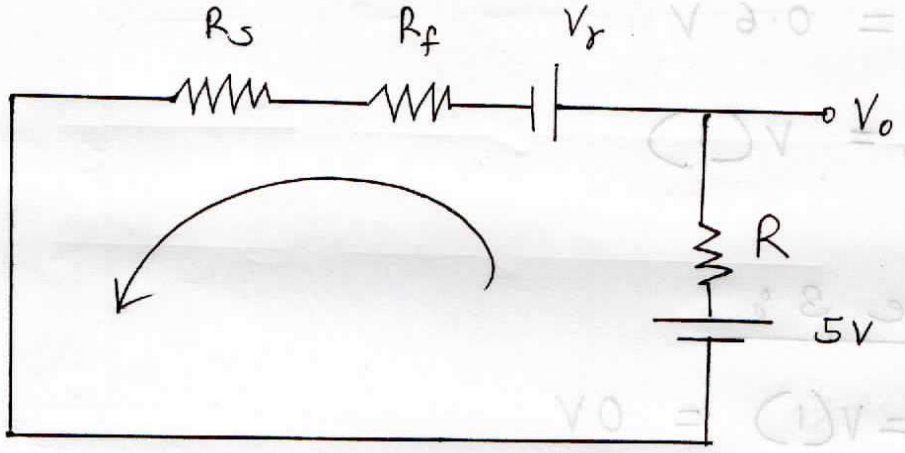
$B = V(1) = 0V$

Here, D_1 is in reverse bias

D_2 is in forward bias

According to piecewise linear model





Applying KVL,

$$-5 + iR + V_\gamma + iR_f + iR_s = 0$$

$$\Rightarrow \quad i = \frac{5 - V_\gamma}{R + R_f + R_s}$$

$$= \frac{5 - 0.6}{R + R_f + R_s} \quad [\text{Silicon diode}]$$

$$= \frac{4.4}{R + R_f + R_s}$$

Usually, R is much larger than $R_s + R_f$ i.e $R >> R_s + R_f$

$$\therefore i = \frac{4.4}{R}$$

So,

$$V_o = 5 - iR = 5 - \frac{4.4}{R} \cdot R = 5 - 4.4$$

$$= 0.6\ V$$

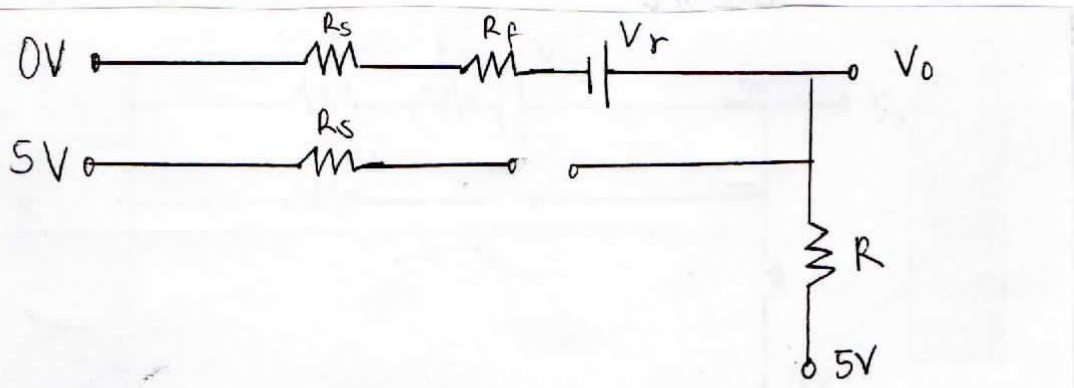
$\therefore V_o = V(1)$

Case 3 :

$A = V(1) = 0V$

$B = V(0) = 5V$

Here, D_1 is in forward bias & D_2 is in reverse bias

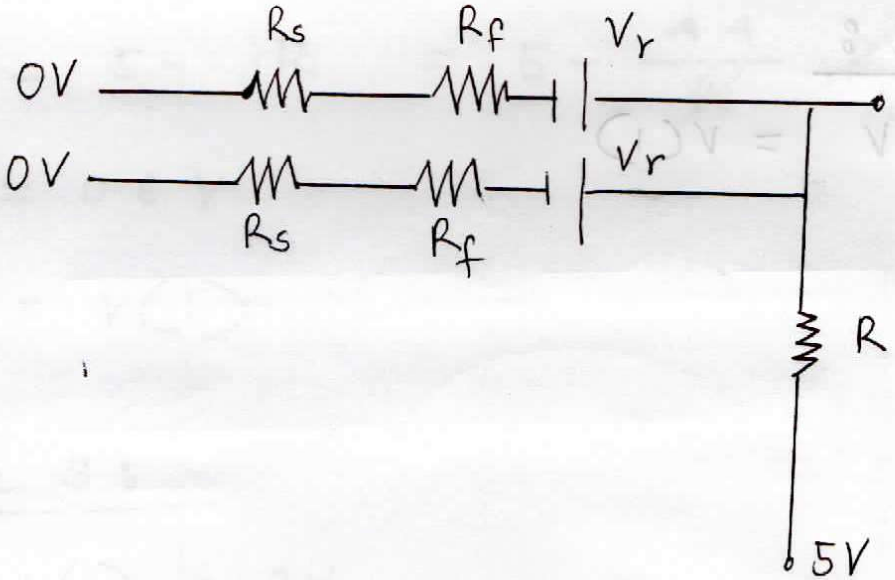


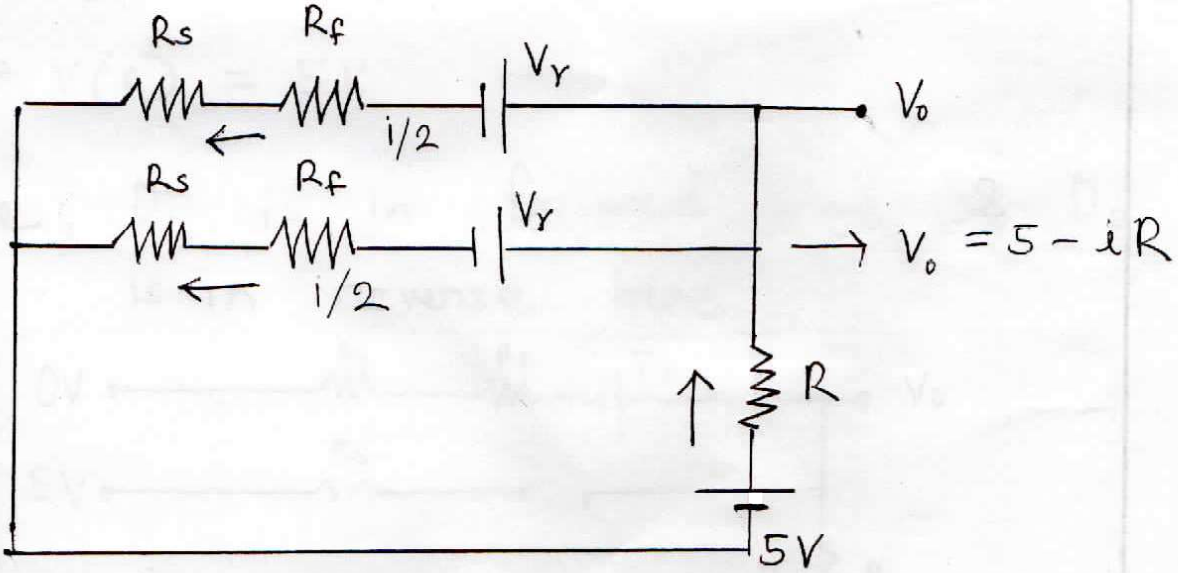
Case 4 :

A = V(1) = 0V

B = V(1) = 0V

Both D_1 & D_2 are in forward Bias.





Applying KVL,

$$-5 + iR + V_r + \frac{i}{2}R_f + \frac{i}{2}R_S = 0$$

$$\Rightarrow i\left(R + \frac{R_f}{2} + \frac{R_S}{2}\right) = 5 - V_r$$

$$\Rightarrow i = \frac{5 - V_r}{R + \frac{R_f}{2} + \frac{R_S}{2}}$$

$$= \frac{5 - 0.6}{R + \frac{1}{2}(R_f + R_S)}$$

Since, $R >> R_f + R_S$

$$\therefore i = \frac{4.4}{R}$$

So, $V_o = 0.6\ V = V(1)$

Ideal Parameters

$R = 2.2\ K\Omega$

$R_S = 50\ \Omega$

$R_f = 100\ \Omega$