Ahsanullah University of Science and Technology (AUST)

Department of Computer Science and Engineering

LAB REPORT

Course No. : CSE2210

Course Title: Digital Electronics and Pulse Techniques Lab

Experiment Number: 04

Name of the Experiment: Study of a RTL NOR Gate

Submitted By:

180204142 S. M Tasnimul Hasan

Name of the Experiment :

Study of an RTL NOR gate.

Objective :

The main objective of this experiment is to be familiar with NOR Gate using RTL techniques and measuring the output V_o for all possible combinations.

Circuit Diagram :

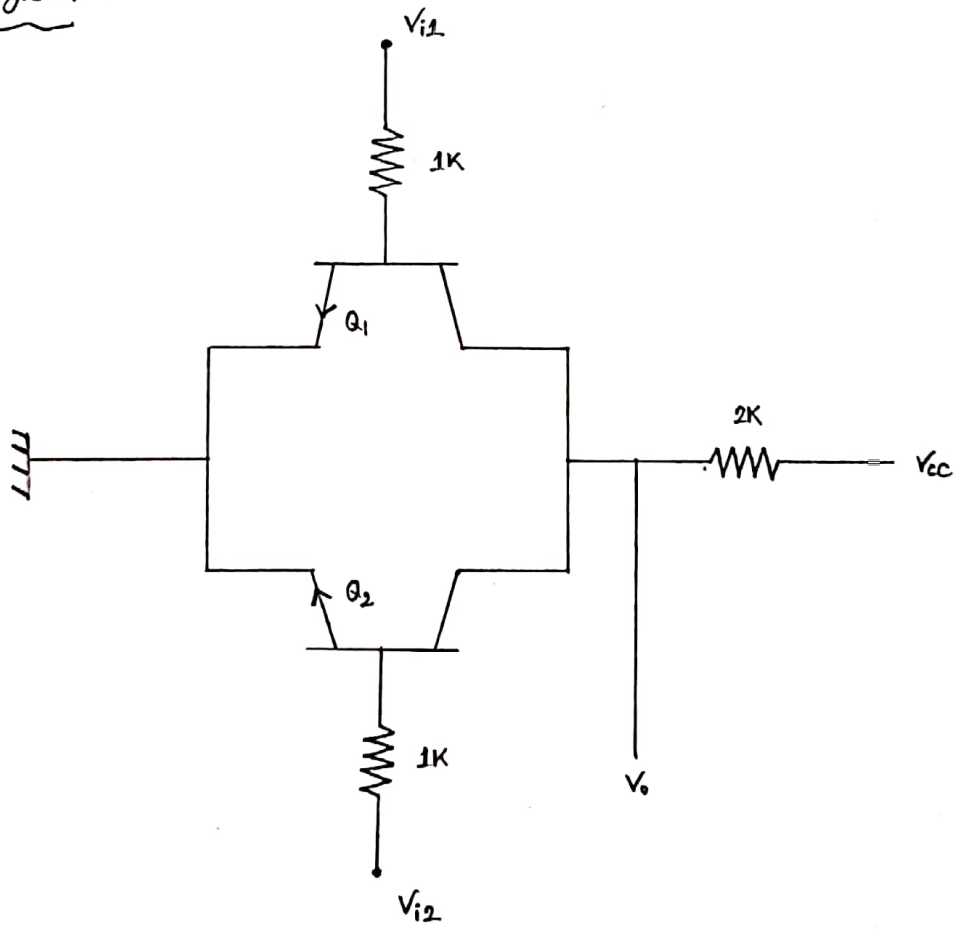

Fig : RTL NOR Gate

Answers to the Questions :

Question - 1 : Analyze the operation of RTL NOR gate with the experimental data.

Answer : Incase of NOR gate combinations we know that when the both input is 0, in that case the output result is 1. But for all other combinations the output result is 0. From the experimental data we see that, when both inputs are low, only then the output is high. For the rest of the input combinations the output is low.

Input		Output
V_{i1}	V_{i2}	V_o
0	0	5.00
0	1	0.02
1	0	0.02
1	1	0.02

Question - 02 : What is the importance of studying the RTL gate ?

Answer : The importance of studying RTL gate are :

① We can perform NOR operation with RTL gate. As NOR gate is an universal gate, any logic gate can be performed using this RTL gate.

② RTL gate is the first manufactured gate of the logic family. It is no longer used in new systems because it has low fan out. The output depends on the fan out. Though noise margins are small and the output swing is low but RTL gate leads to introduction to DCTL, which is used in MOS and cmos logic.

Question - 03 : Draw the V_o vs V_{i1} and V_{i2} curves.

Answer : Both graphs are attached below -

Experimental Data :

Data Table for Procedure - 1 :

V_{i1}	V_{i2}	V_o
0.00	0.00	5.00
0.00	1.00	0.02
1.00	0.00	0.02
1.00	1.00	0.02

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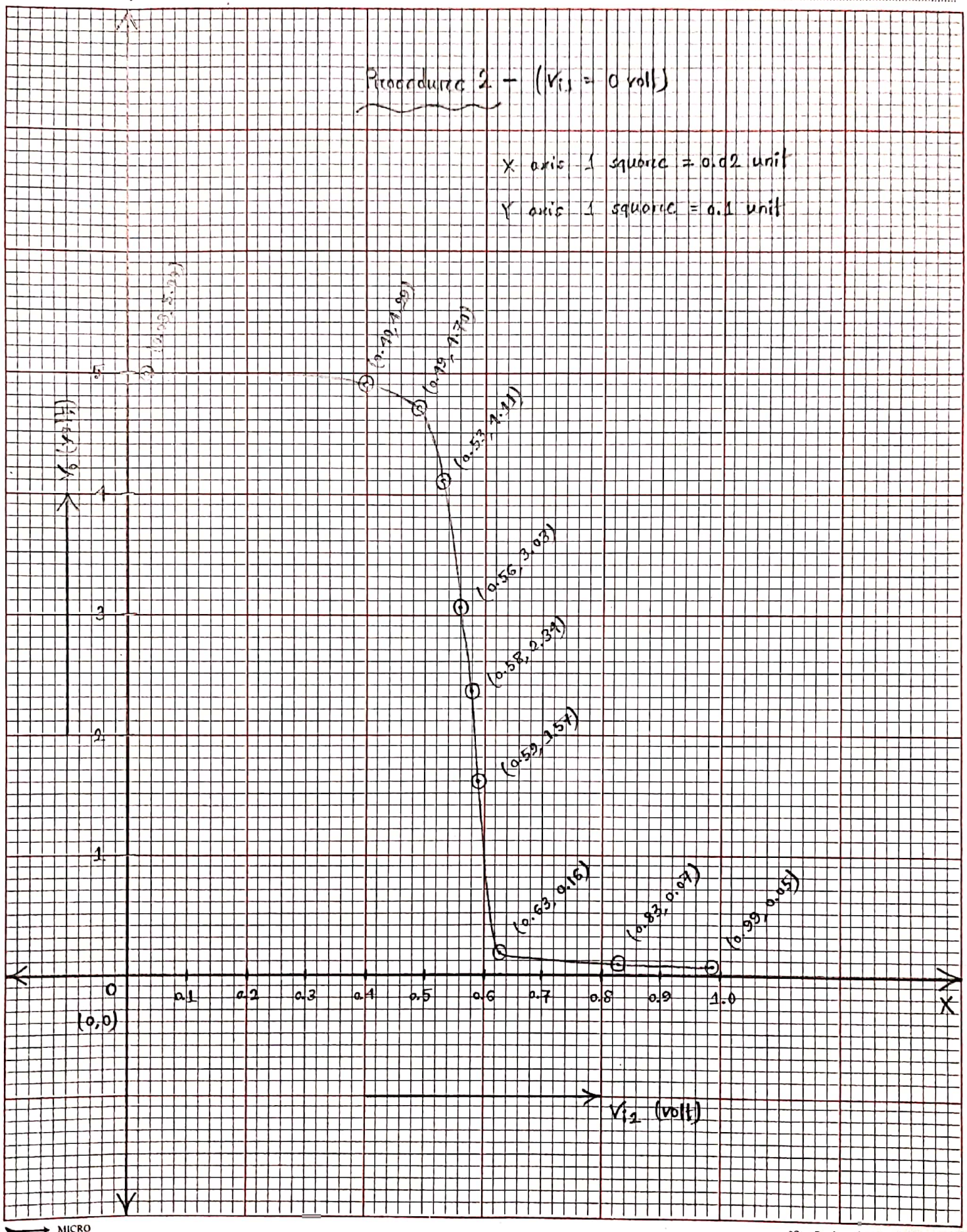

MICRO

Star Products 8 Inch × 10 Inch

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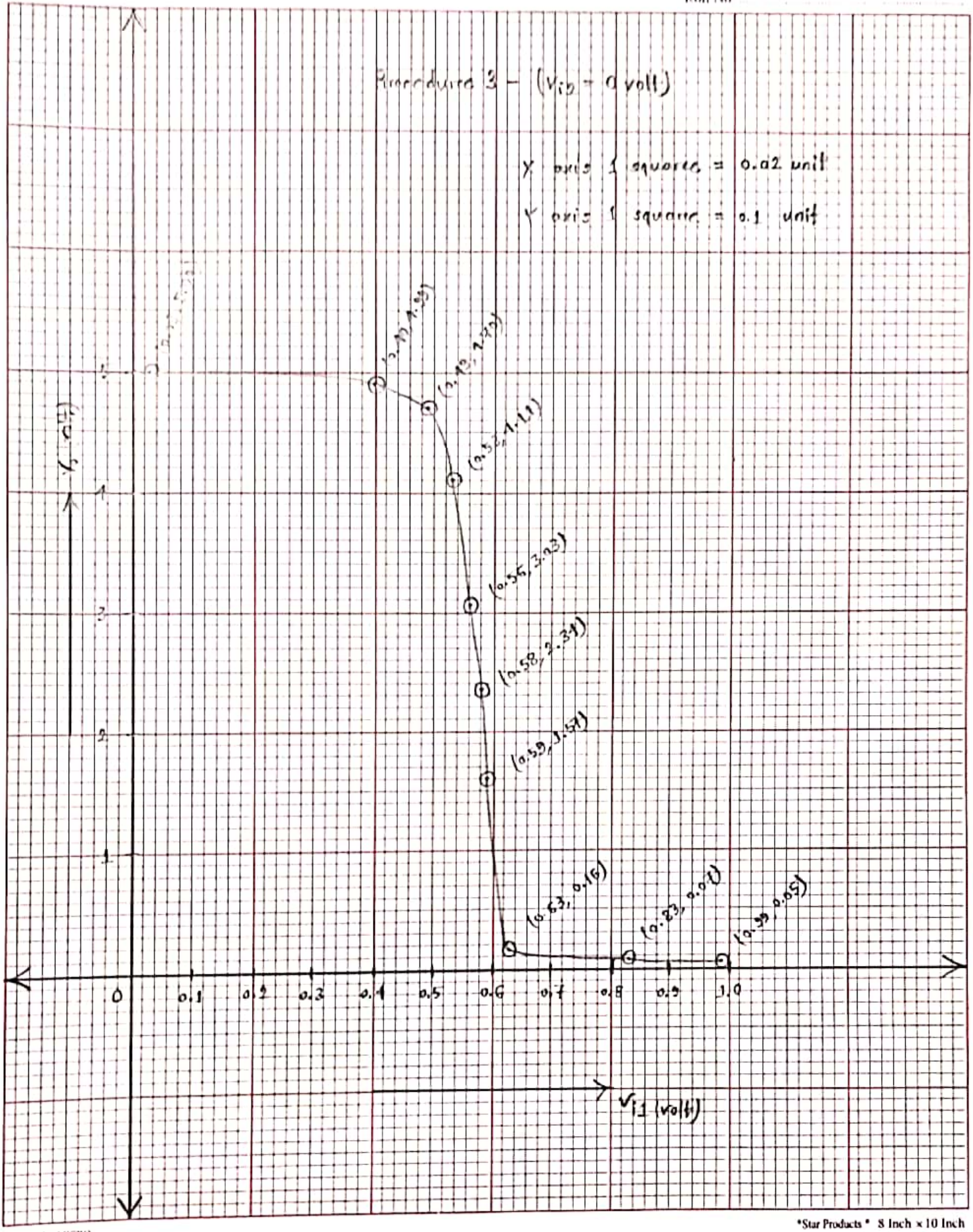
Procedure 3 – (V_{ib} = 0 volt)

X axis 1 squares = 0.02 unit

Y axis 1 square = 0.1 unit



Star Products 8 Inch × 10 Inch

MICRO

Data Table for Procedure - 2 :

V_{i1}	V_{i2}	V_o
0.00	0.03	5.00
0.00	0.40	4.99
0.00	0.49	4.70
0.00	0.53	4.11
0.00	0.56	3.03
0.00	0.58	2.34
0.00	0.59	1.57
0.00	0.63	0.16
0.00	0.83	0.07
0.00	0.99	0.05

Data Table for Procedure - 3 :

V_{i1}	V_{i2}	V_o
0.03	0.00	5.00
0.40	0.00	4.99
0.49	0.00	4.70
0.53	0.00	4.11
0.56	0.00	3.03
0.58	0.00	2.34
0.59	0.00	1.57
0.63	0.00	0.16
0.83	0.00	0.07
0.99	0.00	0.05

Discussion of the findings :

In this experiment, we have implemented NOR gate using RTL technique. When both the inputs were low, we got high voltage at the output voltage terminal. For all other combinations we got low voltage output. This is the characteristics of a NOR Gate. So, we can say we have designed a NOR Gate using RTL technique successfully and observed its characteristics.