Ahsanullah University of Science and Technology
Department of Computer Science and Engineering

Course Outline

Course No	:	CSE2213
Course Title	:	Computer Architecture
Credit Hour	:	3.0
Semester (Session)	:	Spring 2020
Student Year & Student Semester	:	2nd Year, 2nd Semester
Course Teacher(s)	:	Syeda Shabnam Hasan, Assistant Professor

Course Objective/Course Outcome (CO):

CO_1: To conceptualize the basics of organizational and architectural issues of a digital computer.
CO_2: To identify the elements of modern instructions sets and their impact on processor design.
CO_3: To analyze performance issues in processor and memory design of a digital computer.
CO_4: To understand various data transfer techniques in digital computer and analyze processor performance improvement using instruction level parallelism.

Text/ Reference books:

- "Computer Organization" By Carl Hamacher, Zvonko Vranesic, Safwat Zaky (5th edition), McGraw-Hill Education.
- "Computer Organization and Design: The Hardware/Software Interface'' By John L. Hennessy and David A. Patterson, (5th Edition), Morgan Kaufmann Publishers Inc.

Lecture Plan:

Week	Topics/Contents	Course Outcome
01	Basic Structure of Computers: Types of a computer, Basic functional units of a computer system, Basic operational concepts, Bus structures, Performance evaluation: Basic performance equation, Pipelining and superscalar operation, Quantitative measurement of performance; Instruction set architecture: CISC and RISC; Multiprocessor and multicomputer.	CO_1
02	Machine Instructions and Programs: Representation of numbers, characters and instructions, Signed integer operations and overflow detection, Addressing modes of instructions, Assembly language notations, Basic input/output operations, Instruction formats.	CO_2
03	Machine Instructions and Programs: Program sequencing and branching, Subroutines: Nesting, parameter passing and stack frame; Stack processor organization, Example programs and instructions, Encoding of machine instructions. Quiz#1	CO_2
04	Input/output Organization: Accessing I/O devices, Program controlled I/O, Interrupt based I/O: Handling multiple devices, Role of operating system, Processor examples; Direct memory access.	CO_1 , CO_2
05	Input/output Organization: Bus arbitration algorithms, Synchronous and Asynchronous Bus, Interface circuits: Serial and parallel ports for input, output and combined I/O operations, Standard I/O interfaces: PCI, SCSI and USB bus standards. Quiz#2	CO_1 ,CO_2, CO_3
06	The Memory System: Internal organization of semiconductor RAM memory, Static memory, Synchronous and Asynchronous DRAM, Read-only memories, Principles of locality, Memory hierarchy.	CO_1 , CO_3, CO_4
07	The Memory System: Cache memory: Direct mapped, set-associative and fully associative cache, Multi-level cache, Measuring and improving cache performance; Virtual memory.	CO_1 , CO_3, CO_4
08	CPU Arithmetic: Addition and subtraction of signed numbers Carry look-ahead fast adders, Multiplication, Fast multiplication, Booth's algorithm for signed operand multiplication, Integer division.	CO_1, ,CO_2, CO_4

Week	Topics	Course Outcome
09	CPU Arithmetic: Floating-point numbers: IEEE standard representation, Arithmetic operations, Guard bits and truncation. Quiz#3	CO_1, , CO_2, CO_4
10	Basic Processing Unit: Single bus CPU datapath architecture, Arithmetic and logical operations, Fetching and storing instructions from/to memory, Execution of a complete instruction, Branch instructions, Control sequence of common instructions.	CO_1 , CO_2
11	Basic Processing Unit: Multiple bus architecture, Hardwired control unit, Micro-programmed control: Microinstructions, Micro-program sequencing, Wide branch addressing; Example of a complete processor.	CO_1 , CO_2
12	Pipelining: Role of Cache memory, Pipeline performance, Hazards: Examples of data, instruction and structural hazards, Operand forwarding, Handling data hazard in software.	CO_1 , CO_3, CO_4
13	Pipelining: Conditional and unconditional branches, Delayed branching, Branch prediction, Data path and control considerations, Superscalar operation, Performance considerations. Quiz#4	CO_1,CO_3, CO_4
14	Review on previous lectures and problem solving.	

Note: *This Lecture Plan is subject to change. Course teacher will slow down or speed up each chapter to meet the needs of students*.

Marks Distribution:

Attendance and Class Performance	10
Class Test	20
Final Exam	70
Total	**100**

FOUR class tests will be taken (as it is a 3-credit course) and best THREE will be considered for "Class Test" marks.