CSE 3215: Microcontroller Based System Design

Quiz 1 (Set A1)

Time: 20 minutes

Marks: 10

No.	Question	Marks
1.	A microcontroller is basically a ……	[1]
2.	Why is pipelining easier in RISC processors whereas difficult in CISC processors?	[3]
3.	What is the split cache version of the Modified Harvard Architecture?	[4]
4.	A 1024K memory chip has 16 pins for data. Find: (a) the organization (b) the number of address pins for this memory chip.	[2]

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Quiz 1 (Set B1)

Time: 20 minutes

Marks: 10

No.	Question	Marks
1.	A microprocessor is basically a ……	[1]
2.	Why are Register banks used for Fast Context Switching?	[3]
3.	Analyze which one gives better performance between modified Harvard architecture and Harvard architecture.	[4]
4.	A 512K memory chip has 16 pins for data. Find: (a) the organization (b) the number of address pins for this memory chip.	[2]

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Quiz 1 (Set A2)

Time: 20 minutes

Marks: 10

No.	Question	Marks
1.	AVRs are all …….. , meaning that the CPU can work on only …….. of data at a time.	[1]
2.	What is embedded system and why does it use microcontroller most of the time?	[3]
3.	Explain the purpose and working procedure of a watchdog timer.	[4]
4.	Write down the difference between Flash Memory and EEPROM.	[2]

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Quiz 1 (Set B2)

Time: 20 minutes

Marks: 10

No.	Question	Marks
1.	The ARM architecture is a …….. developed by ARM Ltd.	[1]
2.	What is memory organization and memory capacity of a semiconductor memory chip?	[3]
3.	Distinguish between RISC and CISC.	[4]
4.	Why was Von-Neumann Architecture more popular than Harvard Architecture in the earlier days?	[2]