

-6  
Level: Bachelor  
Programme: BCA  
Course: Computer Architecture

Semester: Spring      Year : 2018  
Full Marks: 100      Pass Marks: 45  
Time : 3hrs.

*Candidates are required to give their answers in their own words as far as practicable.*

*The figures in the margin indicate full marks.*

*Attempt all the questions.*

1. a) Define computer organization and architecture. Explain the instruction set used in IAS computer. 7
- b) What is register organization? Describe dataflow interrupt cycle and execute cycle with diagram. 8
2. a) Multiply two numbers  $(3) \times (-2)$  using Booth's algorithm 8
- b) Explain in detail about hardwired and micro-programmed control unit with their applications. 7
3. a) What is control unit? Describe the function unit and control of the processor. 8
- b) What is cache memory? Explain direct, Associative and set Associative mapping in cache memory. 7
4. a) Write the differences between RAM and ROM. 7
- b) What is I/O module? Explain the major functions of an I/O module. 8
5. a) Assume that pipeline has  $K=6$  segment and executes  $n=150$  tasks in sequence. Let the time taken to process a sub-operation in each segment is 50 sec, calculate the speed up ratio in the pipeline. 7
- b) What is pipeline hazard? Describe branch hazard with different resolution technique. 8
6. a) What is parallel processing? How can we achieve parallelism in uniprocessor System? 8
- b) Explain Flynn's classification. Explain software and hardware solutions for cache coherence. 7
7. Write short notes on: (Any two) 2×5
  - a) Arithmetic and logical micro operation.
  - b) BCD Arithmetic unit
  - c) Power efficient processors

# POKHARA UNIVERSITY

BCA 5TH  
2075

Level: Bachelor

Semester: Fall

Year: 2018

Programme: BCA

Full Marks: 100

Course: Computer Architecture

Pass Marks: 45

Time: 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

- a) What is addressing mode? Describe different addressing modes used in computer. 8
- b) Explain the applications of Logic Micro Operations. Define HDL. 7
- a) What is instruction cycle? Explain dataflow fetch and interrupt cycle with diagram. 7
- b) Perform  $(7)_{10} * (-3)_{10}$  using Booth's Algorithm 8
- a) Explain the algorithm for Unsigned Multiplication. 7
- b) Explain control unit with controls, inputs and outputs with diagram. 8
- a) Differentiate between hardwired and micro-programmed control unit. 7
- b) Define RAID. Explain Memory hierarchy. Write the difference between magnetic disk and magnetic tape. 8
- a) What is mapping? How set associative mapping is different from associative mapping? 7
- b) Why DMA has priority over CPU when both request a memory transfer? A Programmed I/O Operation keeps the CPU busy needlessly. Explain. 8
- a) What are the conflicts that may arise in instructions pipelining? Explain with Solutions. 8
- b) What is cache coherence? Explain in detail about Flynn's classification. 7

Write short notes on any two:

2×5

- a) Structure and Functions of computer
- b) RISC vs. CISC
- c) Dual Core and Quad core Processors

# POKHARA UNIVERSITY

Level: Bachelor Semester – Fall Year : 2017  
Programme: BCA Full Marks: 100  
Course: Computer Architecture Pass Marks: 45

Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

Differentiate between Computer Architecture and Computer Organization. What are instructions set design issues of CPU? 8

Define the term micro-operation. Write down the sequence of microinstructions for fetch and interrupt cycle. 7

Explain in detail instruction cycle state diagram.

What is floating point arithmetic? Perform the following signed multiplication.  $(7)_{10} \times (-3)_{10}$ . 7

Differentiate between Hardwired Control Unit and Micro programmed Control unit. Explain Horizontal Microinstruction format. 8

Why are external devices not connected directly with bus computer system? Draw an internal structure of I/O module. 7

What are the cache memory design issues? Explain mapping of cache memory with its pros and cons. 7

How Interrupt Driven I/O is better than programmed I/O? Discuss DMA transfer with the help of block diagram. 8

Explain various types of interconnection structures in multiprocessor system. 8

What is Register Renaming? Explain the role of overlapped register window in RISC processor. 7

What are different hardware and software performance issues in multicore computer? 8

Assume that pipeline has K=4 segment and execute n= 70 task in sequence. Let the time taken to process a sub operation in each segment in 20sec. calculate the speed up ratio in the pipeline. write short notes on any two: 7

- a) Cache coherency
- b) Arithmetic pipelining
- c) VHDL

BCA ST'1  
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POKHARAUNIVERSITY

Level: Bachelor  
Programme: BCA  
Course: Computer Architecture

Semester – Spring

Year : 2017

Full Marks: 100

Pass Marks: 45

Time : 3hrs.

*Candidates are required to give their answers in their own words as far as practicable.*

*The figures in the margin indicate full marks.*

*Attempt all the questions.*

- |    |   |          |
|----|---|----------|
| a) | What is Computer Architecture? What are the instructions used in IAS computer. Explain in brief.  | 8        |
| b) | Define VHDL. Explain about shift micro operations in detail.  | 7        |
| 2. | a) Describe the basic ALU with its functional block diagram and operational truth table.<br>b) Draw Booth's multiplication algorithm and perform multiplication between -4 and -7.  | 7        |
| 3. | a) Differentiate between Hardwired Control Unit and Micro programmed Control unit.<br>b) Why replacement algorithm is used in set associative mapping? Explain.   | 8        |
| 4. | a) Explain how data transfer is performed in DMA with an example.<br>b) Explain the overlapping register windows in RISC.   | 7        |
| 5. | a) A non pipeline system takes 40ns to process a task. The same task can be processed in a six segment pipeline with clock cycle of 10ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speed that can be achieved?<br>b) Explain in detail about Flynn's classification. | 8        |
| 6. | a) What is virtual memory? Explain in brief about RAID.<br>b) Describe hardware performance issue in multi-core computer.   | 7        |
| 7. | Write short notes on any two:<br>a) Addressing modes<br>b) BCD Adder<br>c) Dual core processor  | 8<br>2×5 |

**POKHARA UNIVERSITY**

Level: Bachelor	Semester – Fall	Year : 2016	7.	Write short notes on any two:
Programme: BCA		Full Marks: 100	a)	Integer representation.
Course: Computer Architecture		Pass Marks: 45	b)	RAID.
		Time : 3 hrs.	c)	Cache Coherence.
<i>Candidates are required to give their answers in their own words as far as practicable.</i>				
<i>The figures in the margin indicate full marks.</i>				
<b>Attempt all the questions.</b>				
Define Computer Architecture and what are the instructions used in IAS computer? Explain each in detail.	8			
What is micro operation? Explain the logical and arithmetic micro operation with examples.	7			
What do you mean by instruction cycle? Explain about each state of instruction cycle.	8			
Compute $(7)_{10} \times (-3)_{10}$ where numbers are represented by 2's complement representation.	7			
Briefly explain the functioning of micro-programmed control unit with necessary block diagram.	7			
Define micro-instruction Sequencing Techniques. What are the micro-instruction formats used in Intel-Pentium explain each in detail?	8			
Explain the associative mapping technique in cache memory and compare it with set associative mapping.	7			
Why interrupt driven I/O is better than programmed I/O and explain how DMA overcomes the drawback of both?	8			
Describe instruction pipelining. Assume that the pipeline has K=9 segment and execute 100 task in a sequence. Let the time taken to process a sub operation in each segment is 12 secs. Calculate the speed up ratio in the pipelining.	7			
Define Flynn's Taxonomy? Draw different interconnection structure of multiprocessor system and describe it with necessary diagram.	8			
What are the RISC instruction? Explain the various pipelining Hazards in instruction pipelining and its solution.	8			
Explain the software performance issues of multi core computer.				

what is dual and quad core multi-processor?

POKHARA UNIVERSITY

Year : 2016  
Full Marks: 100  
Pass Marks: 45  
Time : 3hrs

*Candidates are required to give their answers in their own words as far as practicable.*

*The figures in the margin indicate full marks  
Attempt all the questions*

- | POKHARA UNIVERSITY |  | Year : 2016     | Time : 3 hrs.                   |
|--------------------|--|-----------------|---------------------------------|
| Level: Bachelor    | Semester – Spring  | Full Marks: 100 | Pass Marks: 45                  |
| Programme: BCA     | Course: Computer Architecture  |                 |                                 |
| 1.                 | a) Define Computer Architecture and what are the instruction used in IAS computer? Explain each in detail.   | 8               | a) Booth's Algorithm.           |
| 2.                 | b) Define Instruction Cycle. Explain the basic components used in processor organization.  | 7               | b) Shift Operation.             |
| 3.                 | a) Compute $(7)_{10} \times (-3)_{10}$ where numbers are represented by 2's complement representation  | 8               | c) Addressing modes.            |
| 4.                 | b) Briefly explain the functioning of micro-programmed control unit with necessary block diagram.  | 7               | 7. Write short notes on any two |
| 5.                 | a) Define micro-instruction Sequencing Techniques. What are the micro-instruction formats used in Intel-Pentium? Explain each in detail.   | 8               |                                 |
| b)                 | Define write through back. Briefly explain the full associative mapping technique.   | 7               |                                 |
| 6.                 | a) Define cache ratio. Describe cache read operation with flowchart,   | 7               |                                 |
| b)                 | What are the limitations of programmed I/O? How these are improved in interrupt driven I/O? And how the limitations of Interrupt driven I/O are improved by DMA? Also draw the DMA Cycle.        | 8               |                                 |
| 7.                 | a) What are the CISC instructions? Explain the various pipelining Hazards in instruction pipelining and its solution.  | 8               |                                 |
| b)                 | Define Enslow's Taxonomy. Draw different interconnection structure of multiprocessor system and describe it with necessary diagram   | 7               |                                 |
| 8.                 | a) Assume that pipeline has K=8 segment and execute n=120 tasks in sequence. Let the time taken to process a sub-operation in each segment is 20s, calculate the speed up ratio in the pipeline. | 8               |                                 |
| b)                 | Explain the Dual Core and Power Efficient Processors   | 8               |                                 |

# POKHARA UNIVERSITY

2x5

Level: Bachelor

Semester – Fall

Year : 2015

Programme: BCA

Full Marks: 100

Course: Computer Architecture (New)

Pass Marks: 45

Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

Figures in the margin indicate full marks.

Answer all the questions.

- |  |
|--|
| a) Explain direct, indirect and displacement addressing mode with advantages and disadvantages. 8  |
| b) Define RTL. Explain all micro operations with RTL code. 7   |
| i) Describe Register Organization and datapath in computer. 7  |
| ii) Multiply two numbers $(-3)_{10} \times (5)_{10}$ using Booth's multiplication algorithm. 8   |
| i) Briefly explain the functioning of micro-programmed control unit with necessary block diagram. 7  |
| ii) Define micro-instruction sequencing technique. What are the micro-instruction sequencing technique used in Intel Pentium and explain in detail? 8  |
| i) Explain how set associate mapping exhibits the strength of both direct and associate mapping. 7   |
| ii) Define RAID. Explain different level of RAID with their features. 8  |
| i) What are the limitations of programmed I/O, how these are improved in interrupt driven I/O, and how the limitation of interrupt driven I/O are improved by DMA. 8                                 |
| ) Describe the architecture of register overlapped window. 7   |
| ) Assume that pipeline has K=8 segment and execute n=140 tasks in sequence. Let the time taken to process a sub-operation in each segment is 20 sec. Calculate the speed up ratio in the pipeline. 8 |
| ) What are hardware and software performance issues of multicore computers? Explain. 7   |

Write short notes on any two:

- i) Floating point representation
- ii) Instruction Pipeline c) Cache Coherence

2x5

# POKHARA UNIVERSITY

Level: Bachelor

Semester – Spring

Year : 2015

Programme: BCA

Full Marks : 100

Pass Mark : 45

Time : 3 Hrs

Course: Computer Architecture

*Candidates are required to give their answers in their own words as far as practicable.*

*The figures in the margin indicate full marks.*

*Attempt all the questions.*

- |    |   |     |
|----|---|-----|
| 1. | a) Define Computer Architecture and what are the instruction used in IAS computer explain each in detail.   | 8   |
| 2. | b) Describe Register organization and data path in computer.  | 7   |
| 3. | a) Multiply two number $(-2) \times (4)$ using Booth's multiplication algorithm.  | 8   |
| 2. | b) Briefly explain the functioning of micro-programmed control unit with necessary block diagram.   | 7   |
| 3. | a) What is RAID? Explain various levels of RAID.  | 7   |
| 3. | b) Define cache miss. Describe cache read operation with flowchart.   | 8   |
| 4. | a) What are the limitations of programmed I/O, how these are improved in interrupt driven I/O, and how the limitations of interrupt driven I/O are improved by DMA also draw the DMA Cycle.           | 8   |
| 4. | b) What is hazard? Describe the methods to resolve the problem of branch hazard in designning a pipelined architecture.   | 7   |
| 5. | a) Assume that pipeline has $K=4$ segment and execute $n=70$ task in sequence. Let the time taken to process a sub-operation in each segment is 20 sec. Calculate the speed up ratio in the pipeline. | 8   |
| 5. | b) Explain the Single Core Dual and Quad Core Processors.   | 7   |
| 6. | a) Explain Flyns classification of parallel computer.   | 7   |
| 6. | b) Differentiate between RISC and CISC computer architecture.   | 8   |
| 7. | Write short notes on any two:   | 2x5 |
|    | a) Shift micro operations.  |     |
|    | b) Addressing modes   |     |
|    | c) Register window  |     |

**POKHARA UNIVERSITY**

Level: Bachelor  
Programme:BCA  
Course:Computer Architecture (New)

Semester –Spring  
Year : 2014  
Full Marks: 100  
Pass Marks: 45  
Time : 3 hrs.

*Candidates are required to give their answers in their own words as far as practicable.*

*The figures in the margin indicate full marks.*

*Attempt all the questions.*

7. Write short notes on any two:

a) Arithmetic and logical micro-operation.

b) BCD arithmetic

c) Dual core and Quad core processors

a) Write about different types of addressing modes supported by computer architecture. 8

b) What is data path? Explain design principles for modern system. 7

a) Explain the Booth's algorithm for multiplication of signed numbers. Find the result of  $(-7)_{10} \times (3)_{10}$  using the same algorithm. 8

b) Explain hardwired and micro-programmed control unit with their uses. 7

a) Describe the basic functional elements of processor. 8

b) What is memory hierarchy? Briefly describe the concept of R.A.D. 7

a) Why cache memory is required? Differentiate between direct and associative mapping scheme for cache memory. 8

b) Describe programmed I/O and Interrupt DrivenI/O. 7

a) What do you mean by register windows? Discuss how does it help to improve of performance of procedure calling? Differentiate between RISC and CISC architecture. 7

b) What do you mean by multiprocessors system? Write about Flynn's classification of computers. 8

a) What is Cache Coherence? Explain hardware and software for Cache Coherence. 7

b) Write about any three approaches for dealing with conditional branches in instruction pipelining. 8

# POKHARA UNIVERSITY

Level: Bachelor  
 Programme: BCA  
 Course: Computer Architecture

Semester – Fall

Year : 2014  
 Full Marks: 100  
 Pass Marks: 45  
 Time : 3hrs.

*Candidates are required to give their answers in their own words as far as practicable.*

*The figures in the margin indicate full marks.*

*Attempt all the questions.*

- |   |     |
|---|-----|
| What is addressing mode? Explain various addressing modes.  | 8   |
| Define Instruction Cycle? Explain the basic component used in processor organization.   | 7   |
| Perform $x \times y$ , where $x=(-7)_{10}$ and $y=(5)_{10}$ . Consider a 4 bit registers and $x$ and $y$ is represented in 2's complement representation.   | 8   |
| Briefly explain the functioning of micro-programmed control unit with necessary block diagram.  | 7   |
| Differentiate between direct and associative mapping for cache memory.  | 7   |
| Define cache hit ratio. Describe cache Read operation with a flowchart.   | 8   |
| What are the limitations of programmed I/O, how these can improve in interrupt driven I/O, and how the limitations of interrupt driven I/O are improved by DMA.                                       | 8   |
| Differentiate between RISC and CISC.  | 7   |
| What are types of problem occurring in implementing the pipelining? How branches in piping are handled?   | 7   |
| Assume that pipeline has $K=8$ segment and executes $n=120$ tasks in sequence. Let the time taken to process a sub-operation in each segment is 40 sec. Calculate the speed up ratio in the pipeline. | 8   |
| Describe Flynn's classification with all types.   | 7   |
| Explain the Dual Core and Quad Core Processors.   | 8   |
| Write short notes on any two:   |     |
| a) Shift micro operations   | 2×5 |
| b) BCD Adder  |     |
| c) Micro-instruction in fetch cycle   |     |

# POKHARA UNIVERSITY

Level: Bachelor

Semester – Spring

Year : 2014

Programme: BCA

Full Marks: 100

Course: Computer Architecture (New)

Pass Marks: 45

Time : 3hrs.

*Candidates are required to give their answers in their own words as far as practicable.*

*The figures in the margin indicate full marks.*

*Attempt all the questions.*

2. a) Write about different types of addressing modes supported by computer architecture. 8
- b) What is data path? Explain design principles for modern system. 7
2. a) Explain the Booth's algorithm for multiplication of signed numbers. 8  
    Find the result of  $(-7)_{10} \times (3)_{10}$  using the same algorithm.
- b) Explain hardwired and micro-programmed control unit with their uses. 7
3. a) Describe the basic functional elements of processor. 8  
    b) What is memory hierarchy? Briefly describe the concept of RAID. 7
4. a) Why cache memory is required? Differentiate between direct and associative mapping scheme for cache memory. 8  
    b) Describe programmed I/O and Interrupt Driven I/O. 7
5. a) What do you mean by register windows? Discuss how does it help to improve of performance of procedure calling? Differentiate between RISC and CISC architecture. 7  
    b) What do you mean by multiprocessors system? Write about Flynn's classification of computers. 8
6. a) What is Cache Coherence? Explain hardware and software for Cache Coherence. 7  
    b) Write about any three approaches for dealing with conditional branches in instruction pipelining. 8
7. Write short notes on any two: 2×5
  - a) Arithmetic and logical micro-operation.
  - b) BCD arithmetic
  - c) Dual core and Quad core processors

## POKHARA UNIVERSITY

*Candidates are required to give their answers in their own words as far as practicable.*

*The figures in the margin indicate full marks.*

**Attempt all the questions.**

- |    |  |              |
|----|--|--------------|
| 1. | a) What is addressing mode? Explain various addressing modes.  | 8            |
|    | b) Define Instruction Cycle? Explain the basic component used in processor organization.   | 7            |
| 2. | a) Perform $x \times y$ , where $x=(-7)_{10}$ and $y=(5)_{10}$ . Consider a 4 bit registers and $x$ and $y$ is represented in 2's complement representation.   | 8            |
|    | b) Briefly explain the functioning of micro-programmed control unit with necessary block diagram.  | 7            |
| 3. | a) Differentiate between direct and associative mapping for cache memory.  | 7            |
|    | b) Define cache hit ratio. Describe cache Read operation with a flowchart.   | 8            |
| 4. | a) What are the limitations of programmed I/O, how these can improve in interrupt driven I/O, and how the limitations of interrupt driven I/O are improved by DMA.                                       | 8            |
|    | b) Differentiate between RISC and CISC.  | 7            |
| 5. | a) What are types of problem occurring in implementing the pipelining? How branches in pipelining are handled?   | 7            |
|    | b) Assume that pipeline has $K=8$ segment and executes $n=120$ tasks in sequence. Let the time taken to process a sub-operation in each segment is 40 sec. Calculate the speed up ratio in the pipeline. | 8            |
| 6. | a) Describe Flynn's classification with all types.   | 7            |
|    | b) Explain the Dual Core and Quad Core Processors.   | 8            |
| 7. | Write short notes on any two:  | $2 \times 5$ |
|    | a) Shift micro operations  |              |
|    | b) BCD Adder   |              |
|    | c) Micro- instruction in fetch cycle   |              |

# POKHARA UNIVERSITY

Level: Bachelor

Programme: BCA

Course: Computer Architecture

Semester – Spring

Year : 2013

Full Marks: 100

Pass Marks: 45

Time : 3hrs.

*Candidates are required to give their answers in their own words as far as practicable.*

*The figures in the margin indicate full marks.*

*Attempt all the questions.*

- |    |   |    |
|----|---|----|
| 1. | a) Differentiate between computer architecture and organization.                                    | 7  |
|    | b) Compile the following C statement:<br>$A[12]=h+A$ .  | 8  |
| 2. | a) Explain any one algorithm used for division with the block diagram for hardware.                 | 8  |
|    | b) What is virtual memory? Discuss about direct mapping for cache memory.                           | 7  |
| 3. | a) Explain the simple datapath for R-type instructions.   | 10 |
|    | b) Why a single cycle implementation is not used? Explain.  | 5  |
| 4. | a) What are hazards? What are their types? Explain about control hazards.                           | 10 |
|    | b) Differentiate between SIMD and MIMD computers.   | 5  |
| 5. | a) What is bus? Discuss the different types of bus arbitration schemes.                             | 8  |
|    | b) What are the four registers that are used to control the terminal devices? Explain each of them. | 7  |

**OR**

- |    |  |     |
|----|--|-----|
| 6. | a) Discuss about assembler and linker with their use and working.  | 7   |
|    | b) Discuss the main characteristics of CISC and RISC. Explain why it is easy to design compiler in CISC? | 7   |
| 7. | b) Design a 3 bit binary counter using JK flip-flops.  | 8   |
|    | c) Write short notes on any two:   | 2×5 |
|    | a) Procedure calls   |     |
|    | b) Finite State Machine  |     |
|    | c) Register window   |     |

POKHARA UNIVERSITY

Level: Bachelor

Semester – Fall

Year : 2013

Programme: BCA

Full Marks: 100

Course: Computer Architecture

Pass Marks: 45

Time : 3hrs.

*Candidates are required to give their answers in their own words as far as practicable.*

*The figures in the margin indicate full marks.*

*Attempt all the questions.*

1. a) Explain an algorithm for multiplication of signed numbers. Find the result of  $(-4)_{10} \times (-5)_{10}$  using same algorithm. 8
- b) Write about different addressing modes supported by MIPS architecture. 7
2. a) Define the term data path and control. Draw data path for R-type instruction. 7
- b) Define structural and control hazard. Discuss any two methods to resolve the problem of control hazards. 8
3. a) What is parallel processing? How you can use instruction pipelining? Explain with example. 7
- b) What is a cycle stealing mode of DMA? Draw the block diagram of DMA controller. 8
4. a) Explain direct-mapping and associative mapping with suitable figure. 7
- b) Discuss the working of terminal devices (input and output devices) in MIPS. 8
5. a) Design a 3-bit binary counter using JK flip-flops. 8
- b) Explain the terms gates, truth table, combinational logic and finite state machine. 7
6. a) What do you mean by register windows? Discuss how does it help to improve of performance of procedure calling? 8
- b) Discuss how pipelining can be achieved in RISC architecture giving example. 7
7. Write short notes on any two: 2×5
  - a) Hardwired versus micro-programmed control
  - b) Combinatorial Logic
  - c) Uses of ICs in the Development of modern Computers.