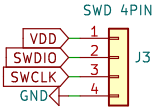
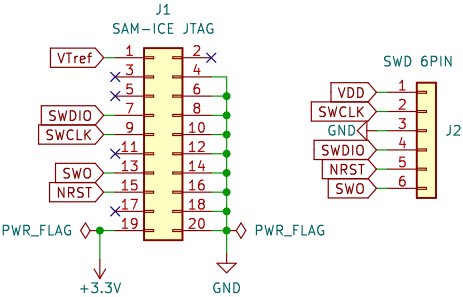
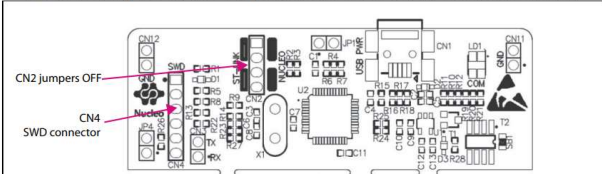


VTref	1	●	●	2	NC
Not used	3	●	●	4	GND
Not used	5	●	●	6	GND
SWDIO	7	●	●	8	GND
SWCLK	9	●	●	10	GND
Not used	11	●	●	12	GND
SWO	13	●	●	14	GND*
RESET	15	●	●	16	GND*
Not used	17	●	●	18	GND*
5V-Supply	19	●	●	20	GND*

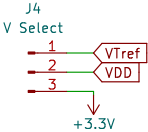
Table 4. JTAG/SWD cable connections on STLINK-V2				
Pin no.	ST-LINK/V2 connector (CN3)	ST-LINK/V2 function	Target connection (JTAG)	Target connection (SWD)
1	VAPP	Target VCC	MCU VDD ⁽¹⁾	MCU VDD ⁽¹⁾
2	TRST	JTAG TRST	NJTRST	GND ⁽²⁾
3	GND	GND	GND ⁽³⁾	GND ⁽³⁾
4	GND	GND	GND ⁽³⁾	GND ⁽³⁾
5	TDI	JTAG TDO	JTDI	GND ⁽²⁾
6	GND	GND	GND ⁽³⁾	GND ⁽³⁾
7	TMS_SWDIO	JTAG TMS, SW IO	JTMS	SWDIO
8	GND	GND	GND ⁽³⁾	GND ⁽³⁾
9	TCK_SWCLK	JTAG TCK, SW CLK	JTCK	SWCLK
10	GND	GND	GND ⁽³⁾	GND ⁽³⁾
11	Not connected	Not connected	Not connected	Not connected
12	GND	GND	GND ⁽³⁾	GND ⁽³⁾
13	TDO_SWO	JTAG TDI, SWO	JTDO	TRACESWO ⁽⁴⁾
14	GND	GND	GND ⁽³⁾	GND ⁽³⁾
15	NRST	NRST	NRST	NRST
16	GND	GND	GND ⁽³⁾	GND ⁽³⁾
17	Not connected	Not connected	Not connected	Not connected
18	GND	GND	GND ⁽³⁾	GND ⁽³⁾
19	VDD	VDD (3.3 V)	Not connected	Not connected
20	GND	GND	GND ⁽³⁾	GND ⁽³⁾

Table 5. Debug connector CN4 (SWD)		
Pin	CN4	Designation
1	VDD_TARGET	VDD from application
2	SWCLK	SWD clock
3	GND	ground
4	SWDIO	SWD data input/output
5	NRST	RESET of target STM32
6	SWO	Reserved

Figure 9. Using ST-LINK/V2-1 to program the STM32 on an external application



Note.
For a genuine ST-Link V2, connect the VTarget (VTr) pin to the target's VDD, while for a clone, connect the 3.3V pin to the target's VDD



Samiul

Sheet: /
File: JTAG_to_SWD.kicad_sch

Title: JTAG to SWD

Size: A4 Date: 2023-10-16

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