Advanced Analog Integrated-Circuit Design and Analysis

Midterm Project – Amplifier Design

1. Summary

We are assigned to design a low-power low-supply fully differential operational amplifier, which ALL the specifications listed in Table 1-1 are required to be fulfilled. Our final amplifier designed meets all the requirements. The comparison between the hand calculation and the simulation are summarized in the below table. In this project, TSMC 0.18μm process technology is selected.

Parameters	Specifications	Hand calculation	Simulation
Supply Voltage	± 1.0 V	± 1.0 V	± 1.0 V
Power Consumption	<= 2.0 mW	1.22mW	0.945mW
Low-frequency Gain A_0	>= 80 dB	88.2dB	88dB
Unity-Gain Frequency f_0	>= 250 MHz	297MHz	314MHz
Slew Rate SR	> 80 V/μs	110V/ μs	positive: 110V/μs negative: 132V/μs
Phase Margin PM	>= 60°	61.8°	61
CMRR	>= 80 dB	∞	189.52dB
PSRR	>= 80 dB at dc	∞	260dB
	>= 60 dB at 1 MHz	∞	146.1dB
DC Output	0V ± 50 mV	0V	-0.197mV
Differential Output Swing	> ± 1.2 V	± 1.4V	± 1.5 V
Total Harmonic Distortion (vid = 75% FS)	<= -30dBc	-	-45.304dBc
Input Offset Voltage	<- 100 mV	65mV	5.64fV (systematic offset) -4.83mV (random offset)
Equivalent Input Noise	< 1 mV rms (integrated over 1MHz BW)	2.47μV rms	7.7474μV_{rms} (w/o mismatch) 9.4867μV_{rms} (w/ mismatch)
(Single-Ended) Load Capacitor C_L	1 pF	1 pF	1 pF

Table 1 Design Summary

2. Introduction

Among the parameters listed, the low-frequency gain, unity gain frequency (UGF) and differential output swing are the most difficult to achieve in this amplifier design project. For 80dB gain, multi-stage circuit as to be used but UGF would be degraded. We choose to employ a folded cascode amplifier with gain boosting and common mode feedback as our circuit to achieve higher gain. Also to achieve output swing larger than 1.2V, using folded cascode structure helps to increase both the output swing and the gain. Auxiliary amplifiers are employed to achieve gain boosting. A pair of linear MOSFETs are used to achieve the common-mode feedback regulation. Figure 2-1 shows the proposed circuit.

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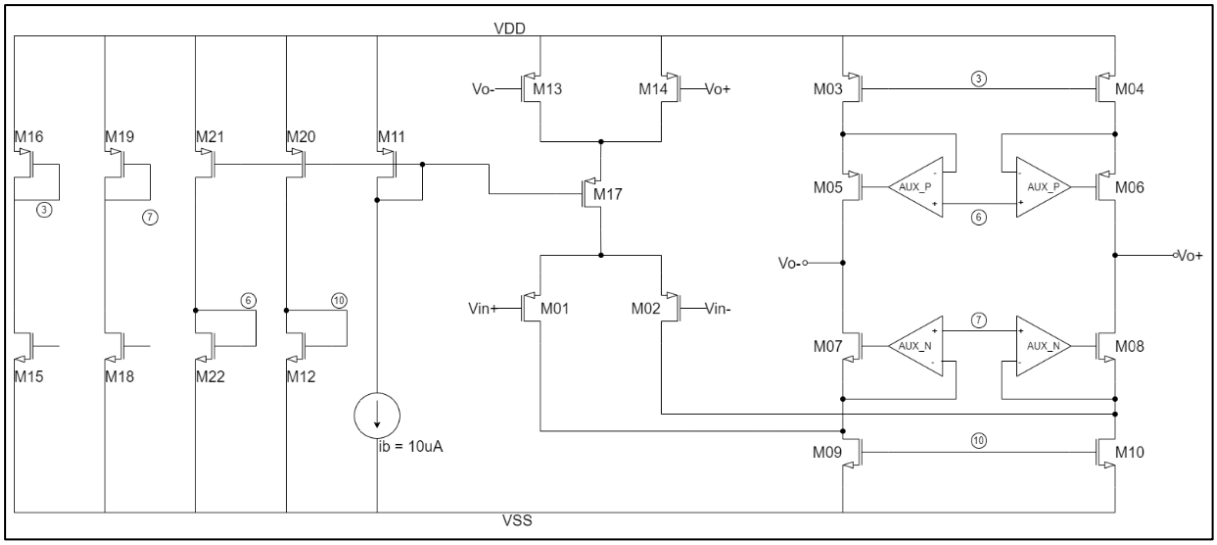

Figure 2-1 Schematics of designed amplifier

Common mode feedback (CMFB) circuit is constructed by 2 linear MOSFET devices, M13 and M14, with biasing controlled by M17. To maximize output swing, DC output voltage of 0V needs to be achieved stably. The voltage feedback loop can be achieved when v_o increases. The current flow through M13 and M14 decrease as V_{gs} of M13 and M14 decrease, then the current flow through M17 decreases thus v_o decreases. Such loop ensures a stable DC output is provided.

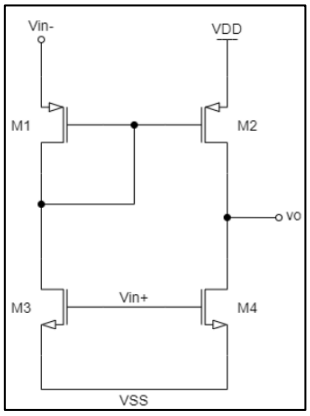

Figure 2-2 AUX_P (NMOS as input stage)

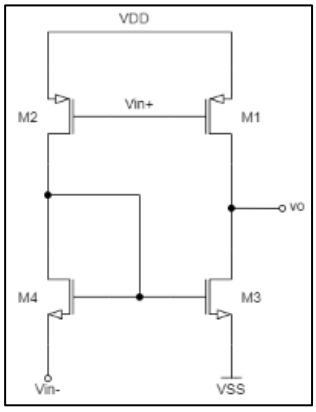

Figure 2-3 AUX_N (PMOS as input stage)

Regulated cascode with level shifting structure is adopted by adding 4 auxiliary amplifiers to the folded cascode branch, 2 AUX_P and 2 AUX_N. Using AUX_N as an example, the aspect ratio of M3 needs to be 1/4 of M4, so the overdrive voltage of M3 can be increased to 0.4V. This way Vgs of M3 can be increased to 0.9V and vin- can be reduced to 0.2V.

3. DC Hand Calculation

I. Calculations

Assumptions:

1. $Vov = Vgs - Vt = 0.2V$
2. $\mu_n c_{ox} = 247\mu A/V,\ \mu_p c_{ox} = 92\mu A/V$
3. $V_{tn} = 0.45V,\ V_{tp} = -0.45V$
4. $\lambda_n = 0.18,\ \lambda_p = 0.13$

A. Slew Rate:

$SR \geqslant 80V/us$

$\frac{2I_1}{Cout} \geqslant 80V/us$

We set $C_{Para} = 1pF$ *for a larger margin,*

$\therefore Cout = C_L + C_{Para} = 1p + 1p = 2pF$

$\therefore I_1 \geqslant 80uA$

We choose $I_1 = 110\mu A$

$\therefore SR = 110V/\mu s$

B. Power Consumption:

$P_{total} \leqslant 2mW$

$I_{total} \leqslant 1mA$

$I_{main} + I_{aux} + I_{bias} \leqslant 1mA$

$I_{main} = I_{M09} + I_{M10} = 440\mu A$

$I_{aux} = 4 * 30\mu A = 120\mu A$

$I_{bias} = 5 * 10\mu A = 50\mu A$

$I_{total} = 610uA$

$\therefore P_{total} = 1.22mW$

C. Output Swing:

We set $V_{dsat} = 0.15V$

Output Swing $= 2 - 4V_{dsat} = 2 - 4*0.15 = \pm 1.4V$

D. DC Output:

To ensure v_{o+} *and* v_{o-} *become* $0V$, $M13$ & $M14$ *have to operate in triode region.*

Therefore, we set $V_{gs13,14} = 1V$ & $V_{ds13,14} \approx 0.01V$.

$I_{M17} = 2I_1 = 220\mu A$

$\frac{1}{2}\mu_p c_{ox}\left(\frac{W}{L}\right)_{13,14}\left[(V_{gs13,14} - V_t)V_{ds} - \frac{1}{2}{V_{ds}}^2\right] = 220\mu A$

$\therefore \left(\frac{W}{L}\right)_{13,14} = 45.5$

E. Input Offset Voltage:

For the worst case mismatch,

$$V_{os} = \Delta V_{tn} + \Delta V_{tp}\frac{g_{mp}}{g_{mn}} - \frac{(V_{ov})_n}{2}\left(\frac{\Delta\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)} + \frac{\Delta\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)}\right)$$

$$= 50mV + 50mV \times \frac{1}{2} - \frac{0.2}{2} * 10\%$$

$$= 65mV$$

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II. Simulation results

A. Slew Rate: From Figure 3-1, Positive slew rate is 101V/µs; Negative slew rate is 132 V/µs.

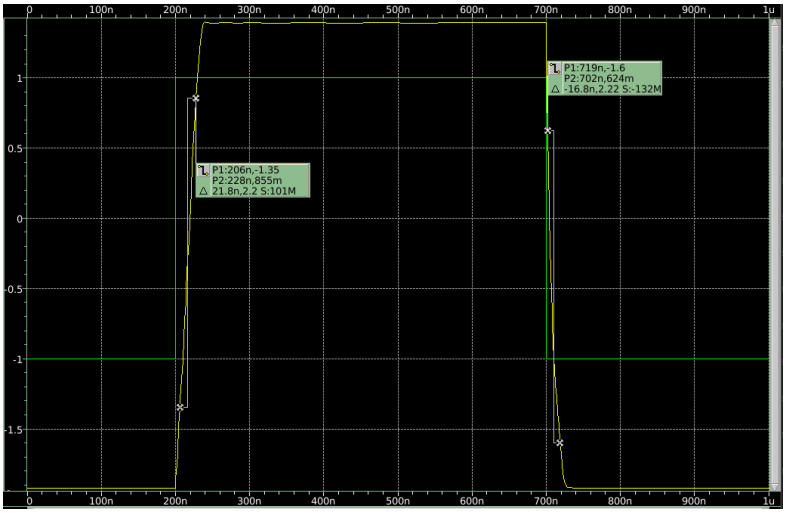

Figure 3-1 Simulation Result for Slew Rate

B. Power consumption: From Figure 3-2, Total power = 0.932m+0.0133m = 0.945mW

```
**** voltage sources

subckt
element  0:vs       0:vcm      0:vdd      0:voff     0:vss
 volts      0.          1.0000     1.0000     0.        -1.0000
 current    0.          0.       -466.0004u    0.       466.0004u
 power      0.          0.        466.0004u    0.       466.0004u

    total voltage source power dissipation=  932.0008u       watts


**** current sources

subckt   x1
element  1:ib
 volts      1.3258
 current   10.0000u
 power    -13.2579u


    total current source power dissipation= -13.2579u       watts
```

Figure 3-2 Simulation result for power consumption

C. Differential Output Swing: From Figure 3-3, Output voltage swing is ±1.5V.

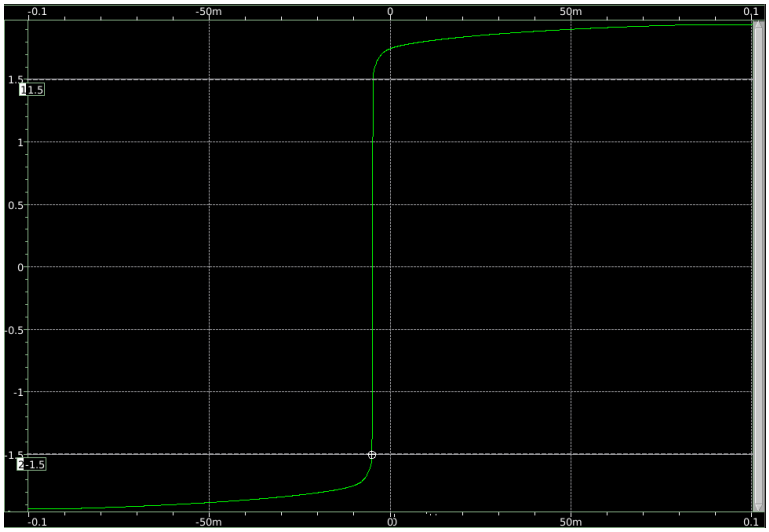

Figure 3-3 Simulation result for output swing

D. From Figure 3-4, DC Output: DC output is -0.197mV.

```
****** operating point information tnom=  25.000 temp=  25.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:100     =   0.       0:101     =   0.       0:102     =   0.
+0:vdd     =   1.0000   0:vin+    =   0.       0:vin-    =   0.
+0:vo+     =-197.0695u  0:vo-     =-197.0693u  0:vss     =  -1.0000
```

Figure 3-4 Simulation result for DC output

E. Input offset voltage: From Figure 3-5, Offset voltage is 5.64fV

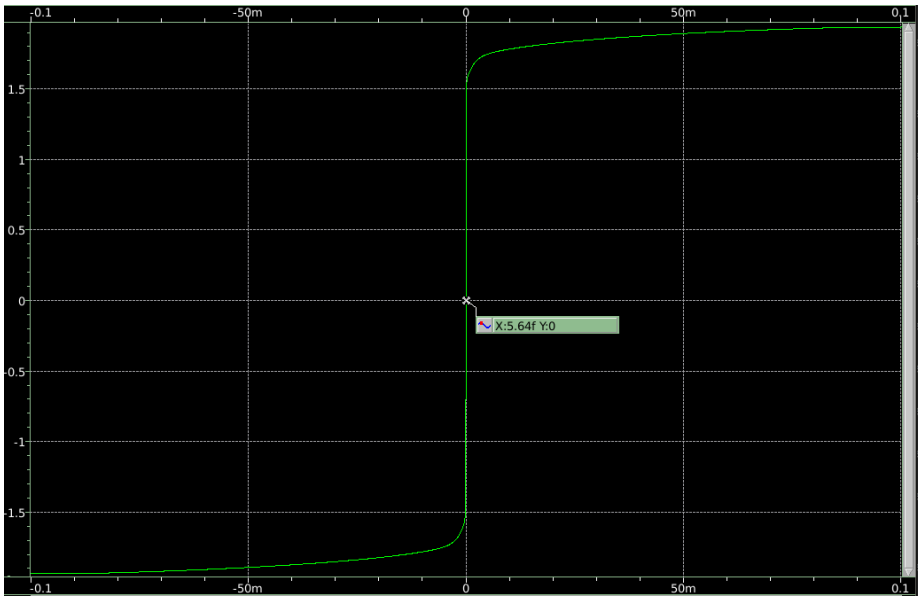

Figure 3-5 Simulation result for system offset voltage (without mismatch)

For worst case mismatching, the W of M01 is scaled 0.95 time while that of M02 is scaled 1.05 times. From Figure 3-6, the simulation result shows offset voltage is -4.83mV.

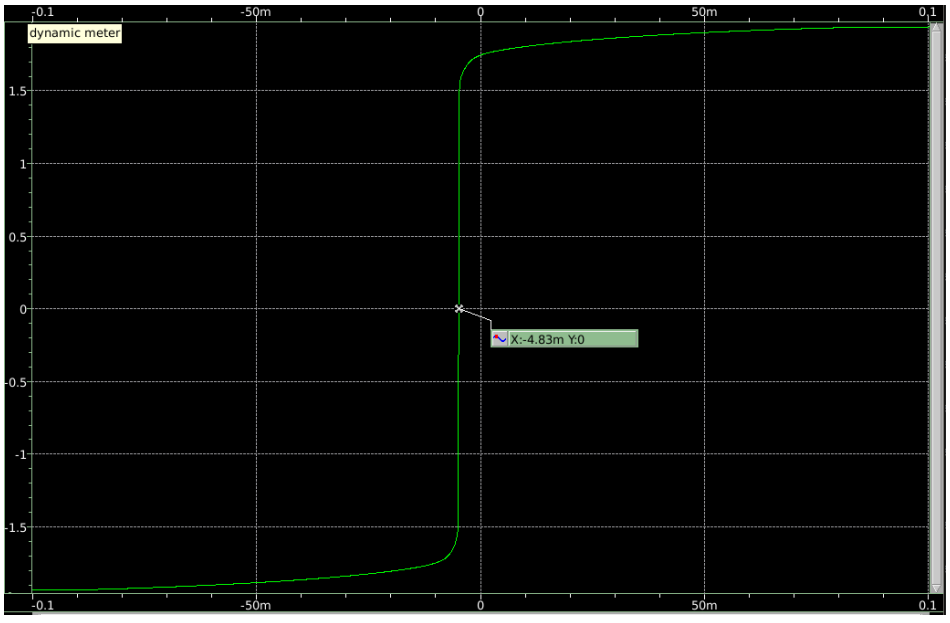

Figure 3-6 Simulation result for random offset voltage (worst case)

III. Comparison with calculated results

A. Slew Rate(SR)

The simulated SR is larger than the calculated result, it is because we have set the parasitic capacitance as 1pF for a bigger margin. Although the simulated I_1 is lower than the calculated result, the actual parasitic capacitance is smaller than 1pF which leads to a bigger value of SR.

B. Power Consumption

The simulated power consumption is lower than the calculated result, it is because the simulated I_1 is lower than the expected value, which contributes to the significantly drop of power consumption of the folded cascode amplifier.

C. Output Swing

The simulated output swing is higher than the calculated result, it is because the simulated V_{dsat} of M05, M06, M07, M08 have a lower value than we assumed.

D. DC output

The simulated DC output is -0.197mV which is close to 0V and our simulation result matches our calculation. As the DC output is sensitive to $Vgs_{13,14}$, we have tuned the size of M13, M14 so that the $Vgs_{13,14}$ to be exactly 1V and the voltage drop across M13, M14 close to 10mV.

E. Input Offset Voltage

The simulated input offset voltage is lower than the calculated result, this is because we have calculated the worse-case mismatches for mosfets and threshold voltage. However, the mismatch for threshold voltage is lower than we expected. The simulated result is still in the acceptable range.

IV. Problems encountered and solutions

1. When our team brought DC and AC calculation results to the simulation, we found out that some of the transistors entered linear region because of wrong biasing voltage. In view of this, we have separated the circuit into different functional blocks: folded cascode amplifier, auxiliary amplifier, CMFB and biasing circuit. With a fine tuning of WL ratio of transistors, we can ensure all the node voltages are as expected before combining all the blocks together.

2. When simulating the output swing, we found out the performance was not good enough. To optimize the result, we found out that the CMFB circuit controls the DC output and output swing, which is controlled by the size of M13, M14. In addition, from the simulation results, the output swing is sensitive to V_{gs} of M13, M14. By adjusting the WL ratio so that the V_{gs} M13 & M14 to be exactly 1V, the output swing finally satisfied the requirement.

4. AC Hand Calculation

I. Small-signal calculations

A. Unity Gain Frequency:

$UGF \geqslant 250MHz$

$$\frac{gm_1}{2\pi C_{out}} \geqslant 250MHz$$

$$gm_1 = \sqrt{2\mu_p c_{ox} I_1 \left(\frac{W}{L}\right)_{1,2}} \geqslant 3.14mA/V$$

$$\therefore \left(\frac{W}{L}\right)_{1,2} \geqslant 488$$

Therefore, we choose $\left(\frac{W}{L}\right)_{1,2} = 690$

$$gm_1 = \sqrt{2\mu_p c_{ox} I_1 \left(\frac{W}{L}\right)_{1,2}} = 3.74mA/V$$

$$\therefore UGF = \frac{gm_1}{2\pi C_{out}} = 297MHz$$

B. Low Frequency Gain:

$A_o = A_{main} A_{aux}$

$A_{main} = gm_1 R_{out}$

$R_{out} = R_{o6} \parallel R_{o8}$

$R_{o6} = r_{o6}(1 + gm_6 r_{o4})$

$R_{o8} = r_{o8}[1 + gm_8(r_{o1} \parallel r_{o10})]$

$$r_{o1,4,6} = \frac{1}{\lambda_p I_1} = 69.9k\Omega$$

$$r_{o8} = \frac{1}{\lambda_n \times 2I_1} = 25.6k\Omega$$

$$r_{o10} = \frac{1}{\lambda_n I_1} = 50.5k\Omega$$

$$gm_{6,8} = \frac{2I_1}{V_{ov}} = 1.1mA/V$$

$R_{out} = 736k\Omega$

$\therefore Amain = gm_1 R_{out} = 68.8dB$

From our design, A_{aux} *is set to* $20dB$.

$\therefore A_o = 88.2dB$

$$\therefore \left(\frac{W}{L}\right)_{3,4,5,6} = \frac{gm_6{}^2}{2\mu_p c_{ox} I_1} = 59.8$$

$$\therefore \left(\frac{W}{L}\right)_{7,8} = \frac{gm_8{}^2}{2\mu_n c_{ox} I_1} = 22.3$$

C. Phase Margin :

$$PM = 180° - \arctan\left(\frac{UGF}{P_{vo+}}\right) - \arctan\left(\frac{UGF}{P_8}\right)$$

$$= 180° - \arctan\left(\frac{297MHz}{\frac{1}{R_{out}C_{out}}}\right) - \arctan\left(\frac{297MHz}{\frac{1}{\frac{1}{gm_7}C_8}}\right)$$

$$= 61.8°$$

D. Equivalent Input Noise :

$$\frac{\overline{V_{eq}{}^2}}{\Delta f} = 2 \times 4kT \times \frac{2}{3}\left(\frac{1}{gm_1} + \frac{1}{gm_7 A_{aux}{}^2}\right)$$

$$= 6.11 \times 10^{-18} V/Hz$$

$$\therefore \sqrt{\frac{\overline{V_{eq}{}^2}}{\Delta f}}(at\ 1MHz\ BW) = 2.47\mu V\ rms$$

E. Common Mode Rejection Ratio :

$$CMRR = \frac{A_{dm}}{A_{cm}} = \infty$$

F. Power Supply Rejection Ratio :

$$PSRR = \frac{A_{dm}}{A_{supply}} = \infty$$

II. HSPICE simulation

A. Unity Gain Frequency, Low Frequency Gain and Phase Margin

From Figure 4-1, UGF is 314MHz, A_o is 88dB, PM is 180°–119° = 61°

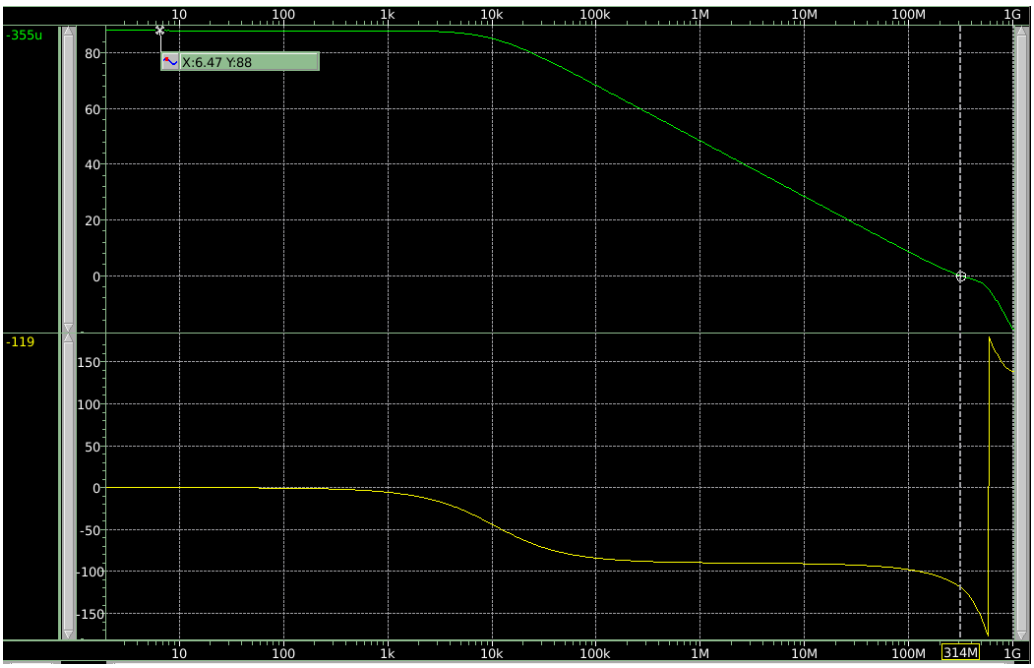

Figure 4-1 AC simulation results

B. Equivalent Input Noise

Without mismatch consideration, the equivalent input noise is 7.7474μV$_{rms}$.

```
**** the results of the sqrt of integral (v**2 / freq)
     from fstart upto    1.0000x      hz. using more freq points
     results in more accurate total noise values.

**** total output noise voltage    =   24.0955m       volts
**** total equivalent input noise =    7.7474u
```

Figure 4-2 Simulation result for Equivalent input noise (without mismatch)

With mismatch consideration the equivalent input noise is 9.4867μV$_{rms}$

```
**** the results of the sqrt of integral (v**2 / freq)
     from fstart upto    1.0000x      hz. using more freq points
     results in more accurate total noise values.

**** total output noise voltage    =  105.9502u       volts
**** total equivalent input noise =    9.4867u
```

Figure 4-3 Simulation result for equivalent input noise (worst case)

C. Common Mode Rejection Ratio (CMRR)

```
****     small-signal transfer characteristics

     v(vo+,vo-)/vs                              =   25.1022k
     input resistance at             vs         =  1.000e+20
     output resistance at v(vo+,vo-)            =   26.2666x
```

Figure 4-4 Simulation result for differential mode gain

```
****     small-signal transfer characteristics

     v(vo+,vo-)/vs                              =    8.3989u
     input resistance at             vs         =  1.000e+20
     output resistance at v(vo+,vo-)            =    1.3459k
```

Figure 4-5 Simulation result for common mode gain

$$CMRR = \frac{A_{DM}}{A_{CM}} = 20\log\left(\frac{25.1022k}{8.3989\mu}\right) = 189.52dB$$

D. Power Supply Rejection Ratio (PSRR)

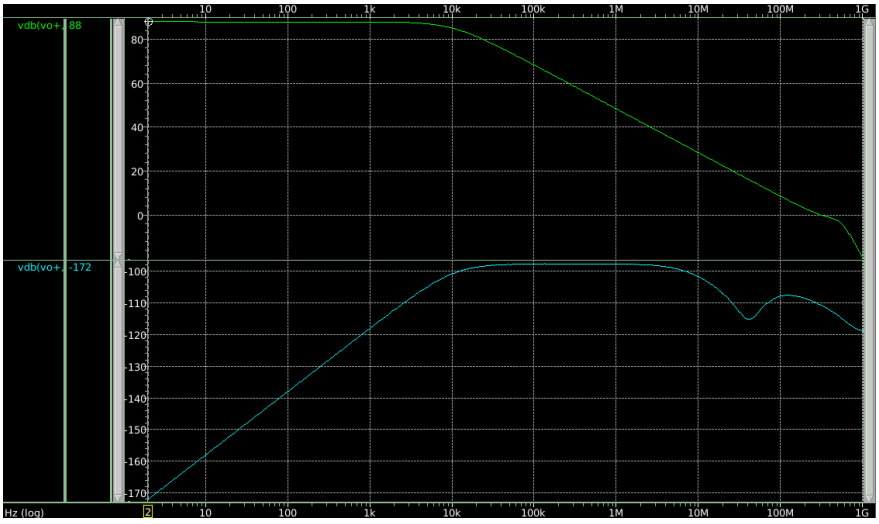

Figure 4-6 Simulation result for PSRR at DC

From Figure 4-6 above, PSRR at DC = 88-(-172) = 260dB

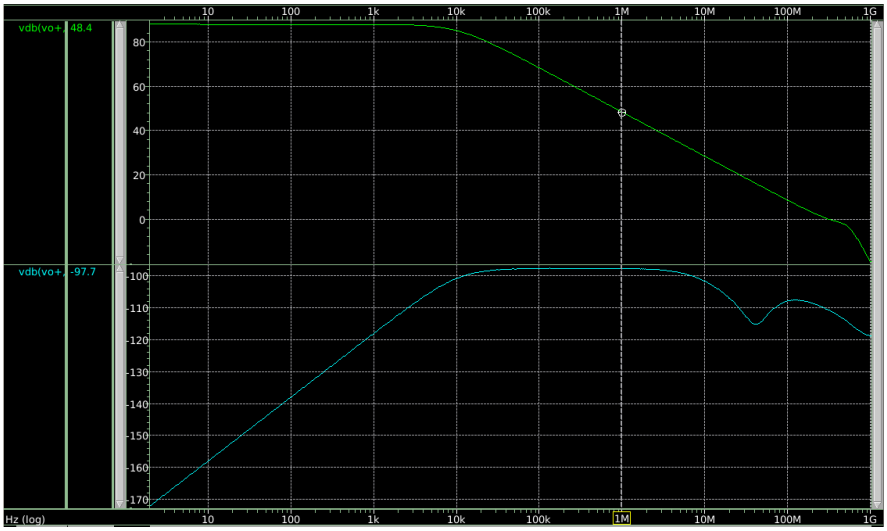

Figure 4-7 Simulation result for PSRR at 1MHz

From Figure 4-7, PSRR at 1MHz = 48.4-(-97.7) = 146.1dB

E. Total Harmonic Distortion:

Output voltage swing is $\pm 1.5V$. DC input for sine wave is $1.5V \times \frac{75\%}{2} = 0.5625V$

```
******
* eesm5120 amplifier design

****** transient analysis tnom=  25.000 temp=  25.000 ******
fourier components of transient response v(vo-,vo+)
dc component =  344.8109n

harmonic frequency  fourier    normalized phase      normalized
no       (hz)       component  component  (deg)      phase (deg)
1          30.0000k  996.6173m    1.0000    90.0094     0.
2          60.0000k  770.5046n  773.1198n  -93.1927  -183.2021
3          90.0000k    4.5173m    4.5326m   82.1143    -7.8951
4         120.0000k    2.7514u    2.7607u  -83.6542  -173.6636
5         150.0000k  938.2897u  941.4745u -102.0027  -192.0120
6         180.0000k    2.2524u    2.2600u  125.1418    35.1324
7         210.0000k    1.3585m    1.3631m -160.7125  -250.7219
8         240.0000k    1.5648u    1.5701u   48.9835   -41.0258
9         270.0000k    2.4808m    2.4892m   24.8215   -65.1879

total harmonic distortion =   0.543001  percent
```

Figure 4-8 Simulation result for total harmonic distortion

Total harmonic distortion = 20log(0.543001%) = -45.304dB

III. Comparison with calculated results

A. Unity Gain Frequency (UGF)

The simulated UGF is larger than the calculated result, it is because we have set the parasitic capacitance as 1pF for a bigger margin. However, the actual parasitic capacitance is smaller than 1pF which leads to a bigger value of UGF.

B. Phase Margin (PM)

The simulated PM is close to our calculation result, it means that we have included right dominant poles in the calculation.

C. Low Frequency Gain (A_o)

The simulated A_o is close to our calculation result; however, we have discovered that our simulated gm_1 are lower than the expected value while R_o is higher than the expected value. In such case, the gain of folded cascode amplifier equals to our calculated which makes our calculation matched with the simulation.

D. Equivalent Input Noise

The simulated input noise is smaller than the calculation result, this is because we have ignored flicker noise in our calculation. In addition, we have only included the thermal noise of folded-cascode and auxiliary amplifier but the biasing and CMFB block also contribute towards input noise.

E. Common Mode Rejection Ratio (CMRR) and Power Supply Rejection Ratio (PSRR)

For CMRR and PSRR, we have assumed they are infinity large as A_{cm} and A_{supply} equal to 0. In the simulated result, they are large enough to meet the specifications.

IV. Problems encountered and solutions

1. When simulating the folded-cascode amplifier and auxiliary amplifier, the transistor M07 & M08 had entered the linear region. In the AC hand calculation, our team assumed M03, M04, M05 and M06 had the same WL ratio and 1:4 WL ratio for M2:M1 and M3:M4 in Aux_p and Aux_n respectively. By fine tuning of their aspect ratio, we succeeded turning M07 & M08 into saturation region.

5. Conclusion

Our team of two has achieved to design and simulated a low-power, high output swing, high differential gain amplifier. The amplifier employed regulated folded cascode structure with gain boosting and common mode feedback. This amplifier consumes only 0.945mW, with low frequency gain of 88dB, UGF of 314MHz, output swing of ±1.5V. The simulation shows all the parameters of the amplifier are met.

All team members have a chance to practice the design flow of analog circuits from hand calculation to simulation. We had a comprehensive understanding of regulated cascode technique and common mode feedback technique. The hand calculation and simulation result breakdown give us great help of which parameter to tune, when there are some unexpected results or certain requirement is not met.

For the possible improvements of the circuit, we can improve further on the gain by further increasing the current, since we still have quite some power margin. Our design consumes less than half of the requirement (0.945mW<= 2mW), and the resulting gain can still reach 88dB. Increasing the current should also further increases the slew rate as well.

6. Individual contribution

Name	**Tasks**	**Contribution**
Lam King Sum Sam	Hand Calculation, circuit sizing Biasing circuit design, Report write up	50%
Tse Ming Fung Alfred	Netlist and simulation, Auxiliary amplifier biasing, Feedback circuit sizing, Report write up	50%

Reference

[1] Howard Luong, EESM5120 Lecture Notes, Advanced Amplifier Design Techniques

[2] EESM5120 2021 Spring HW1 suggested solution

[3] Razavi, B., 2016. Design of analog CMOS integrated circuits Second., New York, NY: McGraw-Hill Education

Appendix

I. Device aspect ratio

	Transistor	W(um)	L(um)	Transistor	W(um)	L(um)
Main Amplifier (Folded-Cascode Amplifier)	M01	124.2	0.18	M06	21.6	0.18
	M02	124.2	0.36	M07	8.028	0.36
	M03	64	0.36	M08	8.028	0.36
	M04	64	0.36	M09	30.456	0.36
	M05	21.6	0.36	M10	30.456	0.36
Bias Circuit	M11	1.85	0.36	M18	1.1	0.36
	M12	1.22	0.36	M19	1.222	0.36
	M15	1.06	0.36	M20	1.68	0.36
	M16	7.1	0.36	M21	1.74	0.36
	M17	60.25	0.36	M22	2.74	0.36
Common Mode Feedback Circuit	M13	19.6	0.36	M14	19.6	0.36
Aux_p (NMOS input stage)	M01	10.94	0.36	M03	2.44	0.36
	M02	2.6	0.36	M04	4.88	0.36
Aux_n (PMOS input stage)	M01	2.23	0.36	M03	0.8	0.36
	M02	1.11	0.36	M04	4	0.36

II. Auxiliary amplifier design

$$For\ Aux_p,\ \left(\frac{W}{L}\right)_1 : \left(\frac{W}{L}\right)_2 = 4:1\ \&\ \left(\frac{W}{L}\right)_3 : \left(\frac{W}{L}\right)_4 = 1:2$$

$$For\ Aux_n,\ \left(\frac{W}{L}\right)_1 : \left(\frac{W}{L}\right)_2 = 2:1\ \&\ \left(\frac{W}{L}\right)_3 : \left(\frac{W}{L}\right)_4 = 1:4$$

$$Set\ I_{aux} = 30\mu A$$

$$\therefore I_{M1} = 20\mu A,\ I_{M2} = 10\mu A$$

$$Set\ A_{aux} = 10 = 20dB$$

$$A_{aux} = gmRo = gm\left(\frac{1}{\lambda_p I_1} \parallel \frac{1}{\lambda_n I_1}\right)$$

$$\therefore gm = 62\mu A/V$$

$$\because gm = \mu cox\left(\frac{W}{L}\right)(V_{gs} - V_t)$$

$$By\ setting\ primary\ \frac{W}{L}\ ratio\ and\ fine\ tuning,$$

$$For\ Aux_p,\ \left(\frac{W}{L}\right)_1 = 30.4,\ \left(\frac{W}{L}\right)_2 = 7.22,\ \left(\frac{W}{L}\right)_3 = 6.78,\ \left(\frac{W}{L}\right)_4 = 13.6$$

$$For\ Aux_n,\ \left(\frac{W}{L}\right)_1 = 6.47,\ \left(\frac{W}{L}\right)_2 = 3.08,\ \left(\frac{W}{L}\right)_3 = 2.22,\ \left(\frac{W}{L}\right)_4 = 11.1$$

III. Folded cascode amplifier netlist

```
** Subcircuit - Folded Cascode Amplifier with CMFB **
.include 'aux_p'
.include 'aux_n'

.subckt folded_cascode_amp   vdd   vss   vin+  vin-  vo+   vo-

** Parameter Define **
.para len=0.36u
.para len1=0.18u
.para w1=124.2u   w2=w1
*.para            w1=117.99u
*.para            w2=130.41u
.para w3=64u      w4=w3
.para w5=21.6u    w6=w5
.para w7=8.028u   w8=w7
.para w9=30.456u  w10=w9
.para w11=1.85u
.para w13=19.6u   w14=w13
.para w17=60.25u
.para w12=1.22u   w20=1.68u
.para w15=1.06u   w16=7.1u
.para w18=1.1u    w19=1.222u
.para w22=2.74u   w21=1.74u

** Circuit Netlist **
m01   8     vin+  2     vdd   cmosp w=w1  l=len1
+as='w1*0.54u'    ad='w1*0.54u'     ps='2*w1+2*0.54u'      pd='2*w1+2*5.4u'
m02   9     vin-  2     vdd   cmosp w=w2  l=len1
+as='w2*0.54u'    ad='w2*0.54u'     ps='2*w2+2*0.54u'      pd='2*w2+2*5.4u'
m03   4     3     vdd   vdd   cmosp w=w3  l=len
+as='w3*0.54u'    ad='w3*0.54u'     ps='2*w3+2*0.54u'      pd='2*w3+2*5.4u'
m04   5     3     vdd   vdd   cmosp w=w4  l=len
+as='w4*0.54u'    ad='w4*0.54u'     ps='2*w4+2*0.54u'      pd='2*w4+2*5.4u'
m05   vo-   12    4     vdd   cmosp w=w5  l=len
+as='w5*0.54u'    ad='w5*0.54u'     ps='2*w5+2*0.54u'      pd='2*w5+2*5.4u'
m06   vo+   13    5     vdd   cmosp w=w6  l=len
+as='w6*0.54u'    ad='w6*0.54u'     ps='2*w6+2*0.54u'      pd='2*w6+2*5.4u'
m07   vo-   14    8     vss   cmosn w=w7  l=len
+as='w7*0.54u'    ad='w7*0.54u'     ps='2*w7+2*0.54u'      pd='2*w7+2*5.4u'
m08   vo+   15    9     vss   cmosn w=w8  l=len
+as='w8*0.54u'    ad='w8*0.54u'     ps='2*w8+2*0.54u'      pd='2*w8+2*5.4u'
m09   8     10    vss   vss   cmosn w=w9  l=len
+as='w9*0.54u'    ad='w9*0.54u'     ps='2*w9+2*0.54u'      pd='2*w9+2*5.4u'
m10   9     10    vss   vss   cmosn w=w10 l=len
+as='w10*0.54u'   ad='w10*0.54u'    ps='2*w10+2*0.54u'     pd='2*w10+2*5.4u'
m11   1     1     vdd   vdd   cmosp w=w11 l=len
+as='w11*0.54u'   ad='w11*0.54u'    ps='2*w11+2*0.54u'     pd='2*w11+2*5.4u'
m12   10    10    vss   vss   cmosn w=w12 l=len
+as='w12*0.54u'   ad='w12*0.54u'    ps='2*w12+2*0.54u'     pd='2*w12+2*5.4u'
m13   11    vo-   vdd   vdd   cmosp w=w13 l=len
+as='w13*0.54u'   ad='w13*0.54u'    ps='2*w13+2*0.54u'     pd='2*w13+2*5.4u'
m14   11    vo+   vdd   vdd   cmosp w=w14 l=len
+as='w14*0.54u'   ad='w14*0.54u'    ps='2*w14+2*0.54u'     pd='2*w14+2*5.4u'
m15   3     10    vss   vss   cmosn w=w15 l=len
+as='w15*0.54u'   ad='w15*0.54u'    ps='2*w15+2*0.54u'     pd='2*w15+2*5.4u'
m16   3     3     vdd   vdd   cmosp w=w16 l=len
+as='w16*0.54u'   ad='w16*0.54u'    ps='2*w16+2*0.54u'     pd='2*w16+2*5.4u'
m17   2     1     11    vdd   cmosp w=w17 l=len
+as='w17*0.54u'   ad='w17*0.54u'    ps='2*w17+2*0.54u'     pd='2*w17+2*5.4u'
m18   7     10    vss   vss   cmosn w=w18 l=len
+as='w18*0.54u'   ad='w18*0.54u'    ps='2*w18+2*0.54u'     pd='2*w18+2*5.4u'
m19   7     7     vdd   vdd   cmosp w=w19 l=len
+as='w19*0.54u'   ad='w19*0.54u'    ps='2*w19+2*0.54u'     pd='2*w19+2*5.4u'
m20   10    1     vdd   vdd   cmosp w=w20 l=len
+as='w20*0.54u'   ad='w20*0.54u'    ps='2*w20+2*0.54u'     pd='2*w20+2*5.4u'
m21   6     1     vdd   vdd   cmosp w=w21 l=len
+as='w21*0.54u'   ad='w21*0.54u'    ps='2*w21+2*0.54u'     pd='2*w21+2*5.4u'
m22   6     6     vss   vss   cmosn w=w22 l=len
+as='w22*0.54u'   ad='w22*0.54u'    ps='2*w22+2*0.54u'     pd='2*w22+2*5.4u'

x1    vdd   vss   6     4     12    aux_p
x2    vdd   vss   6     5     13    aux_p
x3    vdd   vss   7     8     14    aux_n
x4    vdd   vss   7     9     15    aux_n

ib    1     vss   10u

.ends
************************
```

IV. Auxiliary amplifier netlists

AUX_N: PMOS as input stage

```
** Subcircuit - aux_n **
.subckt     aux_n vdd   vss   vi+   vi-   vo

m1    vo    vi+   vdd   vdd   cmosp w=2.23u     l=0.36u     m=0.8
+as='2.23u*0.54u'ad='2.23u*0.54u' ps='2*2.23u+2*0.54u'   pd='2*2.23u+2*0.54u'

m2    2     vi+   vdd   vdd   cmosp w=1.11u     l=0.36u     m=0.8
+as='1.11u*0.54u'ad='1.11u*0.54u' ps='2*1.11u+2*0.54u'   pd='2*1.11u+2*0.54u'

m3    vo    2     vss   vss   cmosn w=0.8u      l=0.36u     m=0.8
+as='0.8u*0.54u' ad='0.8u*0.54u'  ps='2*0.8u+2*0.54u'    pd='2*0.8u+2*0.54u'

m4    2     2     vi-   vss   cmosn w=4u  l=0.36u     m=0.8
+as='4u*0.54u'   ad='4u*0.54u'    ps='2*4u+2*0.54u'pd='2*4u+2*0.54u'

.ends
************************
```

AUX_P: NMOS as input stage

```
** Subcircuit - aux_p **
.subckt     aux_p vdd   vss   vi+   vi-   vo

m1    1     1     vi-   vdd   cmosp w=10.94u    l=0.36u     m=0.8
+as='10.94u*0.54u'     ad='10.94u*0.54u'ps='2*10.94u+2*0.54u'  pd='2*10.94u+2*0.54u'

m2    vo    1     vdd   vdd   cmosp w=2.6u      l=0.36u     m=0.8
+as='2.6u*0.54u' ad='2.6u*0.54u'  ps='2*2.6u+2*0.54u'    pd='2*2.6u+2*0.54u'

m3    1     vi+   vss   vss   cmosn w=2.44u     l=0.36u     m=0.8
+as='2.44u*0.54u'ad='2.44u*0.54u' ps='2*2.44u+2*0.54u'   pd='2*2.44u+2*0.54u'

m4    vo    vi+   vss   vss   cmosn w=4.88u     l=0.36u     m=0.8
+as='4.88u*0.54u'ad='4.88u*0.54u' ps='2*4.88u+2*0.54u'   pd='2*4.88u+2*0.54u'

.ends
************************
```