ELEC 4320 Term Project —— QPSK Implementation

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QPSK Implementation

Introduction

Quadrative phase-shift keying (QPSK), is a special form of Phase-shift Keying (PSK). It indicates a higher-order implementation of PSK. In QPSK modulation, phase changes with input data while keeping frequency and amplitude unchanged. In quadrature of QPSK, there are 4 different states represented by a combination of 00, 01, 10, 11. The first bit represent in-phase components (I) and the second bit represent the quadrature components (Q).

As shown in figure 1, in general QPSK modulator, the input binary bitstream will first be divided into even and odd streams. The two streams will then pass a Non Return Zero (NRZ) Encoder in order to change to data into bipolar. After that, the coded data streams will be mixed with their corresponding carrier signal, defined as sine and cosine basis function. After superimposing the signals, odd data (I phase) and even phase (Q phase) will be added together to produce a QPSK signal.

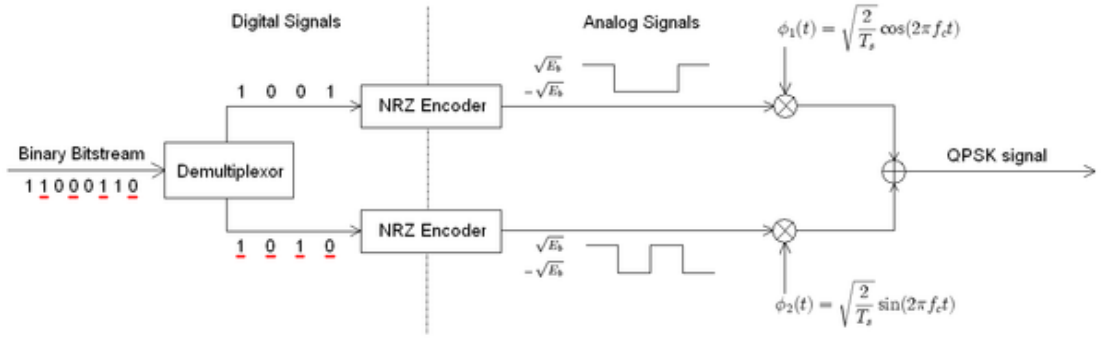

Figure 1: Conceptual Structure of QPSK

Figure 2 shows the general mathematical form of a QPSK signal, where f_c is the carrier frequency, E_s is the energy symbols and T_s is the symbol period. From the equation, it gives four phases π/4 (45 °), 3π/4 (135 °), 5π/4 (225 °) and 7π/4 (315 °) as needed.

$$s_n(t) = \sqrt{\frac{2E_s}{T_s}} \cos\left(2\pi f_c t + (2n-1)\frac{\pi}{4}\right), \quad n = 1, 2, 3, 4.$$

Figure 2: The general mathematical form of a QPSK signal

Figure 3 shows the first basis function used as the in-phase component of the carrier signal and the second as the quadrature component of the carrier signal.

$$\phi_1(t) = \sqrt{\frac{2}{T_s}} \cos(2\pi f_c t)$$

$$\phi_2(t) = \sqrt{\frac{2}{T_s}} \sin(2\pi f_c t)$$

Figure 3: The in-phase & quadrature carrier signal function

QPSK uses four points on the constellation diagram, equispaced around a circle. With four phases, QPSK can encode two bits per symbol (00, 01, 10, 11) shown in the figure 4.

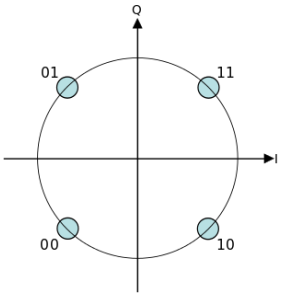

Figure 4: Constellation diagram for QPSK

Methodology

In this project, we have successfully implemented a QPSK modulator in a FPGA broad. The QPSK signal have 100khz central frequency and 200kbps data rate is achieved.

Figure 5. BeMicro Max 10 FPGA development broad

We have chosen BeMicro Max 10 FPGA development broad to work with. The FPGA included in the broad is 10M08DAF484, Which have 8k LEs and 414Kbit ROM on broad. The Broad also include a 12-bit 2Msps DAC named AD5681R. this ADC is created by analog device. Its data interface is SPI. Since our FPGA is intel product, Quartus, a software developed by altera which acquire by intel, is use as a FPGA IDE in this project.

Figure 6. Hantek6022BL desktop oscilloscope

To test our QPSK signal, A desktop oscilloscope is used. The scope is manufactured by Hantek. It had 20Mhz bandwidth. This scope enables us to obtain QPSK signal from the FPGA broad to computer.

Algorithm

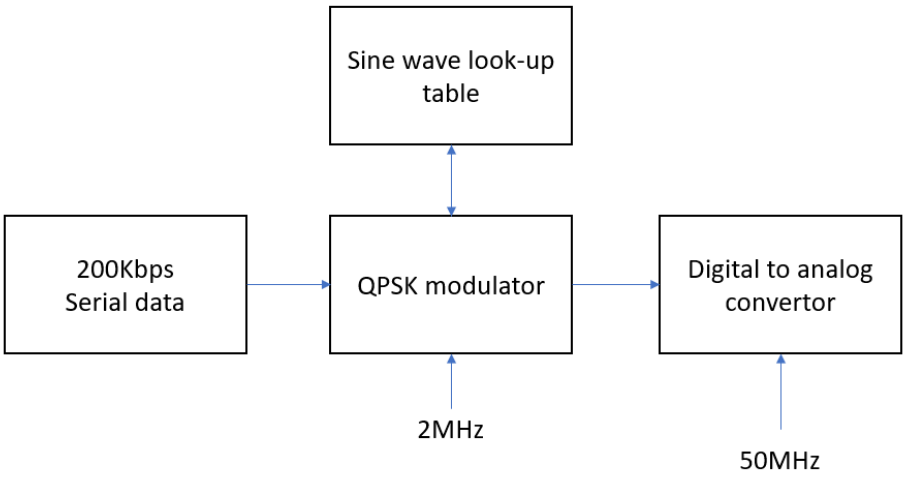

Figure 7. Block diagram for the FPGA program

This Project consist of 3 part, they are Sine wave look-up table, QPSK module and DAC controller.

The DAC controller is response to translate the data into the format that the AD5681R can take. By reviewing the datasheet of AD5681R, it is discovered that the DAC takes 24 bits as a command. Inside the 24 bits, it contains 4 bits command data and 20 bits DAC data. Since this DAC can only convert 12 bits data into analog, only first 12 bits out of 20 Bits data are valid. To shorten the sample time, a command named “Write DAC and input register” is used. This command can update the DAC register and change the analog output at the same time.

To implement this module, state machine is used. There are 25 stage to control output. First 24 stage is data output. the finial stage is to load the data for next cycle. Because of it, the sample frequency is

$$\frac{50Mhz}{25} = 2Mhz$$

For the sine lock-up table, we sample a cycle of sine wave with 20 sampling point and load it into ROM. This ROM is created by intel IP core. Since a cycle of sine wave is constructed by 20 sample point, the frequency of the sine wave is:

$$\frac{2Mhz}{20} = 100Khz$$

For the QPSK modulator, it uses the sine lock-up table to construct a complete sine wave. it uses serial input data to determine the starting point of the sine wave and send 1 cycle of sine wave (20 sample). By varying the starting point, the phase angle varies. Since QPSK take 2 bits per 1 symbol, this modulator will update the buffer when two bits are received. And at the end of a cycle of a symbol, it use the buffer to determine the starting point. Since QPSK take 2 bits per 1 symbol, the bit rate is twice as fast as the symbol rate.

$$100Khz * 2bit = 200Kbps$$

Implementation

To implement the design into FPGA, Quartus is used. For demo purpose a serial emulator module is built. This module will send b01001000 constantly at 200Khz so we can obtain all symbol in QPSK.

The clock is provided by Intel IP core. This core takes advantage of the Phase lock loop module on the FPGA and generated the 50Mhz clock, 2Mhz clock and 200Khz clock for the serial emulator.

After Compiling the design. We know there are 69 logic elements, 240 bit memory and 1 Phase lock loop are used.

Flow Status	Successful - Sun Dec 22 21:17:34 2019
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	QPSKtoplevel
Top-level Entity Name	QPSKtoplevel
Family	MAX 10
Device	10M08DAF484C8GES
Timing Models	Preliminary
Total logic elements	69 / 8,064 (< 1 %)
Total registers	48
Total pins	6 / 250 (2 %)
Total virtual pins	0
Total memory bits	240 / 387,072 (< 1 %)
Embedded Multiplier 9-bit elements	0 / 48 (0 %)
Total PLLs	1 / 2 (50 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 1 (0 %)

Figure 8. resource used to implement the design

To enable the DAC, Some pin assignment is done accordingly.

To	Direction	Location	I/O Bank	VREF Grou	Fitter Loca	I/O Standa	Reserved	Current St	Slew Rate	Differenti	Strict Preservation
CLKin	Input	PIN_N14	6	B6_N0	PIN_N14	2.5 V					
CLKout	Output	PIN_G17	6	B6_N0	PIN_G17	2.5 V					
LDAC	Output	PIN_N18	6	B6_N0	PIN_N18	2.5 V					
RESET	Output	PIN_L15	6	B6_N0	PIN_L15	2.5 V					
SDI	Output	PIN_H17	6	B6_N0	PIN_H17	2.5 V					
SYNC	Output	PIN_N19	6	B6_N0	PIN_N19	2.5 V					

Figure 9. QPSK Pinout

Simulation Result

The QPSK modulator is under simulation.

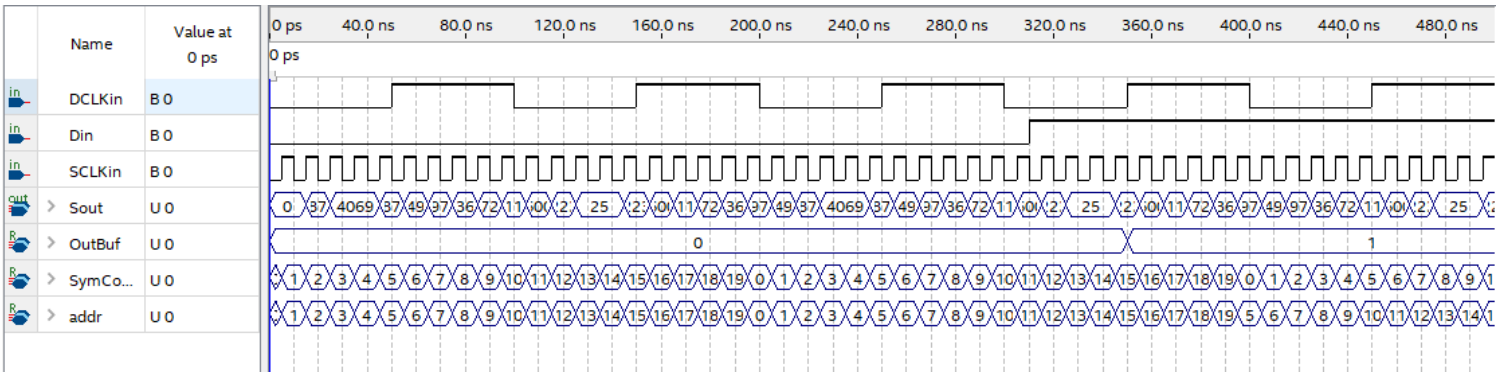

Figure 10. The modulator is able to change the buffer accordingly

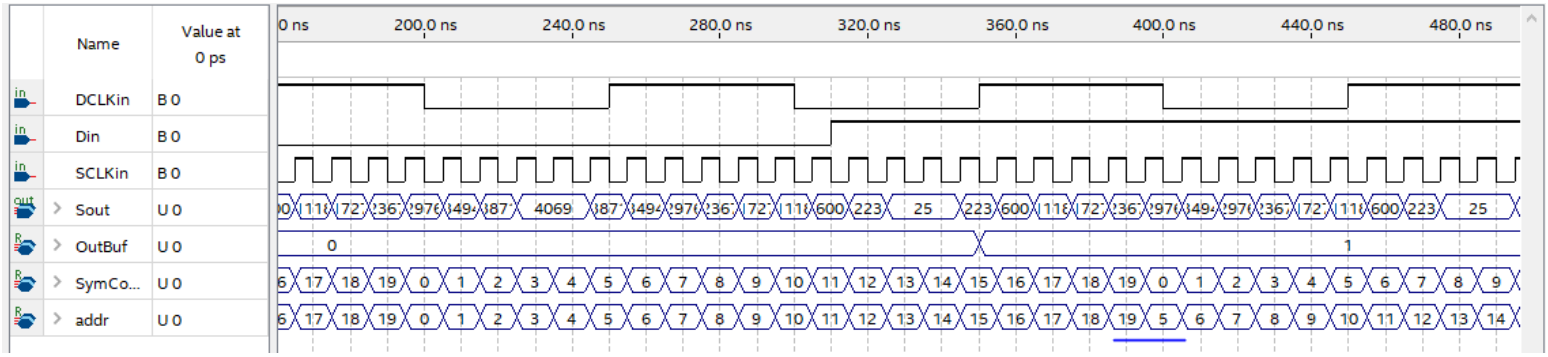

Figure 11. The modulator is able to change the starting point accordingly

For more detail, please check the photo named QPSK simulation wavefrom.png which in the folder we submitted or run the simulation yourself.

Result Comparison

From the figure 12, the QPSK signal waveform indicates different encoded states. It is used to verify whether our result satisfies with the input bitstream. To test our implementation is correctly built, we will match the simulation and excel results with the waveform in figure 12 to get the encoded bit. If both simulation results get the same encoded bitstream, then our implementation is proved correct.

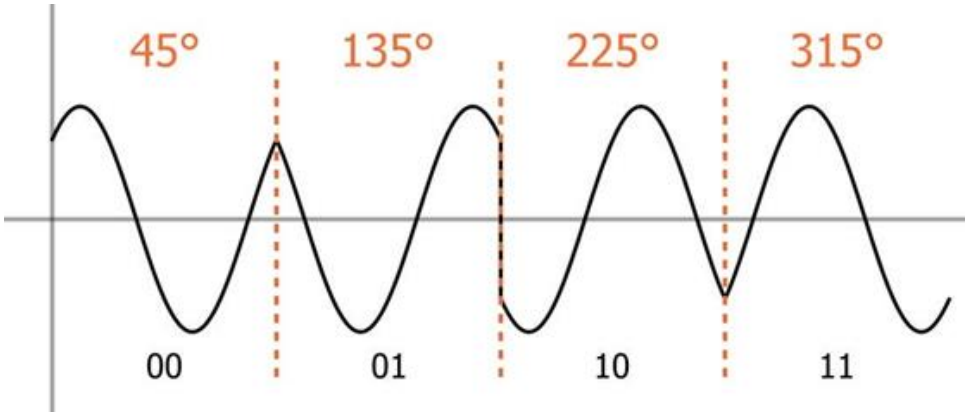

Figure 12: QPSK signal waveform

According to figure 13 and 14, by matching waveform with figure 12, both Hantek6022BL desktop oscilloscope and excel give the same encoded data bitstream 1000111100001111000. Therefore, the results satisfy our expectation. Thus, our implementation is correctly verified.

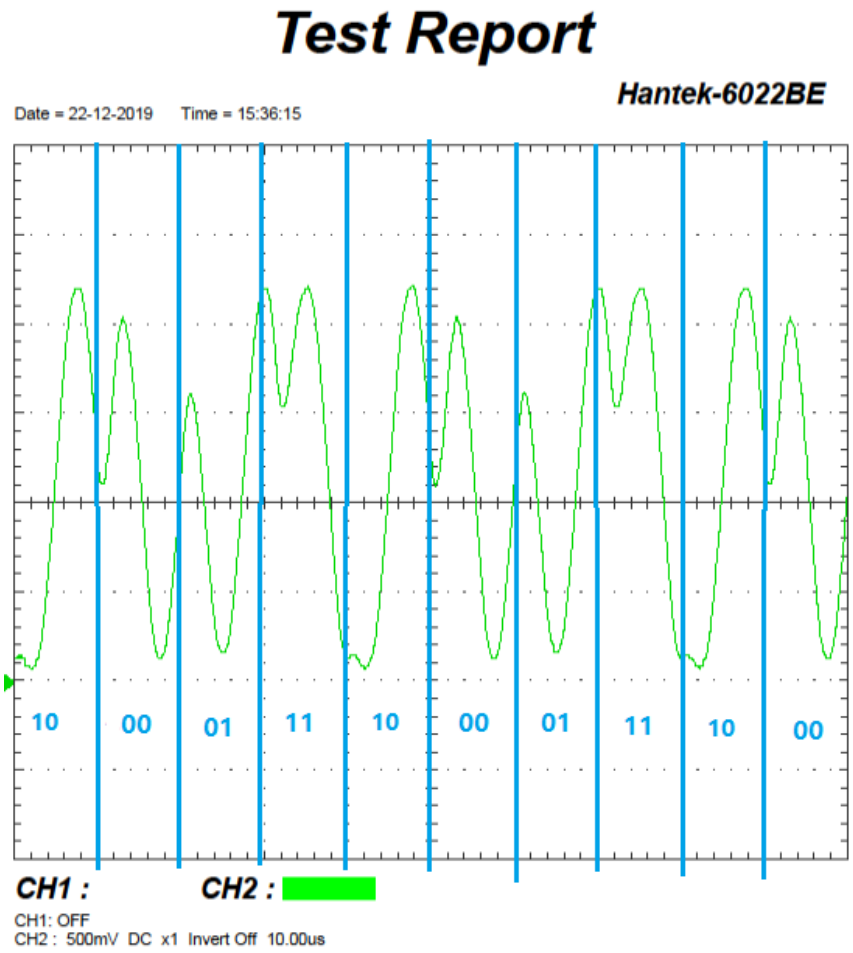

Figure 13: QPSK Test waveform from Hantek6022BL

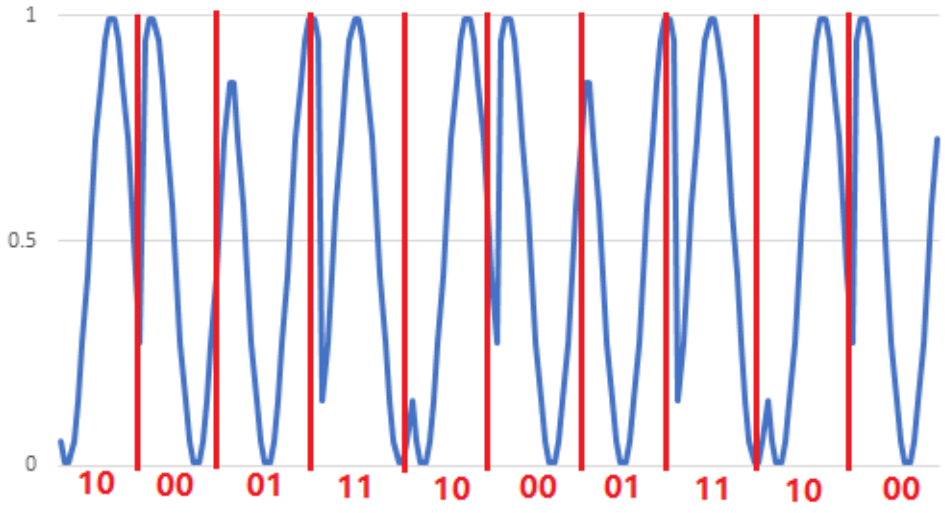

Figure 14: QPSK waveform from excel simulation

Reference:

R. Keim, “Understanding Quadrature Phase Shift Keying (QPSK) Modulation - Technical Articles” 17-Aug-2016. [Online]. Available: https://www.allaboutcircuits.com/technical-articles/quadrature-phase-shift-keying-qpsk-modulation/. [Accessed: 22-Dec-2019].

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"Tiny 16-/14-/12-Bit SPI nanoDAC+, with ±2 (16-Bit) LSB INL and 2 ppm/°C Reference Data Sheet" 2016. [Online]. Available: https://www.intel.com/content/dam/altera-www/global/en_US/uploads/e/ec/BeMicro_Max_10-Schematic_A4-20141008.pdf. [Accessed: 22-Dec-2019].