EESM 5900I Project Report

Group 18

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Introduction

Full adder is the basic component of arithmetic circuit, it can be applied to addition, multiplication, division circuits. Therefore, as the building blocks of complex circuits, the performance of full adder could affect the overall system performance.

A full adder consists of 3 inputs (A, B, C_{in}). It takes A, B as operands and C_{in} as carry bit. Full adder will produce 2 outputs (Sum and Carry).

Here is the logic equation of the sum and carry derived from the truth table.

$Carry = AB + BC_{in} + AC_{in}$

$Sum = (A+B+C_{in})(!Carry)+ABC_{in}$

Input			Output	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

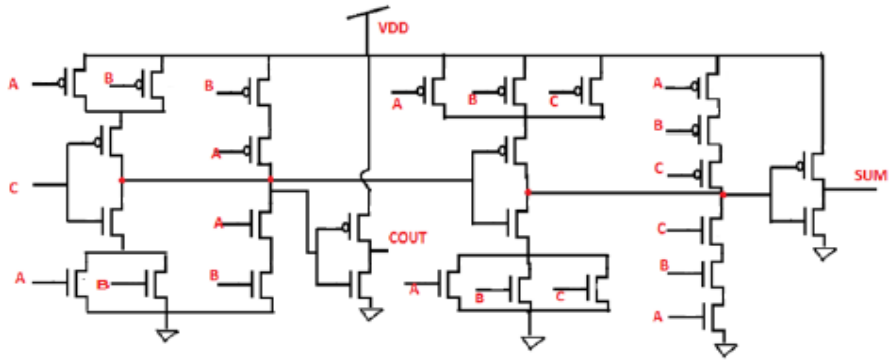
Project Objective

1. Design a full adder in static complementary CMOS design style.
2. Design a full adder in dynamic domino CMOS design style.
3. Compare the number of transistors, output delay and power consumption between two different design styles.

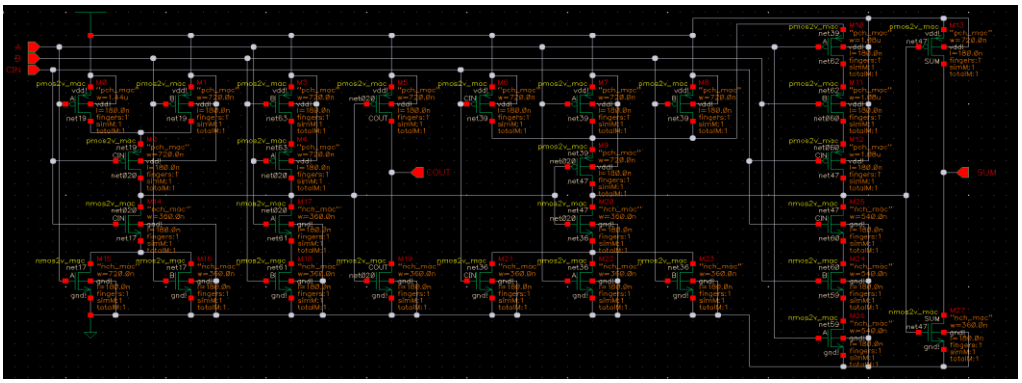
CMOS DESIGN

Static Complementary CMOS

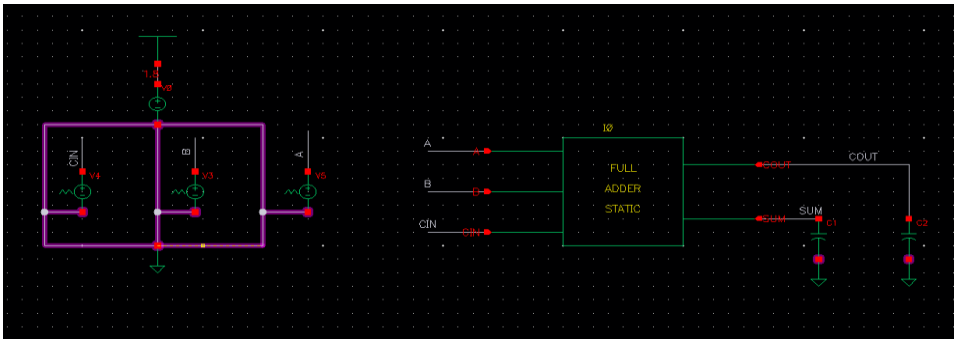
The static complementary CMOS design consists of a PMOS pull up network (PUN) and NMOS pull down network (PDN).



Circuit diagram of a full adder



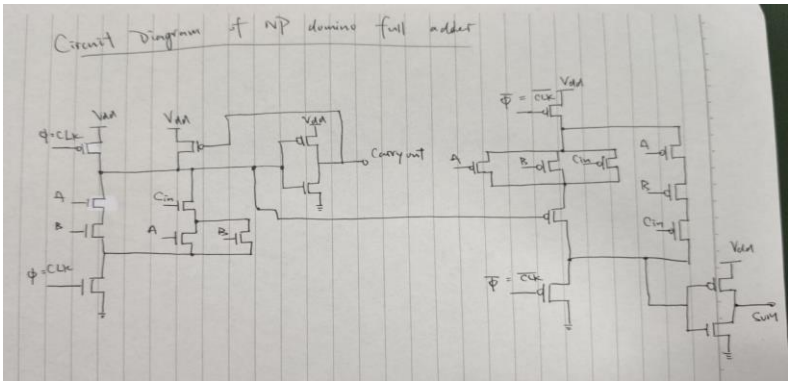
Schematic diagram of the static C2MOS full adder in Virtuoso



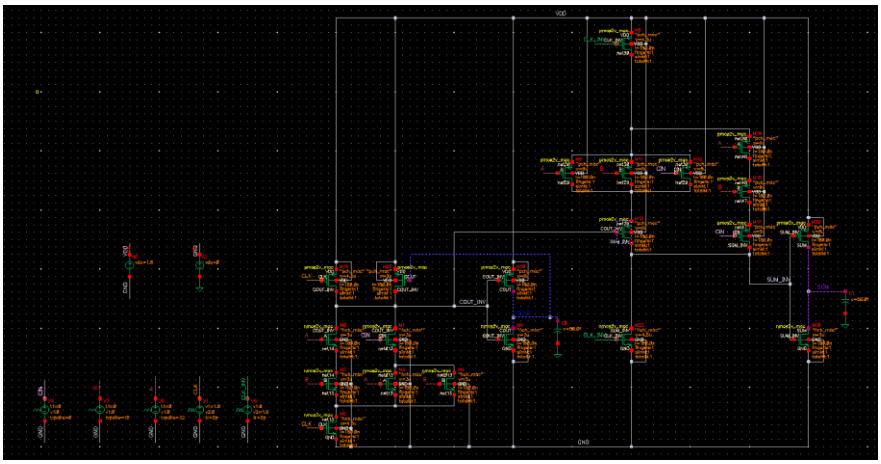
Schematic diagram for the test of full adder

NP Domino

NP Domino logic design is achieved by alternatively cascading PUN and PDN. To execute the PUN and PDN simultaneously, the PDN is controlled by clock signal and PUN is controlled by inverse clock signal. As each stage only involves either PDN or PUN, the chip area will be reduced. In addition, a latching PMOS (M23 in schematic) is inserted acting as a level restorer to minimize the problem of charge sharing.



Circuit diagram of the dynamic domino full adder

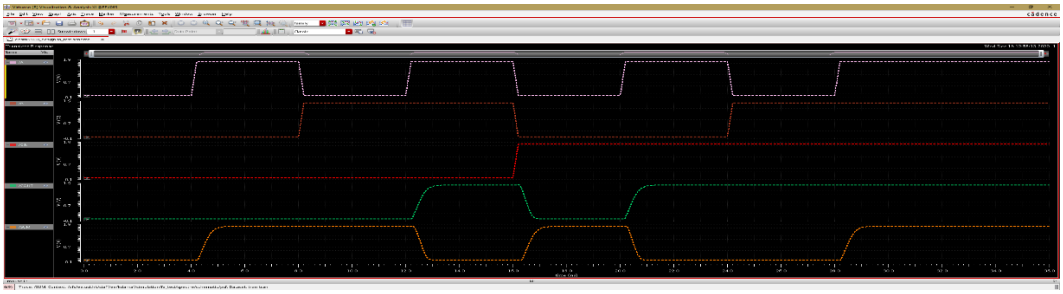


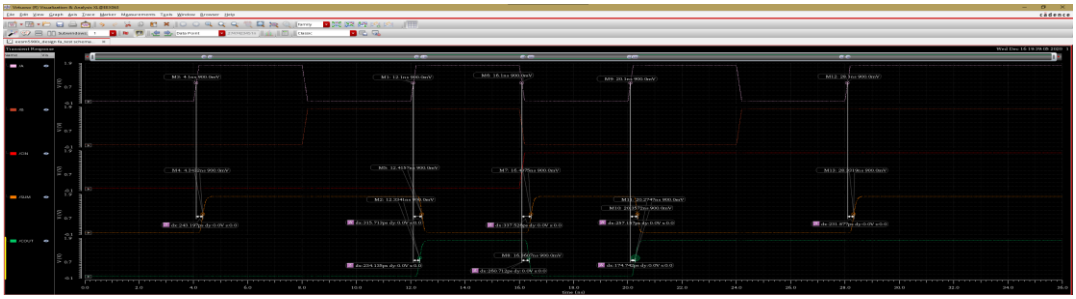
Schematic diagram of the dynamic domino full adder with testbench

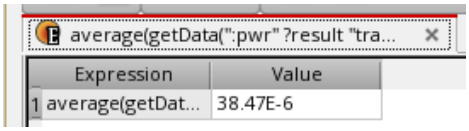
Result and Analysis

Static Complementary CMOS

The following figure is the output pattern of static complementary CMOS design. The output trace of sum and carry match with the truth table result. Therefore, the design functionality is correct.

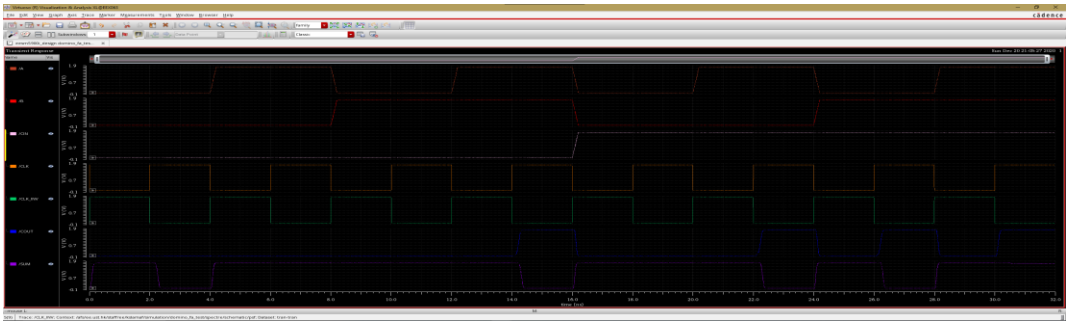


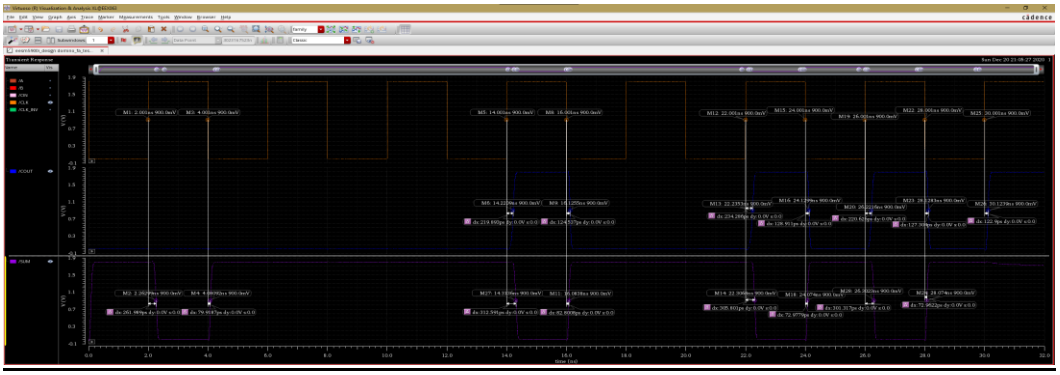


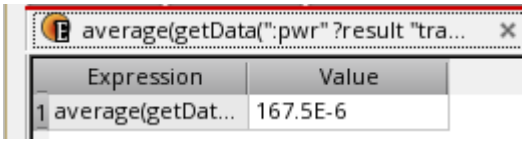


Dynamic Domino

The following figure is the output pattern of NP domino style design. The output trace of sum and carry match with the truth table result. Therefore, the design functionality is right.







Performance table summary

	No of transistor	Sum delay	Carry out delay	Power
Static C2MOS	28	277ps	223ps	38.5uW
NP domino	21	186ps	168ps	167.5uW

Design Style Comparison

1. Chip Area

From the table, the number of gates in dynamic domino is less than that of static C2MOS, more chip area will be saved in dynamic domino style.

2. Delay

From the table, the NP domino full adder has a shorter sum delay and carry out delay time than static C2MOS, the NP domino full adder has a faster speed.

3. Power

From the table, the power consumption of NP domino style is higher than static C2MOS.

Conclusion

In this project, two different design of full adder is presented, namely static complementary style and NP domino style. After the comparison of the simulation results, we could observe that different design style has its pros and cons. For static C2MOS design, it has lower power consumption but it introduces longer delay time and uses larger chip area. For dynamic NP domino design, it has shorter delay time and smaller chip area but it consumes more power.