Lam King Sum Sam (20423789)
Tse Ming Fung Alfred (20756435)

Radio-Frequency Integrated-Circuit Design

RF Project Report

Summary

The table below shows the comparison summary of the designed receiver:

Parameters	Specifications	Calculation	Simulation
Frequency Range	5.15 - 5.25 GHz (lower band), 5.25 - 5.35 GHz (middle band)		
Channel Spacing	20 MHz		
No of Channels / Band	4		
Data Rate	6 - 54 Mbits/s		
Sensitivity	-82 dBm for 6 MBits/s, -65 dBm for 54 MBits/s		
Maximum Input Level	-30 dBm	N/A	-30 dBm
Voltage Gain	> 40 dB	51 dB	51.96 dB
NF	< 10 dB	7.81 dB	8.65 dB
IIP3	> -18 dBm	-12.88 dBm	-12.79 dBm for if_I -12.58 dBm for if_Q
Input Impedance	50 Ω		
Input Impedance Matching S11	< -15 dB	-infinity dB	-264.957dB
Image Rejection	> 50 dB	60 dB	N/A
Power Consumption	Minimum	159 mW	N/A
Channel-Selection Filter Attenuation	> 15 dBc for adjacent channel > 30 dBc for alternating channel	24 dBc for adjacent channel @ 60 MHz 36 dBc for alternating channel @80 Mhz	19.40 dBc for adjacent channel @ 60 MHz 34.75 dBc for alternating channel @80 MHz
LO's Phase Noise	< -130 dBc/Hz @ 20 MHz offset	N/A	-132 dBc/Hz @ 20 MHz offset
ADC's SNR	> 48 dB		
Modulation	OFDM		

Table 1 Receiver Specification Summary

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Introduction

In this project, we have designed an integrated wireless receiver at the system level to meet WLAN 802.11a specifications and to verify the performance using Verilog-A behavioral simulations.

For the reciever topology, a dual conversion reciever architecture is used, which is the combination of heterodyne and direct-conversion style. The RF signal will first enter the heterodyne stage and mix with LO1 to convert the signal to a lower frequency IF1, the signal will then enter the direct-conversion stage and mix with LO2 to further down-converted to a lower frequency IQ signal IF2. In the block diagram shown in figure 1, 18 building blocks are used for the reciever design, namely 3 Ports, 2 LNAs, 3 Mixers, 2 LOs, 4 Buffers, 2 Filters and 2 VGAs.

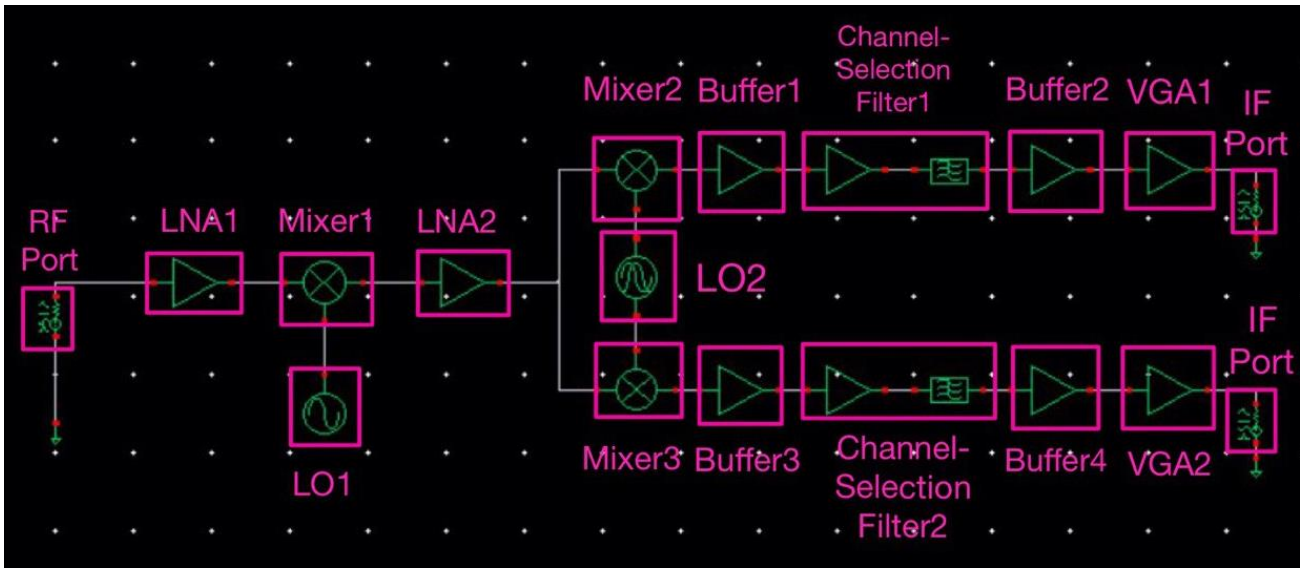

Figure 1: Receiver system diagram

Frequency planning

As the sqecified frequency range is 5.15-5.35 GHz, we set the frequency of RF signal to be 5.2 GHz. For LOs, we select the ratio of LO1 and LO2 to be 2:1. To reduce the effect of DC offset and flicker noise, we set the IF2 frequency to be 40 MHz which is close to the baseband frequency. Therefore, LO1 frequency = (5.2G – 40M)*2/3 = 3.44G Hz. LO2 frequency = (5.2G – 40M)*1/3 = 1.72 GHz.

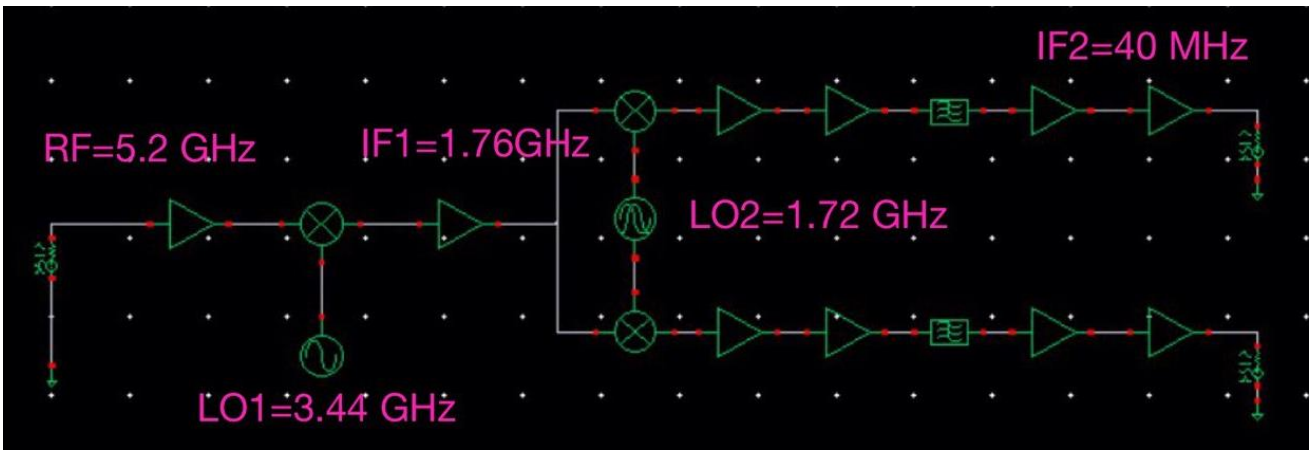

Figure 2: Frequency Planning Diagram

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Building blocks explanation and trade-off

a. LNA

From the equation of cascaded noise figure, it is mainly contributed by the first block. Therefore, LNA1 is mainly used for providing low noise figure.

	Gain (dB)	NF (dB10)	IIP3 (dBm)	Power (mW)	Trade-off
LNA1	20	3	-3	21	NF: -1dB, IIP3: +2dB, Power: +40%
LNA2	19	3	-3	18	Gain: -1dB, NF: -1dB, IIP3: +2dB, Power: +20%

Figure 3: Parameters of LNA1

Figure 4: Parameters of LNA2

b. Mixer

For power of LO, the value is 0 dBm which are set in the simulation. For Mixer2,3's input impedance, as IQ channel technique is used, the input impedance is set at 100 Ω in order to fulfill the input matching. For mixer's IIP2, we set the value same as IIP3 for a better linearity. In addition, mixer's isolation parameters are set to be 100 dB in order to minimize the effect of leakage between RF, LO and IF. For LO2, IR mixer is used which is expected to provide 30 dB IR ratio.

	Gain (dB)	NF (dB10)	IIP3 (dBm)	Power (mW)	Trade-off
Mixer1	-20	18	20	10	Gain: -18dB, NF: -2dB
Mixer2,3	0	16	18	28	Gain: +2dB, NF: -4dB, IIP3: -2dB, Power: +40%

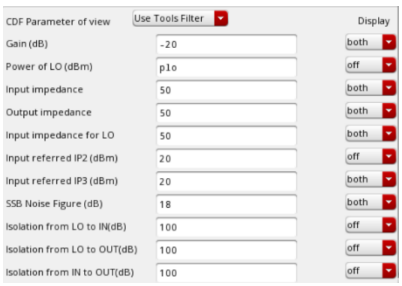

Figure 5: Parameters of Mixer1

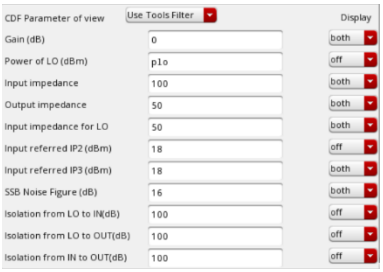

Figure 6: Parameters of Mixer2,3

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c. Oscillator (LO1) and Quadrature Oscillator (LO2)

For LO's noise floor, after we sweeped through different values, we set it to be -132 dBc/Hz in order to minimize the noise figure. In addition, we set the LO's phase noise to be -132 dBc/Hz @ 20MHz offset because the expected value is lower than -130 dBc/Hz @ 20MHz.

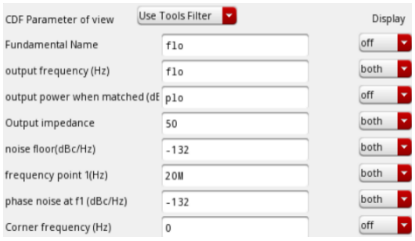

Figure 7: Parameters of Oscillator (LO1)

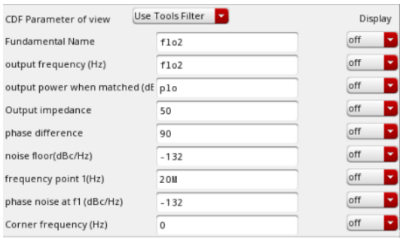

Figure 8: Parameters of Quadrature Oscillator (LO2)

d. Buffer

As off-chip filter is chosen, buffers are used to compensate the loss of the long interconnection.

	Gain (dB)	NF (dB10)	IIP3 (dBm)	Power (mW)	Trade-off
Buffer1,2,3,4	0	17	13	11	Gain: +2dB, NF: -3dB, IIP3: +3dBm, Power: +120%

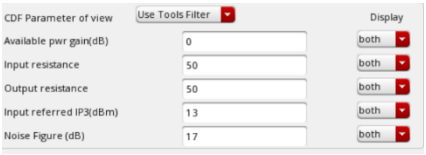

Figure 9: Parameter of buffer

e. IR Filter

From the requirement of filter attenuation, according to the Characteristic curve of 0.1 dB ripple Chebyshev filter, we chose N=5 to give enough margin for attenuation. On the other hand, off-chip filter is chosen as the channel-selection filter due to its low noise figure and high IIP3. As the filter has -6dB gain after simulation, in order to compensate the gain as well as insert the noise figure and IIP3, a LNA is added before the filter. The corner frequency is set at 40 MHz which is equal to IF2 frequency from the frequency planning.

	Gain (dB)	NF (dB10)	IIP3 (dBm)	Order N	Power (mW)	Trade-off
Filter1,2	0	9	22	5	0	Gain: +6dB, NF: +3dB, IIP3: -8dBm, Order N: +1

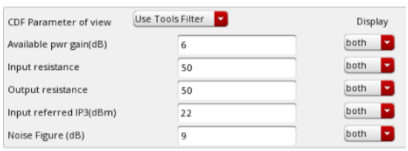

Figure 10: Parameters of filter1,2

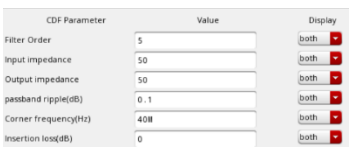

Figure 11: Parameters of LNA

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f. VGA

The last stage of the receiver is VGA, which mainly amplifies the weak filtered IF2 signal. Moreover, as we have enough gain from the previous blocks, we can trade gain for NF and IIP3.

	Gain (dB)	NF (dB10)	IIP3 (dBm)	Power (mW)	Trade-off
VGA1,2	32	17	13	5	Gain: -8dB, NF: -3dB, IIP3: +3dB

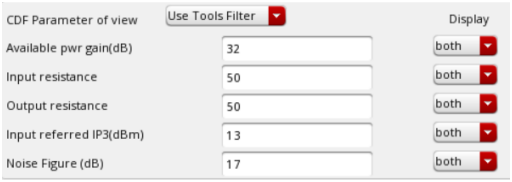

Figure 12: Parameters of VGA1,2

System parameters estimation

Table 2: Summary of building block parameters

	LNA1	Mixer1	LNA2	Mixer2	Buffer1	Filter1	Buffer2	VGA1
Gain (G) | dB20	20	-20	19	0	0	0	0	32
Power Gain (A_p) | V/V	100	0.01	79.4328	1	1	1	1	1584.893
Noise Figure (NF) | dB10	3	18	3	16	17	9	17	17
Noise Factor (F)	1.99526	63.0957	1.99526	39.8107	50.1187	7.94328	50.1187	50.1187
Linearity IIP3 | dBm	-3	20	-3	18	13	22	13	13
Linearity IIP3 | W	0.000501	0.1	0.000501	0.063095	0.019952	0.158489	0.019952	0.019952
Image Rejection (IR) | dB	0	0	0	30	0	30	0	0
Power (P) | mW	21	10	18	28	11	0	11	5

Assumption :
Assume all the output in a block will perfectly match will the nect cascading block.
ie : The input impedance matching $S11 = 0$

1. $Voltage\ Gain = \sum G = G_{LNA1} + G_{Mixer1} + G_{LNA2} + G_{Mixer2} + G_{Buffer1} + G_{Filter1} + G_{Buffer2} + G_{VGA1} = 51\ dB$

2. *From Friis's equation, the cascaded noise figure* (F_T)

$$F_T = F_{LNA1} + \frac{F_{Mixer1}-1}{A_{LNA1}} + \frac{F_{LNA2}-1}{A_{LNA1}A_{Mixer1}} + \frac{F_{Mixer2}-1}{A_{LNA1}A_{Mixer1}A_{LNA2}} + \frac{F_{Buffer1}-1}{A_{LNA1}A_{Mixer1}A_{LNA2}A_{Mixer2}} + \frac{F_{Filter1}-1}{A_{LNA1}A_{Mixer1}A_{LNA2}A_{Mixer2}A_{Buffer1}} + \frac{F_{Buffer2}-1}{A_{LNA1}A_{Mixer1}A_{LNA2}A_{Mixer2}A_{Buffer1}A_{Filter1}} + \frac{F_{VGA1}-1}{A_{LNA1}A_{Mixer1}A_{LNA2}A_{Mixer2}A_{Buffer1}A_{Filter1}A_{Buffer2}}$$

$F_T = 6.042594791$
$\therefore$ *Cascaded noise factor* $(NF_T) = 10log(F_T) \approx 7.81\ dB$

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3. *The cascaded lineaity $IIP_{3,T}$ is calculated from the following equation :*

$$\frac{1}{IIP_{3,T}} \approx \frac{1}{IIP_{3,LNA1}} + \frac{A_{p,LNA1}}{IIP_{3,Mixer1}} + \frac{A_{p,LNA1}A_{p,Mixer1}}{IIP_{3,LNA2}} + \frac{A_{p,LNA1}A_{p,Mixer1}A_{p,LNA2}}{IIP_{3,Mixer2}} + \frac{A_{p,LNA1}A_{p,Mixer1}A_{p,LNA2}A_{p,Mixer2}}{IIP_{3,Buffer1}} + \frac{A_{p,LNA1}A_{p,Mixer1}A_{p,LNA2}A_{p,Mixer2}A_{p,Buffer1}}{IIP_{3,Filter1}} + \frac{A_{p,LNA1}A_{p,Mixer1}A_{p,LNA2}A_{p,Mixer2}A_{p,Buffer1}A_{p,Filter1}}{IIP_{3,Buffer2}} + \frac{A_{p,LNA1}A_{p,Mixer1}A_{p,LNA2}A_{p,Mixer2}A_{p,Buffer1}A_{p,Filter1}A_{p,Buffer2}}{IIP_{3,VGA1}}$$

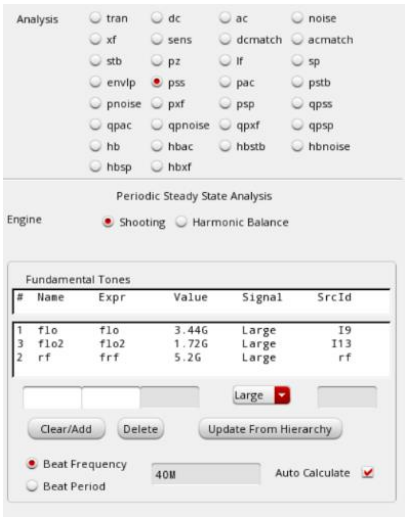
$$\therefore IIP_{3,T} = 55.2732\ \mu W \approx -12.57\ dBm$$

4. *Image Rejection (IR) ratio* $= IR_{Mixer2} + IR_{Filter1} = 60\ dB$

5. *Power* $= \sum P = P_{LNA1} + P_{Mixer1} + P_{LNA2} + 2(P_{Mixer2} + P_{Buffer1} + P_{Filter1} + P_{Buffer2} + P_{VGA1}) = 159mW$

Simulation

a. Power Gain simulation



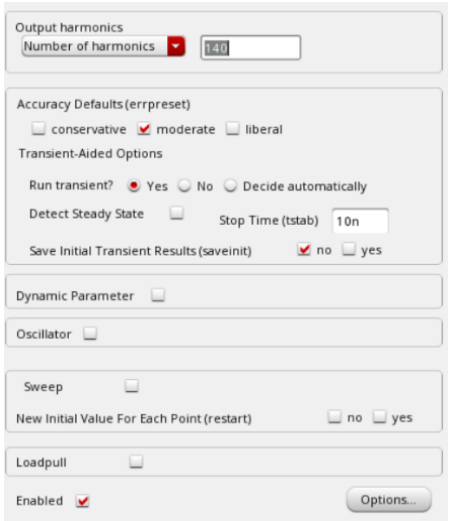


Figure 13: PSS simulation setup

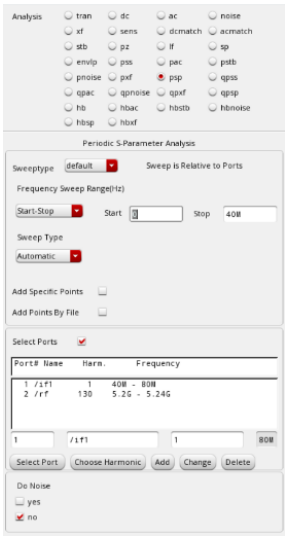


Figure 14: PSP simulation setup

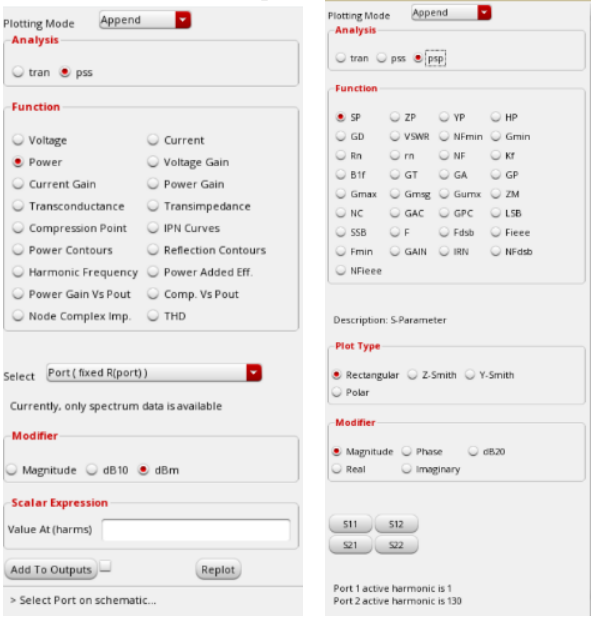


Figure 15: Voltage gain and S11 plot settings

Since the input impedance and output impedances of the system are matched to be both 50Ω, the power gain is equal to voltage gain: 1.96057dBm-(-50.0011dBm) = **51.962dBm**

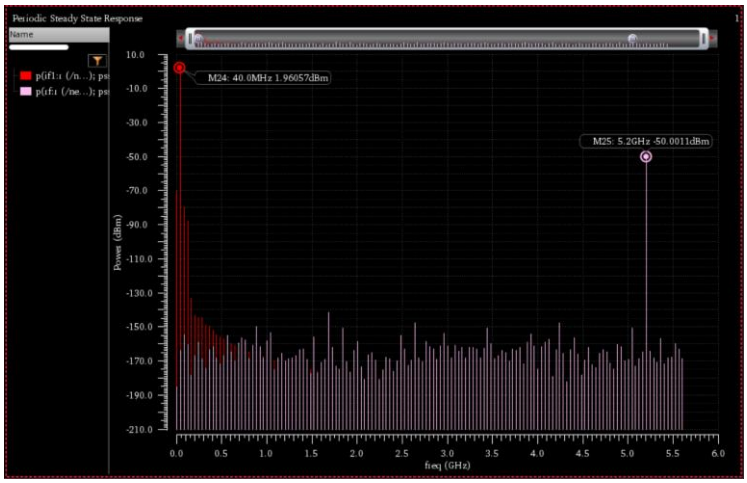


Figure 16: Voltage gain result

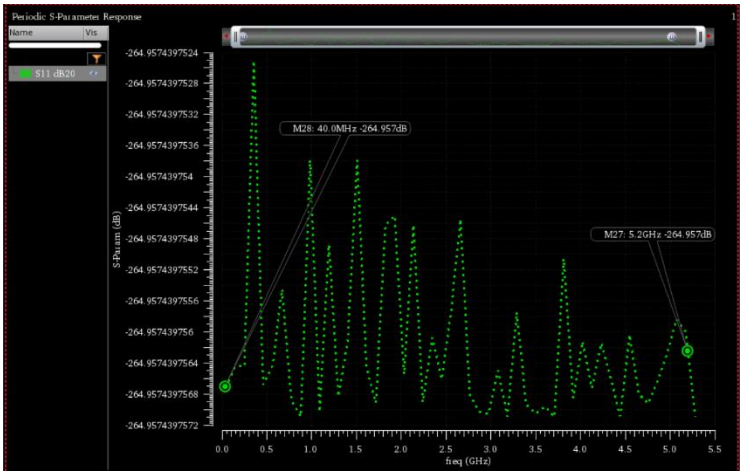


Figure 17: Input impedance result S11

b. Noise Figure Simulation

Figure 18 rf port setup

Figure 19 pnoise simulation setup1

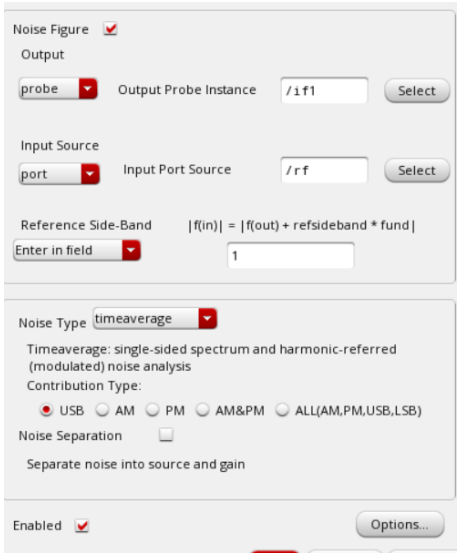


Figure 20 pnoise simulation setup2

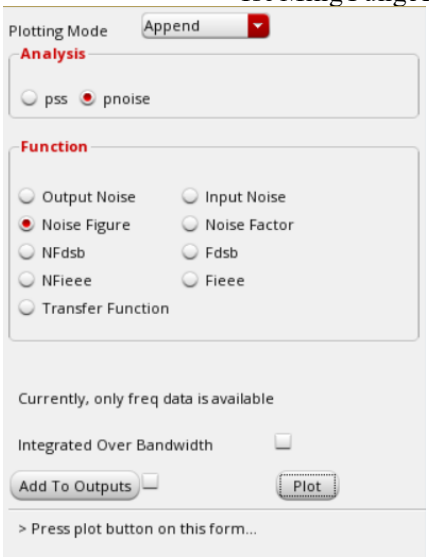


Figure 21 pnoise plot settings

Simulated Noise Figure = **8.65dB**

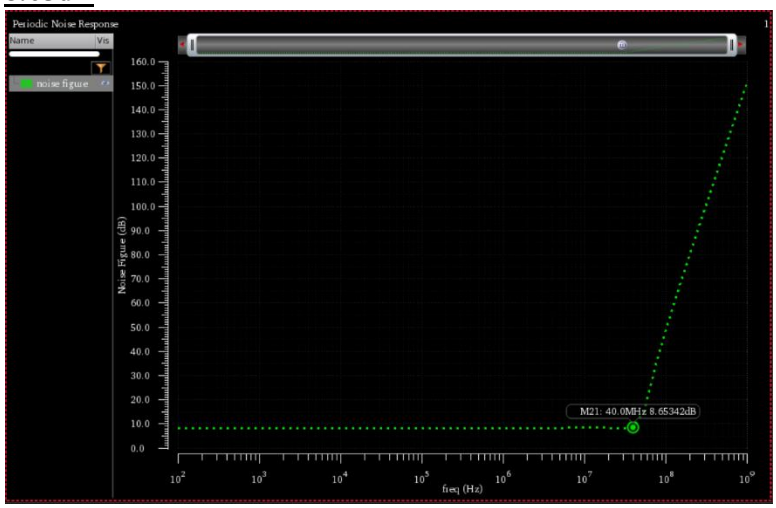


Figure 22: Noise figure result

c. IIP3 Simulation

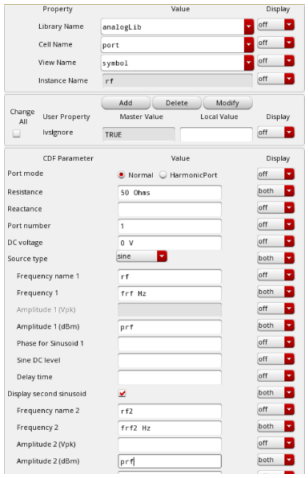


Figure 23 rf port setup

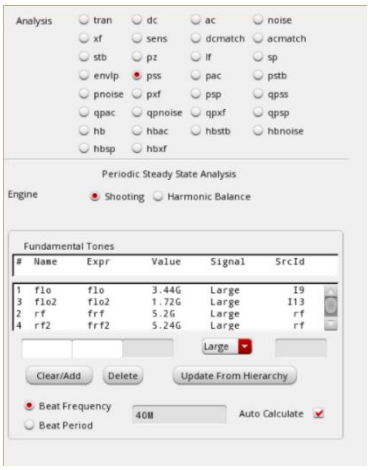


Figure 24 PSS simulation setup1

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Figure 25 PSS simulation setup2

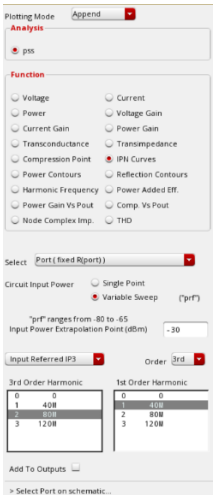

Figure 26 IIP3 plot settings

In phase if port IIP3 = **-12.79dBm**; quadrature phase if port IIP3 = **-12.58dBm**

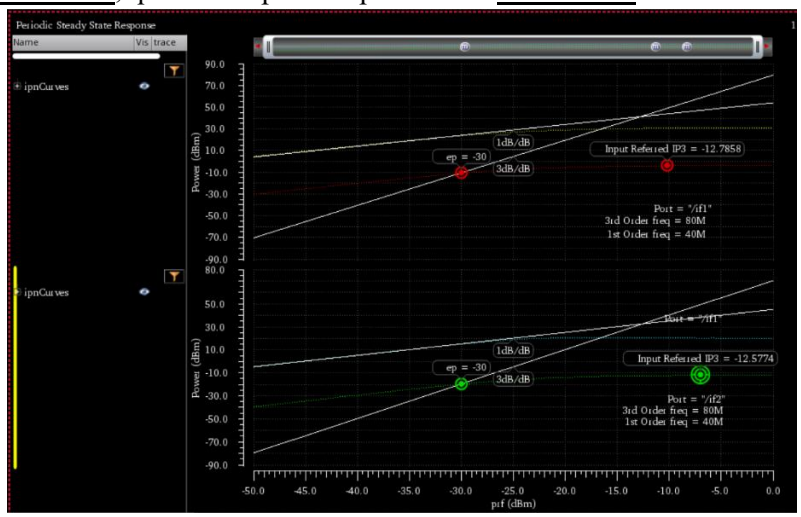

Figure 27: IQ channel IIP3 results (/if1 ->I, /if2 ->Q)

d. Channel selection filter attenuation

For adjacent channel @ 60 MHz, attenuation = -6.1206-(-40.86845) = 19.40dBc

For alternating channel @80 MHz, attenuation = -6.1206-(-25.51937) = 34.75dBc

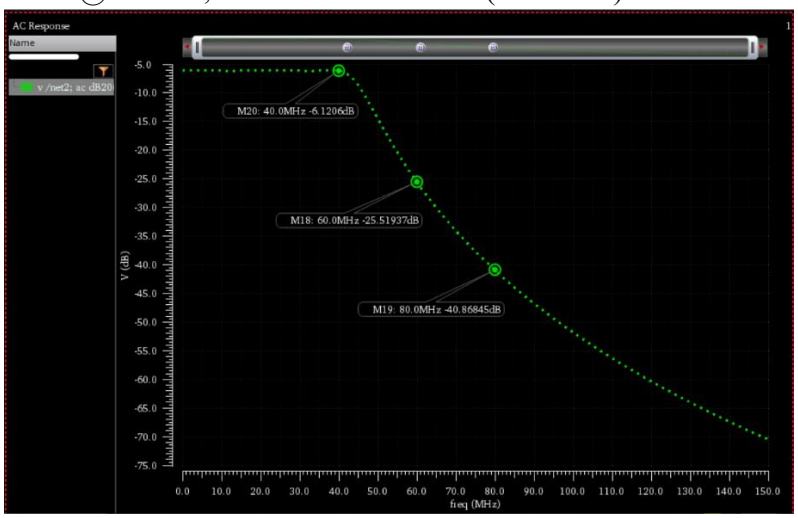

Figure 28: IR filter attenuation curve

Comparison and comment on calculated and simulated results

Parameters	Calculation	Simulation	Requirement
Power Gain (dB)	51	51.96	> 40
Noise Figure (dB)	7.81	8.65	< 10
IIP3 (dBm)	-12.88	-12.79 for if_I -12.58 for if_Q	> -18

Table 3 Calculated and Simulated result comparison

The total power gain simulated is similar to the calculated result. The simulated noise is larger than the calculated estimation, this may due to flicker noise at lower frequencies for dual conversion zero-IF2 transceiver architecture that was chosen; and thermal noise due to input and output port resistance, which was not considered in the calculation. For linearity, the simulated IIP3 is closed to the result of calculation, which the tuning of gain parameters at different cascaded stages of components had gone thru multiple iterations of PSS simulations. Although decreasing the gain of LNA1 can improve IIP3, small gain of early stage does major contribution to noise figure.

Problems encountered and solutions

- Filter topology selection: on-chip filters were chosen on our dual conversion IQ receiver. Simulation shows that noise figure is very high, and also using order of 4 do not meet the adjacent channel attenuation requirement. Off-chip filters with 5th order is chosen with buffers added (burns 27.7% more power as trade-off) to meet with the noise requirement. Also, the quadrature noise floor parameter need to be set to the same as phase noise setting, in order to solve the quadrature noise contribution.
- To meet with both IIP3 and NF requirements, gain of LNAs and buffers had gone through multiple runs of PSS simulations, which each runs of sweep take quite some time. The accuacy parameters of PSS simulations, for example, integration methods, steadyratio and maxperiods are tuned to speed up the simulation.
- IIP3 simulation has a lot of failure sweeps and the result does not converge at first, which the simulated curve is not smooth enough for analysis. Later setting IP2 the same as IP3 for both mixers solves the problem.

Conclusion

- A ideal Verilog A modeled dual-conversion zero-IF2 receiver is designed and simulated in this project. Voltage gain is 51.96dB, noise figure is 8.65dB and IIP3 of the IQ ports are -12.58 dBm and -12.79dBm.
- We have learnt the many trade-offs between gain, IIP3 and NF. Mainly NF and IIP3 due to their complementary behavior, since improving one would almost always result in the other reducing. Hence power had to be burnt to come to a compromise. Also, the fact that when it comes to NF, the components closest to the input affect it the most while for IIP3, it is the components closes to the output that affect it the most. Gain needed to be chosen carefully as well since it affects NF and IIP3 in opposite ways.

Contribution

- Lam King Sum Sam: Architecture design, hand calculation, Simulation, Tuning
- Tse Ming Fung Alfred: Simulation, report write up

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Reference

[1] Howard Luong, EESM5320 Lecture Notes

[2] Chendi Yu, "Cadence Virtuoso ic618 for Simulation of an LNA and an RX"

[3] Chendi Yu, "PSP Analysis for Receiver Gain Simulation"

[3] Virtuoso© SpectreRF Simulation OptionUser Guide

Appendix

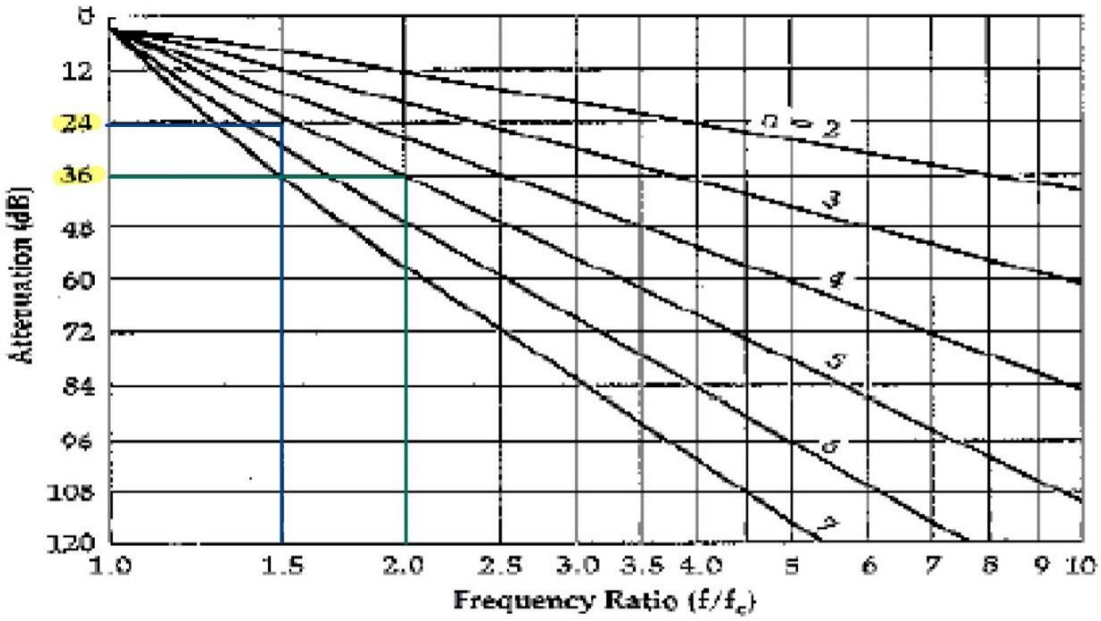

Figure 29: Characteristic curve of 0.1 dB ripple Chebyshev filter

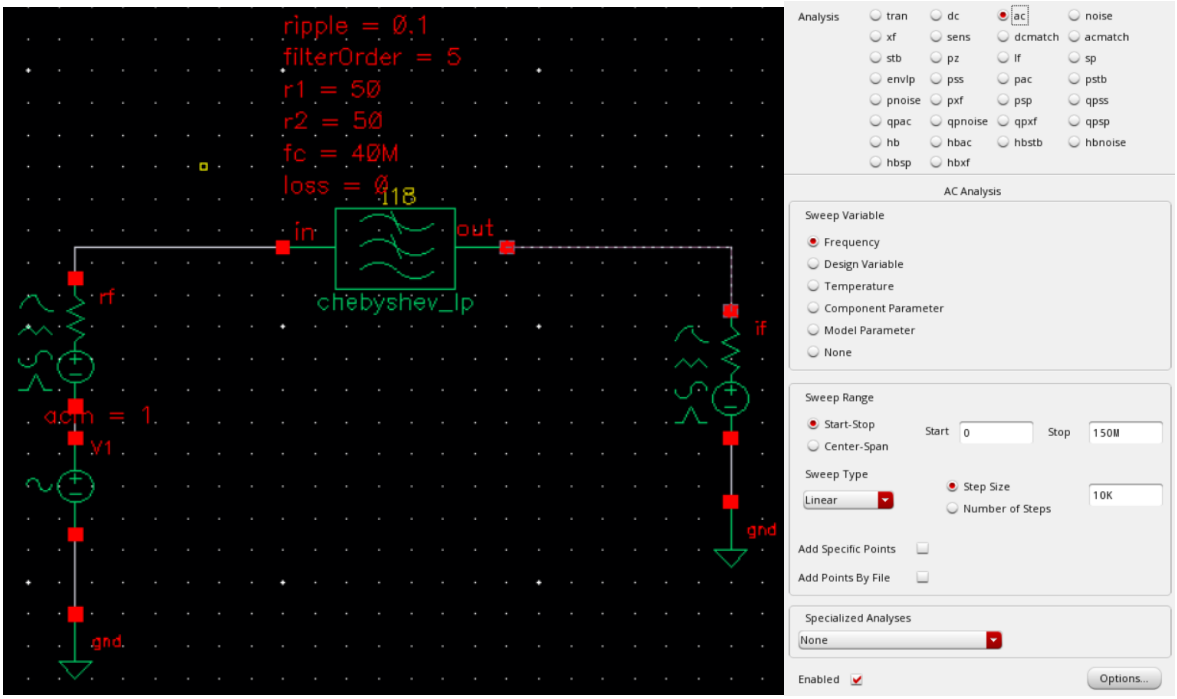

Figure 30: IR filter ac response schematic and simulation setup