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## Appendix A. A Brief Introduction to Logic Analysers

### THE BASIC NEED

An engineer with the task of designing, testing or fault finding digital electronic circuits faces a fundamental problem. How can he observe the operation of his circuit in detail? A conventional oscilloscope is of limited use since digital information tends to be continuously changing and therefore cannot be synchronised with the oscilloscope sweep. A storage oscilloscope allows the signal to be frozen, but its trigger function is inadequate to precisely define the point at which the data must be captured. In addition, with a two channel 'scope, only two signals can be looked at simultaneously which is inadequate for most digital circuit analysis. Logic probes and logic monitors are useful in checking whether signals are high, low or pulsing, but provide little information about how the signals are changing with respect to time.

The answer, of course, is a logic analyser. The logic analyser enables the activity of many digital signal points to be recorded simultaneously, and then examined in detail. The information is recorded with respect to a "clock" signal, and the analyser samples all the signal inputs on each active edge of the clock signal to determine whether they are high or low with respect to a defined threshold voltage. This information is stored in memory and is then available for detailed analysis via the logic analyser's display.

### TYPES OF DATA DISPLAY

There are three basic forms of display. A "timing diagram" is where a series of successive logic levels for each channel are displayed from left to right on a screen. This is similar to the way that an oscilloscope displays information since the trace represents the signals plotted against a time reference.

A "state display" is used to show the digital relationship between the various signals at each point in time. The analyser reads the logic levels for all the signals at each active clock edge and displays them as a "word". This word may be in binary, decimal, hex or ASCII or in a mixture of formats. The display then becomes a list of successive words. This method is particularly relevant to bus organised digital systems such as microprocessor based equipment, parallel data transmission systems, etc.

Many analysers provide the option of disassemblers for various types of microprocessor. By recording and analysing the buses and control signals of the uP, the logic analyser can decode the information into the appropriate mnemonics to describe the logical operations of the uP. Thus a "disassembly display" provides a list of mnemonics and operands specific to a particular uP.

### TRIGGERING THE ANALYSER

In order to define the section of data that is recorded, the logic analyser must be triggered. Triggering may be a simple change of level on a single line (as with triggering an oscilloscope) or it may be the simultaneous occurrence of a set of levels on a set of lines (e.g. triggering on a 16 bit word from a microprocessor address bus).

Most logic analysers provide the ability to define trigger words which include all of the input channels. More sophisticated analysers provide the ability to define a sequence of trigger words connected via logical statements (if-then-goto) to generate the trigger event.

Unlike an oscilloscope where the trigger event starts the sweep, in a logic analyser the trigger event stops the recording process, either immediately or after a defined number of clock cycles. This enables the analyser to capture data occurring before the trigger event as well as after it. Varying the delay changes the amount of pre-trigger and post-trigger data that is recorded.

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## **SYNCHRONOUS AND ASYNCHRONOUS RECORDING**

There are two basic ways of recording data (often called acquiring data). These are synchronous acquisition and asynchronous acquisition. In the synchronous mode, the clock signal for the analyser is supplied from the unit under test, and each piece of data is stored at a defined point; normally when the data is known to be stable.

In the asynchronous mode the clock signal is supplied from the analyser and is independent of the unit under test. Consequently the data may be stored at any point on the data waveform. If the analyser clock is set to be much faster than that of the data being stored, a timing diagram display will show a plot of data against time enabling the exact timing of level changes to be observed.

## **TRACE CONTROL AND DATA QUALIFICATION**

The recording of data into the memory can be controlled to prevent unwanted data from being recorded. For synchronous acquisition one way of achieving this is by "qualifying" the clock signal. Most analysers provide one or more clock qualifier and data is only recorded on a clock edge for which the qualifier input is "true".

Another way of controlling the recording is by means of a "trace" word. A trace word defines the condition for the data inputs which must be true for data to be recorded. Clearly if the trace word defined the condition for all of the data inputs then only the trace word would ever be recorded, so the trace word will normally define a condition for only a few of the data inputs. More sophisticated analysers often provide trace start and trace stop words. When a trace start word is encountered recording starts and when a trace stop word is encountered recording stops.

## **GLITCH CAPTURE**

Sometimes the sampling rate of the clock chosen to record data is too low to ensure that very short pulses are captured. Glitch capture allows pulses occurring between the sample points to be captured. A glitch is defined as two or more transitions of the signal between successive sample points.

Glitch capture provides no information on the width, position or number of pulses which occurred. Glitches are normally displayed on a timing diagram as narrow lines.

## **REFERENCE MEMORIES**

The memory into which the data is recorded is referred to as the acquisition memory. Most logic analysers also have one or more reference memories into which data can be transferred. The reference memory can be used for comparing new data with old or suspect data with known good data.

Logic analysers range from simple units with only eight data channels and 64 words of memory, a maximum clock speed of a few MHz, and limited trigger and display capability; up to highly complex units with 100 or more channels, acquisition speeds of several hundred MHz, very sophisticated trigger and display facilities, and a very large price tag.

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## Appendix B. Understanding the Aquisition Memory of the LA3200/4800

The Acquisition Memory has a total capacity of 8192 words which can be restricted to 1024 words. This is controlled by the Data Memory Depth option on the Configuration screen. In the following explanations a memory depth of 1K has been used, the figures that would apply to an 8K depth are given within brackets.

When an acquisition is started, the acquisition memory is first cleared so that all of the bits are low. The analyser then starts to write data into the memory in synchronism with the memory cycle clock (providing that the trace control conditions are True). Unless the acquisition is terminated beforehand (either by a trigger event or by the Stop key) the memory will fill with data after 1024 (8192) cycles. Once full, the first-in data is over-written by new data and this process continues until the acquisition is stopped.

Because an acquisition can last for any number of memory cycles, there is no fixed relationship between the position of a word in the memory and the hardware address of the high speed RAM which forms the memory. The relationship is defined after the acquisition is stopped. The RAM address at which the acquisition is stopped is normally defined as memory position 1024 (8192).

The acquisition can be stopped in one of two ways, by a trigger event or by pressing the stop key.

### 1. Acquisition stopped by a trigger event

When the trigger event occurs, the acquisition is stopped after a delay which depends upon the setting of the Trigger Position on the Trigger Setup screen. If the position is set to "Start of store" the delay is 1024 (8192) memory cycles. If the position is set to "Middle of store" the delay is 512 (4096) memory cycles. If the position is set to "End of store" the delay is zero.

Thus when the position is set to Start the acquisition will stop with the memory filled entirely with post-trigger data, when it is set to End it will be filled entirely with pre-trigger data, and when it is set to Middle it will be filled 50% with pre-trigger and 50% with post-trigger data.

The above statement assumes that either the Simple Trigger Setup screen is being used or that Step 5 in the trigger sequencer for the Complex Trigger Setup screen has the cycle counter set to 00000. This cycle counter provides a more complex control of the trigger position by adding an additional delay set by the user. For instance, if the position is set to End and the cycle counter is set to 00768 (06144), then the memory would contain 75% pre-trigger and 25% post-trigger data. The cycle counter can be set anywhere between 00000 and 24000 which enables the analyser to capture data that occurred a considerable time after the trigger event.

Note that if a trigger event occurs within a number of cycles from the start of the acquisition which is smaller than 1024 (8192) minus the total trigger delay setting, then the pre-trigger section of the memory will not be full when the acquisition is stopped and the early part of the memory will contain all low bits. To overcome this problem a Pre-Trigger Delay function is incorporated.

Pre-trigger delay is set On or Off from the Acquisition Control section of the Configuration screen. When set to On it prevents a trigger event from being recognised until 8192 memory cycles have occurred since the start of the acquisition. This ensures that the pre-trigger section of the memory is always filled with valid data.

### 2. Acquisition stopped by the Stop key

When an acquisition is terminated by the Stop key rather than by a trigger event there are two possible conditions. Either the analyser had not yet triggered or the analyser was triggered but the post trigger memory had not yet filled.

If the analyser had not yet triggered when the Stop key is pressed, then the analyser stops the acquisition immediately and defines that RAM address as position 1024 (8192). Thus the last data recorded is always placed at the end of memory.

If the analyser had triggered but the memory had not filled when the Stop key was pressed, then the analyser stops recording the input data immediately but continues the acquisition filling the remainder of the memory with 0s (low levels). Thus the data is positioned correctly relative to the trigger marker but the last data recorded will not be placed at the end of memory.