
THURLBY LA3200/4800

LOGIC ANALYSERS

SERVICE MANUAL

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Software

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Manual

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Section 1 - General

1.1. MAINS OPERATING VOLTAGE

Before connecting the instrument to the PC mains supply ensure that the AC line input voltage indicated on the rear panel is correct for the supply being used. If it is necessary to change the operating voltage, see section 3.3. Check that the AC mains supply frequency is in the range 48–63Hz.

1.1.1 Mains Lead

When a three core, mains lead with bare ends is provided this should be connected as follows:

BROWN	MAINS LIVE
BLUE	MAINS NEUTRAL
GREEN/YELLOW	EARTH

WARNING! THIS APPARATUS MUST BE EARTED

Any interruption of the protective conductor inside or outside the apparatus or disconnection of the protective earth terminal is likely to make the apparatus dangerous. Intentional interruption is prohibited.

1.1.2. Fuse

The mains supply fuse for the power supply is fitted in the mains supply socket. To change the fuse, disconnect from the mains supply and pull out the fuse cover situated below the input of the mains socket. Replace the fuse only with one of an identical type, see markings on rear panel and fuse.

1.2. SERVICE HANDLING RECAUTIONS

1.2.1. General

WARNING

The opening of covers or removal of parts is likely to expose live parts. The apparatus shall be disconnected from all voltage sources before any adjustment, replacement or maintenance and repair during which the apparatus shall be opened.

If afterwards, any adjustment, maintenance or repair of the opened apparatus under voltage is inevitable it shall be carried out only by a skilled person who is aware of the hazard involved.

1.2.2. Power Supply

Mains voltages are present on the input terminals of the mains transformer and the rear panel ON/OFF switch. The power supply should not be operated without a load.

1.2.3. LCD Unit

A voltage of approximately 1KV at 50kHz exists on the LCD power board which is fitted next to the LCD unit attached behind the main keyboard. Extreme care should be taken when handling the instrument near the LCD panel as contact could cause skin burns. Under no circumstances should attempts be made to service the LCD unit which is a proprietary display and should be returned complete to Thurlby-Thandar, or their agents overseas, for repair or replacement.

1.3. DISMANTLING THE INSTRUMENT

WARNING: READ THE SERVICE HANDLING PRECAUTIONS, SECTION 1.2. BEFORE ATTEMPTING TO DISMANTLE THE INSTRUMENT

1.3.1. General

The top cover is removed to gain access to the LCD unit, power supply, CPU and MAIN board (component side). To take off the top cover, move the handle to the vertical position so that the instrument is sitting on its 4 rubber feet, remove the 10 screws (5 on each side) which secure the cover, and, whilst pulling the bottom edges of the sides outwards, lift it clear of the instrument. Removal of the IEEE-488 board, if fitted, gives access to the component side of the CPU board; Removal of the CPU board gives access to the component side of the MAIN board; to gain access to the solder side of the MAIN board only, the IEE-488 board (if fitted) and CPU board can be left attached to the rear panel which can be removed intact.

1.3.2. GP500A IEEE-488 Board Removal

Remove the 7-way CPU board connector. The IEEE-488 board is released removing the pillar, secured to the IEEE-488 board, from the CPU board then removing the 2 screws securing the IEEE-488 board brackets to the panel. The board can then be lifted out.

1.3.3. CPU Board Removal

Remove the IEEE-488 board, if fitted (see 1.3.2.). Remove the 16-way keyboard connector PJ4, the 34-way LCD connector PJ5 and the 16-way CPU to MAIN board connectors PJ3. The CPU board is released by undoing the 2 screws securing the CPU board to the hexagonal posts on the MAIN board and the 2 screws securing the CPU board brackets to the rear panel. The board can then be lifted out.

1.3.4. MAIN Board Removal

It is not necessary to remove the IEEE-488 board (if fitted) and CPU board gain access to the MAIN board solder side, see section 1.3.1.

To remove the MAIN board disconnect the 6-way power connector PJ5 and close the latches on the front connectors, PJ1, PJ2, PJ3 and PJ4. Remove the 6 screws securing the board to the bottom framework and withdraw the MAIN board by simultaneously lifting and sliding the board backwards and upwards through the top of the instrument frame.

1.3.5. Front Moulding Removal

To remove the front moulding, unplug the 16-way keyboard connector and the 34-way display connector. Remove the 2 screws, one on either side, securing the front moulding to the side panel and the moulding can then be pulled outwards and away from the casing.

1.3.6. LCD Panel Removal

Remove the front moulding (see 1.3.5.) supporting the LCD panel, and lay with the rear of the LCD panel uppermost. Undo the 2 top retaining screws the 2 bottom bracket screws, disconnecting the ground lead attached to one the brackets. Lift the LCD panel slightly away from the front moulding support it so that the backlight tube can be removed slowly from the side the panel.

1.3.7. LCD Power Board Removal

Remove the front moulding (see 1.3.5.), and the LCD panel (see 1.3.6.) and the 2-way connector from the power supply. Remove the 3 screws securing the power board to the keyboard panel and withdraw the board.

1.3.8. Keyboard Removal

Remove the front moulding (see 1.3.5.), the LCD panel (see 1.3.6.) and the LCD power board (see 1.3.7.). Undo the 5 screws inside and along the bottom of the front moulding and withdraw the soft-key PCS support moulding. Remove the 5 screws securing the Main keyboard PCB and lift the two parts of the keyboard free.

1.3.9. Power Supply Transformer Removal

Disconnect the transformer wires which go to the main switch, noting their position and disconnect the 7-way connector to the power supply. Undo the 4 rear panel screws and remove the transformer.

1.3.10. Power Supply Removal

Disconnect the 7-way transformer connector, the 6-way MAIN board connector and the 2-way LCD power board connector. Remove the 2 rear panel screws securing the PSU PCB mounting pillars to the instrument frame and the 2 rear panel screws securing the PSU heat sink to the frame and carefully remove the PSU from the rear panel of the instrument.

Section 2 - Specification

2.1. Specifications

Number of data channels: 32 (48), 16 per connector

Number of clock inputs:

3 independent clocks, active edge can be independently selected for each. Data is stored on the OR of the three active clock edges.

Number of clock qualifiers: 3;

1 for each clock. Selectable as high, low or don't care.

Input characteristics:

Dependant upon the type of pods fitted. (See pod specifications).

Data Skew: Typically within +/-4ns.

2.2. MEMORY ORGANISATION

Data memory size:

32 (48) bits x 1K deep (normal mode) or

32 (48) bits x 8K deep (deep mode) or

8 (12) bits x 1K or 8K deep (high speed timing mode).

Reference memory size:

2 (4) non-volatile memories each of 32 (48) bits x 1K deep.

Data retention time 3 months typical.

Set-up memory:

Non-volatile storage for 10 set-ups.

Data retention time 3 months typical.

2.3. EXTERNAL CLOCK

Frequency range: DC to 25MHz.

Organisation:

3 independent clocks, individually qualified. Data is recorded on the logical OR of each active clock edge.

Data set-up and hold times: 15ns set-up; 0ns hold.

2.4. INTERNAL CLOCK

Clock rate:

Selectable 40ns to 100ms (25MHz to 10Hz) in 1:2:5 sequence (normal asynchronous modes). 10ns (100 MHz) in high speed timing mode (requires high speed data pods). 200ms and 1s (5Hz to 1Hz) in Roll mode.

2.5. GLITCH CAPTURE (Only available when high speed data pods are fitted)

Number of channels: 16 (24) (8 per pod) when in glitch mode.

Minimum detectable pulse: 5 nsec .

2.6. TRIGGERING

Trigger sequencer words: 4 words of up to 32 (48) bits

Trigger sequencer terms:

Each term can be the logical combination (including NOTs) of any number of the sequencer words.

Trigger sequencer steps:

Up to 4 steps with two comparisons and one redirection per step, e.g. for step N; IF event X occurs THEN GOTO step N+1, IF event Y occurs THEN GOTO STEP M. Event or clock counting on each step.

Trigger filter: 1 to 15 clock events. (1 to 14 extra clocks).

Trigger position:

Selectable between 100% pre-trigger, 50% pre-trigger/50% post-trigger and 100% post trigger plus up to 23,999 clocks of post-trigger delay.

Trace control:

Any trigger word can be used as a trace start word or a trace stop word allowing comprehensive qualification of the data stored.

Glitch Triggering:

Glitch words can be ANDed with normal trigger words.

2.7. TIMING DISPLAY

Number of channels:

Any 16 channels plus a timing scale (channels may be repeated).

Channel labelling:

Each channel can be uniquely labelled with up to 8 characters.

Number of samples:

For normal mode the full 1K memory depth can be displayed with an expansion of x1, x4, x16 or x64. For deep mode the full 8K memory depth can be displayed with an expansion of x1, x8, x32, x128 or x256. The expansion window can be moved anywhere in the store. The position of the window is shown graphically on the display.

Cursor system:

There are two moveable cursors and a fixed trigger marker. The display shows the absolute and relative position of each within the store along with the data value at the reference cursor. A window into the state display showing the state of all the channels at the reference cursor position is also shown.

Glitch display: Glitches are displayed as narrow vertical lines.

State information:

The state of all 32 (48) channels at the reference cursor position is displayed in the format as set within the State Display system.

Roll mode operation:

Timing diagram is updated continuously as acquisition takes place when using very slow clock rates (5Hz and 1Hz).

Analogue Display Mode (LA4800 only):

8 channels can be displayed as the analogue equivalent of an 8-bit binary word. 8 further channels can be displayed in conventional mode simultaneously.

2.8. STATE DISPLAY

Channel groups:

Up to eight groups can be defined. Each group can be given a user defined name. Each group can contain up to 16 channels. Channels can be randomly positioned. Channels can be repeated in different groups.

Display format:

Each individual group can be displayed in its own radix selected from binary, ASCII, octal, decimal, hex, or ASCII. Each group is displayed under its own defined label.

16 consecutive store locations can be selected from the selected memory (main or reference) and scrolled up and down. The start line can also be selected directly from the keyboard.

2.9 SEARCH AND COMPARE

Word Search:

An individual word can be searched for in any memory. A mask can be specified.

Block Search:

A block of any length and any position can be searched for in any memory. A mask can be specified and a filter can be set.

Page Compare:

The current page can be compared with the same page in another memory. Differences are displayed in reverse video.

Block Compare:

A block of any length and any position can be compared with a block of similar length any position within any memory. A mask can be specified and a filter can be set.

Conditional Repeat:

During data acquisition, the block compare function can be operated automatically. The acquisition can be stopped on either equality or an inequality.

Mask and Filter:

A mask specifies which parts of the data are to be defaulted to don't care for the purposes of a search or a comparison. A filter specifies an allowable number of non-matching words that can exist between matching words. It is particularly useful in compensating for data position skew in asynchronous data capture.

2.10. SIGNATURE ANALYSIS (LA4800 only)

Compression of data into unique 4 digit Hex signatures using a multiple feedback path shift register algorithm. The data can be from a single channel or a group of channels. Data can be from any section of any memory.

Signatures can be used for rapid go, no-go testing against prepared documentation.

2.11. PERFORMANCE ANALYSIS (LA4800 only)

Performance analysis provides statistical information for a group of 16 channels (normally a microprocessor address bus). A histogram is generated showing the percentage of the time for which the address was within a number of user defined address ranges.

2.12. DISPLAY

9" supertwist blue mode LCD with cold cathode fluorescent back lighting. 80 columns by 25 lines in text mode, 640 by 200 pixels in graphics mode.

2.13. INTERFACE OUTPUTS

Data input/output:

RS-423 serial interface standard (RS-232 compatible), IEEE-488 interface optional Output to a printer via the serial interface, optional serial to Centronics parallel interface cable available.

Trigger interface: Outputs for the following signals : Triggered, word A True, word B True, Memory clock. Inputs for the following: Disable sequencer goto, disable event Clock counting.

2.14. POWER

110V ~10%, 120V ~10%, 220V ~10%, 240V ~10%, 48 - 63Hz, 75VA max.

2.15. MECHANICAL

Size - 315 x 190 x 268mm (12.4 x 7.5 x 10.5").

Weight - 5kg (11 lb).

2.16. ENVIRONMENTAL

Temperature - -20C to +60C storage, 0C to 40C operating.

Humidity - 20% to 80%. (non condensing).

2.17. OPTIONAL DATA PODS

Combination data pod AP01:

Single pod with 32 data inputs (DC to 25MHz) 3 clock inputs, 3 clock qualifier inputs. Single 40-way connector with colour coded plug-in connection leads.

Input impedance: 100k/10pF.

Threshold: TTL (+1.4V).

Max. input volts: +10V/-5V.

Combination data pod AP02:

Single pod with 48 data inputs (DC to 25MHz), 3 clock inputs, 3 clock qualifier inputs.

40-way and 24 way connectors with colour coded connection leads.

Input impedance: 100k/10pF.

Threshold: TTL (+1.4V).

Max. input volts: +10V/-5V.

High Speed data pods AP03:

16 channels at DC to 25MHz, 8 channels at DC to 25MHz with glitch capture, 4 channels at 100MHz (asynchronous only).

Colour coded plug-on connection leads.

Input impedance: 100k/6pf.

Threshold: TTL (+1.4V).

Max. input volts: +10V/-5V.

Min. pulse width (Glitch mode): 5ns.

Clock pod AP04:

3 clock inputs, 3 clock qualifier inputs.

Colour coded plug-on connection leads

Input impedance: 100k/6pf.

Threshold: TTL (+1.4V).

Max. input volts: +10V/-5V.

High Speed variable threshold data pods AP03V:

16 channels at DC to 25MHz, 8 channels at DC to 25MHz with glitch capture, 4 channels at 100MHz (asynchronous only).

Colour coded plug-on leads.

Input impedance: 100k/6pf.

Threshold: variable -5V to +10V in 0.1V steps.

Hysteresis: typically =200mV.

Min. input overdrive: =50mV above hysteresis level.

Max. input volts: =50V.

Min. pulse width (Glitch mode): 5ns.

Variable threshold clock pod AP04V:

3 clock inputs, 3 clock qualifier inputs.

Colour coded leads.

Input impedance: 100k/6pf.

Threshold: variable -5V to +10V in 0.1V steps.

Hysteresis: typically +/-200mV.

Min. input overdrive: =50mV above hysteresis level.

Max. input volts: +/-50V.

2.18. OTHER OPTIONS

Microprocessor disassembler pods:

Disassembler pods are available for many popular 8 bit and 16 bit microprocessors. Each pod has the disassembler firmware incorporated within test clip and is supplied complete with a test clip connector for connection to the target microprocessor.

Serial to parallel printer cable PC01:

This cable enables the logic analyser to be used with printers which have a Centronics parallel input.

IEEE-488 interface GP500a:

This option enables data to be sent to and from the logic analyser using the IEEE-488 bus (GPIB) instead of RS-232.

Software interface for IBM-PC compatible computers LATALK:

Disk based software which will operate on most IBM compatible personal computers. The computer is linked to the serial interface of the logic analyser by a cable which is supplied. The software allows remote control of the analyser, disk storage of acquisition data, disk storage of set-up data etc.

Section 3 – Circuit Description

3.1. GENERAL

Throughout the circuit descriptions, the following conventions apply:-

1. Bold type indicates a signal name shown on the relevant circuit diagram in section 5.
2. A signal name followed by bar indicates a 'bar' signal on the circuit diagram.

Approximate circuit diagram 'grid references' are given at the each sub-section.

3.2. LCD

The LCD is a proprietary unit which should be returned complete to Thurlby Thandar, or their agents overseas, should a fault develop. Since there are no field-serviceable parts in this assembly, only connections and adjustments (see 3.3) are given.

Refer to sections 1.2 and 1.3 for Handling Precautions and removal of the LCD from the instrument. All connections to the LCD are via the connector PJ5 on the CPU board and PJ3 on the Power Supply Board.

3.3. POWER SUPPLY

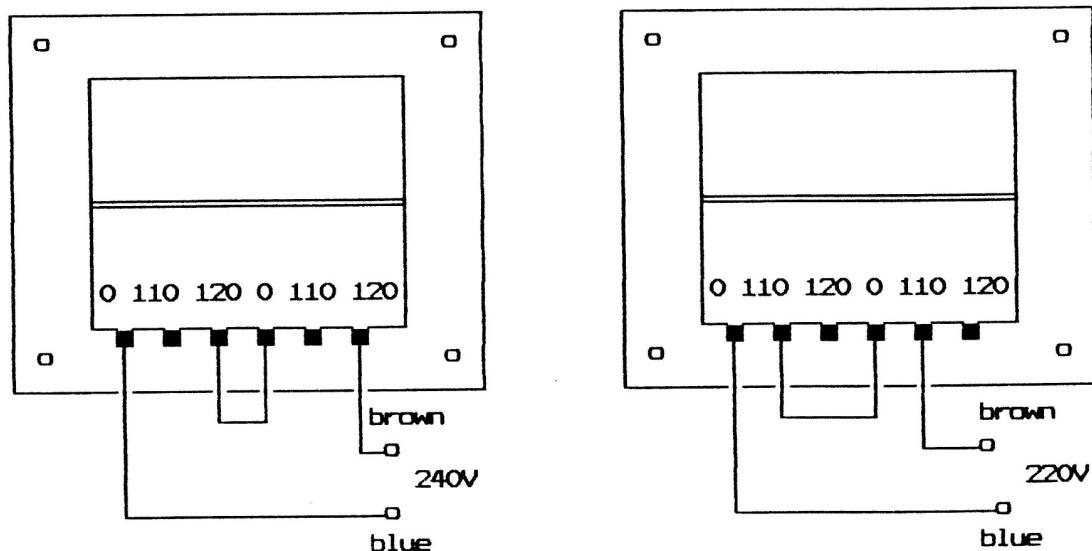
Refer to sections 1.2 and 1.3 for Handling Precautions and removal of the power supply from the instrument.

DO NOT OPERATE THE PSU WITHOUT A LOAD

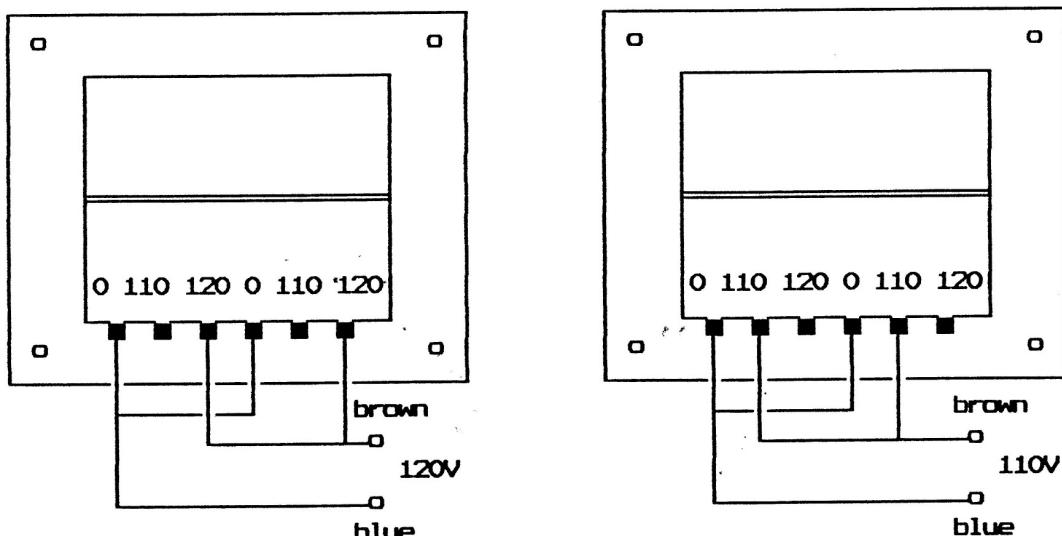
3.3.1 Mains Connections

The set operating voltage of the instrument is shown on the rear panel label. Should it be necessary to alter the operating voltage change the transformer connections following the appropriate diagram below.

240V and 220V Operation: Primaries in series



120V and 110V Operation: Primaries in parallel



If a change is made, the operating voltage label should also be changed.

3.3.2. Operation

ref. fig 11

The principal secondary winding is bridge rectified by BR1 and regulated by IC1-C, Q1, Q3 and voltage reference ZD1 to provide the main 5V 2.5A supply to the analyser. PR1 is factory preset for 5.1V output. IC1-D output goes low to reset the analyser whenever the regulator output is more than 250 mV below its set value.

Another positive regulator IC1-A, Q2, Q4, powered from the same winding, provides up to 1Amp at an output voltage between 2 and 4.5V set by VR1 to the inverter which powers the fluorescent back light for the LCD display. VR1 is provided as a rear panel adjustment for the LCD brightness control.

IC1-B provides a fold back action to limit the total current taken by the positive regulators to about 3.8Amp.

IC2 is fed from a separate secondary winding and provides a -5V rail.

IC3 is also fed from an independent secondary and is set to deliver approximately -23V by adjustment of PR2 directly after switch on. The -23V rail, **VLCD**, is fed to the main board where it becomes the LCD contrast control voltage. Thermistor TH1 causes the magnitude of this voltage to decrease by about 0.3 percent per deg C to stabilise the contrast of the LCD display.

PSUON is generated when the +5v rail rises and is used on the main board CPU board as a system reset line.

3.3.3. Service Adjustment

Nominal Voltage	Permissible Range
+5V	Adjust to +5.1V (PR1)
-23V	Adjust to -23V (PR2)

3.3.4. Power Supply PCB Signal Directory

PSUON	Power supply ON control line for system reset
VLCD	-23V supply line to LCD
+5V	5 volt supply rail
2- 4.5V	LCD brightness voltage
0V	Ground rail

3.4. CPU BOARD

3.4.1. General

The CPU board is a single board computer using a 6303X CPU running at 8MHz. The board contains 64K of non-volatile RAM, 32K of system RAM and 64K of system EPROM. The LCD screen generation is based on the M6255 LCD controller which is programmed to produce 24 lines by 80 characters of 7 by 7 pixels in text mode and 640 by 200 pixels in graphics mode. The CPU board also contains the circuitry for the keyboard and RS-423 interfaces. The CPU board interfaces with the MAIN board via a 16-way connection.

3.4.2. Reset Circuit

ref. fig 1, 5,6/A-C

Q3 and Q4 and associated discrete components provide a power-on and a power-down reset. When the +5V rail rises Q4 will be OFF until PSUDN rises and turns Q3 ON via RP4-D. The collector of Q3 is pulled LOW which then turns Q4 ON via RP4-C. When Q4 turns ON its collector output, **RESET bar** will go HIGH.

When the +5V rail falls below 4.8V, the switch off point is set by components on the PSU board (see 3.3.2.), PSUON will go LOW which will turn OFF Q3. This will also turn OFF Q4 which will pull the **RESET bar** line LOW. The power-down reset ensures the Non-volatile RAMs are not erroneously written to while the +5V rail is falling.

3.4.3. Clock

ref. fig 1, 1/C,D

The CPU board timing is derived from the 8MHz oscillator consisting of XTAL1, C5 and C6. IC17-8 is used to produce LCDCLK ANDing the CPU clock with **SCLK**. The CPU interface clock, **ECLK**, is an output line from the CPU and used by IC17-D to produce **ECLK bar**.

3.4.4. Data and Address Bus.

ref. fig 1,2,3/C,D

The CPU data bus, **D0-D7**, connects directly to the CPU EPROM and RAM positions, LCD controller, IC2, RS423 controller, IC3, and, via a transceiver IC10, to the LCD RAM.

The CPU address bus, **A0-A15**, connects directly to the CPU EPROM and RAM positions and LCD controller and memory decoders IC7, IC8 and IC15.

3.4.5. Memory Organisation and Selection

ref. fig 1, 4/A-C

Addresses ranging from 0000H to 001FH are assigned by the CPU as registers. Addresses from 0020H to 003FH are assigned by the CPU as memory and are used for addressing the ACIA, IC3, at address 0020H, and the LCD controller, IC2, at address 0030H. Addresses ranging from 0040H to 00F0H are assigned by the CPU as internal page zero memory locations

IC8 decodes the upper eight address lines, **A8-A15**, so that the bottom

256 bytes of memory are reserved, by pulling the enable line, **PAGE0 bar**, HIGH when all eight address lines are LOW to enable addressing of IC3 and IC2 at addresses 20H and 30H, using **ACIASEL bar** and **LCDSEL bar** respectively, and correct addressing of the CPU page zero locations. IC15 is disabled above address 0100H as a HIGH on any input to IC8 will result in the output, **PAGE0 bar** being LOW to enable IC7.

Addresses ranging from 0100H to 3FFFH are assigned to both 16K pages of non-volatile 32K RAM, IC6, which is selected when the outputs from IC7 pin 11 or pin 15 are LOW which in turn pulls the output from IC14-A LOW. This along with **PAGE0 bar**, to IC13-B whose output drives Q7. Q7 can only be ON when the **RESET bar** line is driven HIGH through RP5-D so that access by **CS2 bar** going LOW, is only possible when **RESET bar** is HIGH.

Addresses ranging from 4000H to 7FFFH are assigned to the lower half of 32K RAM, IC5, which contains part of the disassembler code when loaded both 16K pages of the 32K non-volatile LCD RAM, IC9. The lower half of IC5 selected when the output from IC7 pin 14 goes LOW so pulling **CS3 bar** through IC14-D. IC9 is permanently selected whilst the **RESET bar** line is HIGH through RP5-8 which turns Q6 ON to pull **CS4 bar** LOW.

Addresses ranging from 8000H to 8FFFH are assigned to the upper 16K page of the 32K RAM, IC5, which contains the remainder of the disassembler code when loaded and the first and third 16K quarters of the 64K ROM, IC4. The upper half of IC5 is selected when the output from IC7 pin 13 goes LOW so pulling **CS3 bar** LOW through IC14-D. IC4 is selected when the outputs from IC7 pin 12 and pin 7 go LOW so pulling **CS1 bar** LOW through IC14-C via IC14-8.

Addresses ranging from C000H to FFFFH are assigned to the second and fourth 16K pages of the 64K ROM, IC4, which contains the 6303 root program. The upper half of IC4 is selected when the output from IC7 pin 9 bar LOW so pulling **CS1 bar** LOW through IC14-C.

3.4.6. EPROM and RAM Overlay Selection

ref. fig 1, 2,3/C

The lower 32K of IC4 is paged in over the upper 32K when the CPU port line **PAGEROM** is LOW. When **PAGERAM** is HIGH the upper 16K of IC6 is paged over the lower 16K, when LOW the lower 16K of IC9 is paged over the upper 16K. When **PAGEDIS** is LOW the lower half of IC5 is paged in over the top half of IC9 and the upper half is paged in over the third quarter of IC4.

3.4.7. Non-volatile RAM Supply Rail

ref. fig 1, 5/8,C

The Non-volatile RAM supply rail (+5A) is switched between the system +5V rail and the 2.5V Nicad battery, BAT1. When **PSUON** goes HIGH it turns on Q3 whose collector is pulled LOW which turns ON Q5 via RP5-A and holds Q5 in saturation while the **PSUON** is HIGH. When **PSUON** goes LOW Q3 is turned OFF which turns OFF Q5 so switching the non-volatile RAM supply to standby voltage from **BAT1**. R12 defines the re-charge current for **BAT1** and C7 decouples **+5VA**.

3.4.8. LCD Controller and Display RAM

ref. fig 1, 2-4/E-H

The LCD controller, IC2, is set to work in graphics mode with 640 x 200 dots. The controller is clocked by **LCDCLK**, generated from the ANDed version of the 8MHz CPU clock and **SCLK**, which is a CPU output pulled HIGH to synchronise the LCD controller to RAM accessing. IC2 is chip selected by **LCDSEL bar**, see 3.4.5.

The Display RAM, IC9, is loaded by pulling **D_{IEN}** LOW which outputs A0 to A14 onto **MA0 - MA14**. Display data is put onto the data bus, **D0-D7**, through the display buffer, IC10. **LCDRAM bar**, see 3.4.5., is pulled LOW to enable the data onto the display data bus, **RDO-RD7**. The display RAM is then written to when to **WR bar** goes LOW through IC13-C and **CS4 bar** is driven LOW. To read from the display RAM the same procedure is used except that RD bar switches the display buffer, IC10, to transfer data out.

Screen updating is carried out by the LCD controller which outputs the display data as 4 parallel bits, **UD0-UD3**, which are latched by the display using **LIP**, the display data latch signal, and shifted through its own shift registers using **CLP**, the display data shift clock, until all 640 bits of row information have been sent. This process is continued for all 200 rows to produce a display of 80 x 200 bytes which is stored in half of IC9, the remaining half of IC9 being used by the CPU for non-volatile data storage. Although the display is set to graphics mode it has the potential to display 80 characters per row by 25 rows.

FRMB and **FRP** are used to reset the frame controller back to the first display row.

VLCD is the LCD supply rail and **VLCDCON** is the variable rail which controls the LCD contrast.

3.4.9. LCD Contrast Control

ref. fig 1, 5/A

The variable voltage output, **VLCDCON**, and -23V rail, **VLCD**, from the MAIN board are passed from PJ3 to the LCD connector, PJ5, from where they are passed to the LCD board and used for contrast central.

3.4.10. Keyboard Interface

ref. fig 1, 2,3/A-C

The keyboard interface comprises all of the CPU port 5 outputs and six inputs of port 6. Port 5 outputs to the keyboard connector, PJ4, are all pulled HIGH by the resistors RP1-A to RPI-H. The two ports form a 48 way matrix using 35 junctions. The keyboard is polled during a timer interrupt by walking a zero across the outputs of port 5 while simultaneously reading the data on port 6. A LOW, therefore, on any input indicates a key is depressed which is then decoded by the CPU depending on the output from port 5.

Diodes, D1 to D6, are used to isolate input lines from output lines to stop a short circuit situation. The system software is responsible for debouncing the keyboard.

3.4.11. RS-423 and IEEE-488 Interface

ref. fig 1, 5,6/D-F

The RS-423 interface consists of IC3, an ACIA, IC12 and associated components. IC3 is chip selected using **ACIASEL bar**, **A0**, see 3.4.5., and sends and receives data via the CPU data bus, see 3.4.4., using **WR bar** to select the direction. The CPU **ECLK** is used as the device clock and the CPU timer output. **T/RCLK** is the transmit and receive clock.

The RS-423 consists of IC12, Q1, Q2 and associated resistors. The TXD and outputs from IC3 are buffered and inverted by IC12 and then passed out to interface, PJ1, as **TXD** and **CTS bar**. The two input lines, RXD and **CTS bar** are buffered and inverted by Q2 and Q1 respectively after passing through series resistors for overload protection. The RS-423 interface provides +5V and -5V via series resistors for overload protection as well as 0V.

The IEEE-488 connector, PJ2, receives serial data directly from IC3 and the four serial lines, TXD, RXD, CTS bar and RTS bar, connect to the board via 7-way flat cable from PJ2.

3.4.12. CPU to MAIN Board Interface

ref. fig 1, 5/A

The CPU board connects to the MAIN board via 16-way flat cable from PJ3. The interface consists of the CPU signals, **TX** and **RX**, **VLCDR** and **VLCDCON** and the power rails, +5V -5V and 0V.

TX and RX are the serial interface lines used by the CPU to send and receive control information and data to and from the MAIN board. The RS232 function is controlled internally by the on-board serial controllers in the CPU's on the MAIN board and the CPU board.

3.4.13. CPU PCB Signal Directory

ACIASEL bar	Chip select for the ACIA
A0 - A15	CPU address bus
CLP	LCD controller display data shift clock
CS1 bar	IC4 ROM chip select line
CS2 bar	IC6 non-volatile RAM chip select line
CS3 bar	IC5 RAM chip select line
CS4 bar	IC9 non-volatile display RAM chip
CTS bar	clear to send control line
D0-D7	CPU data bus
ECLK	CPU E clock output
ECLK bar	Inverted version of ECLK
FRP	LCD controller display frame signal
FRMB	LCD controller display frame start signal
LDCLK	LCD controller clock
LCDRAM bar	Chip select line for the LCD controller RAM
LCDSEL bar	Chip select line for the LCD controller
LIP	LCD controller display data latch signal
MA0 - MA14	LCD controller RAM address bus
PAGEDIS	CPU output to disable selecting page ROM
PAGERAM	Chip select line for the page RAM
PAGE0	Control line to enable CPU page zero
PAGE0 bar	Control line to disable chip select when page zero
PSUON	Power supply ON control line for system reset
RD bar	CPU read control line
RD0 - RD7	LCD controller RAM data bus
RESET bar	CPU Board reset line
RTS bar	RS423 and IEEE-488 ready to send control line
RX	CPU data receive line from MAIN board
RXD	CPU data receive line from IEEE-488 and RS423
SCLK	CPU serial clock for serial acquisition setup data
SCLKIW	CPU serial clock input
TX	CPU data transmit line to MAIN board
TXD	CPU data transmit line to IEEE-488 and RS423
T/RCLK	Transmit/receive clock for RS423 interface
UD0 - UD3	LCD controller 4 bit parallel data bus
VLCD	Supply line to LCD
VLCDON	Variable supply line to LCD to adjust contrast
WR bar	CPU write control line
+5V	+5 Volt supply rail
+5VA	Battery supply rail
-5V	-5 Volt supply rail

3.5. MAIN BOARD

3.5.1. General

The MAIN board connects directly to the input pods. The MAIN board microprocessor interfaces with the CPU board via a 16-way cable and contains all the acquisition circuitry of the analyser. The MAIN board is controlled by its own 6303 CPU which receives set up information from the master 6303 on the CPU board and sends back acquisition data on request. Prior to an acquisition the CPU board sends the current acquisition parameters including clock selection, filter count, trigger words and sequence information to the MAIN board CPU. During the acquisition the CPU monitors the acquisition status and when the acquisition completes it reads the acquisition data.

An acquisition is initiated by resetting the MAIN board and then driving **GO bar** line LOW; it is terminated by the **STOPPED** line or the **GO bar** line from the CPU being driven HIGH, which prevents further clocks entering.

3.5.2. Clock Inputs and Qualification

ref. fig 3, 5,6/A-C

The three clock input circuits are identical in operation so the circuit for **CLK1** and qualifier **QUAL1** only is described.

The clock signal from the pod, CLK1, passes through series resistor RP7-A and into IC64-A. Clock edge selection is achieved using the output **CLPOL1** from IC57 which is set HIGH for a positive edge clock and LOW for a negative edge clock. The signal is then passed through the analogue gate IC67-B. A HIGH on **CSEL1** out of IC58 will enable the specified clock whilst a LOW will disable the clock. This allows for the selection of either or no clock edge.

The clock qualifier signal from the pod, **QUAL1**, passes through series resistor RP7-B and is selected by **QPOL1** from IC57, and **QSEL1** from IC58 into IC67-C in the same way as CLK1 and passes as a HIGH to the data input of IC59-A.

When a clock is received the clock input to the latch IC59-A, which has a pull up resistor, RP6-A, to hold the line high when de-selected, goes HIGH and, if **QUAL1**, which is the data input to IC59-A, is TRUE then the output of the latch goes HIGH. This signal is fed back through inverter IC62-C and integrated by R4 and C9 to generate a LOW going pulse, with the loop delay determining the clock pulse LOW width, to reset IC59-A which generates a negative going clock pulse into IC61-A and IC61-B and IC74-A.

When an acquisition is started the inputs to IC63-B are both LOW making **STPCLK bar** HIGH with **CL1**, **CL2** and **CL3** sitting HIGH. When a clock is received **CL1** will pulse LOW so generating a HIGH pulse on **PODCLK**, **CLK1A** and **CLKA**. **PODCLK** is a clock signal passed back to the High Speed pods to be used for 100MHz internal clock operation and for glitch capture, see 3.6.6.2.

CLKA is further delayed through IC63-C, R29 and IC63-D to produce CLKB which is further delayed through R30 and inverted through IC62-B and enabled through IC68-C by **STPCLK bar** being HIGH to generate the RAM write pulse, **ACQWR bar**.

CLKA is also passed through IC68-A and IC68-D in parallel when **PROCWR bar** is HIGH to generate **CLKC**. R8 defines the DC voltage and R34 is a pull up to speed up the positive edge of **CLKC**.

3.5.3. Internal Clock Generation

ref. fig 3, 3,4/A-C

The 25MHz clock is generated using from the oscillator comprising IC69-F, XL2 and associated components. The 20MHz clock is generated using from the oscillator comprising IC69-E, XL3 and associated components. The 100MHz clock is generated inside the AP03 pod from the 25MHz clock, see section 3.6.6.3.

All other internal clocks down to 2MHz are generated from the 20MHz clock using the decade counter IC54-A connected as divide by 2 to produce 10MHz from pin 3 and as a divide by 10 to produce 2MHz from pin 7. The 5MHz clock is produced from pin 13 of IC54-B connected as a divide by 2. The remaining clocks are produced by the CPU internal timer 3 with its output, **SLOWCLK**, passing directly to the multiplexer.

All clocks are selected through the eight input multiplexer, IC55, which the required output selected using the PB5, PB6 and PB7 outputs from the PIA, IC51, to produce **INTCLK**.

EXTCLKIN from PJ7 pin 7 on the rear Panel is buffered through IC33-F passed to the multiplexer but is not software selectable in the same way as the other clocks.

The internal clock is selected by turning off all the external clocks and qualifier inputs using the **CSEL** and **QSEL** outputs from IC58 to open circuit the analogue gates. The **CSEL1** line going LOW is inverted and passed to IC67-A which allows **INTCLK** through to the clock input of IC59-A to generate **PODCLK**, **CLK1A** and **CLKA** as before.

3.5.4. Clock GO bar Line

ref. fig 3, 5/D,E

The **GO bar** signal is a CPU output into IC63-B. After **ARESET** is pulsed HIGH to reset the MAIN board, the **GO bar** line is set LOW to initiate an acquisition allowing the clocks through IC61-A, IC61-B and IC74-B. The acquisition can be stopped by the CPU pulling the **GO bar** line HIGH and stopping the clocks.

3.5.5. Glitch Capture

Glitch capture is provided on data channels **A8 to A15**, **B8 to B15** and **C8 to C15** with the remaining channels used for data inputs.

In Glitch mode only eight channels in each pod are used. The pod separates data and glitch channels for separate display and triggering into eight channels of each.

3.5.6. Pod Connections and Control Signals

ref. fig 3, 2/A,B & fig 2, 2-6,A

Neither the AP01 nor the AP02 pod uses any control information from the analyser only the power rails to supply power to the pod, see section 3.6. The control lines **PODSEL1** and **PODSEL2** from IC57 are used by both AP03 and AP04 pods to turn the glitch capture in the pods on and off. VREF is used by the AP04 pod to produce the variable threshold levels. VREF is varied by programming the outputs from the CPU internal timers, **TOUT1** and **TOUT2**. These outputs are XOR'ed by IC65-C and the output is integrated using C12 and R12 to produce a steady reference voltage for the pods. The capacitors C13 to C15, C23 to C25 and C33 to C35 are used to decouple the control lines in the pods.

3.5.7. Data Receivers and Latches

ref. fig 2, 2-6/B-D

As data input **D0** from pod input A is typical it will be described representative of all inputs.

D0 passes through series resistor RP1-A and is received by IC5-A. It is buffered and inverted to become **BDO** which passes to the primary latch, IC6. When valid **BDO** is latched by **CLK1A** in IC6 and its output, **LDO**, passes to latch IC7. When the next clock is generated **CLKC** latches **LDO** in IC7 whose output feeds the data acquisition ram, IC11.

3.5.8. Address Counters and Acquisition RAMs

ref. fig 2, 1/C-F & 2-6/E

Four binary counters, IC1 to IC4, are cascaded to provide an 11 or 13 bit resettable address counter. The counters are reset by **ARESET bar** and clocked by **TRACECLK**. The counter addresses the 8K x 8 bit acquisition RAMs IC11 and IC12, IC111 and IC112 and IC211 and IC212 and can use 11 address lines when using 1K storage mode or 13 address lines when in 8K storage mode. The control line **2K/8KSEL bar** from the CPU is used via IC56-C and IC56-D to switch the two extra lines in or out by being driven HIGH to pull **RA11** and **RA12** LOW.

The acquisition RAMs are written to at a maximum speed of 25MHz using **ACQWR bar** which is generated when storage is turned ON. All RAMs are permanently enabled by tying their CE1 inputs LOW and their CE2 inputs HIGH. The CPU reads the RAMs by disabling the data latches, by driving **RAMBUFEN bar** HIGH, and enabling the RAMs outputs, by driving **ARAMRD bar** LOW. The data is read out via buffer IC13 using the data bus **DH0** to **DH7** and the buffer output enable **RAMRD1**. The address counters are reset and, if the first data sample is not at location zero, the CPU board generates the required number of clocks to advance the counters to that point. The CPU board then reads all six RAMs and then pulls **PROCCLK bar** LOW which passes into IC60-B to set the flip-flop. The output is inverted by IC62-A and integrated by R19 and C17 to pulse the reset line to produce a pulse on **TRACECLK** which increments the counters so that the next RAM location can be read. This is repeated for RAM locations.

3.5.9. Recognition RAMs

ref. fig 2, 1-6/H

The recognition RAMs, IC18 to IC21, IC118 to IC121 and IC218 to IC221 are programmed prior to every acquisition. The CPU drives **I/PLATCHEN bar** HIGH, to disable the input latches, which drives **TRGLATCHEN bar** LOW to enable and latch the data from **DH0** to **DH7**, from IC51, onto the **A0** to **A3** lines of the recognition RAMs to select the ram address to write to. **DH0** to **DH7** are then set up through IC51 with the recognition RAM data on the **D1** to **D4** inputs. The CPU then writes to the PIA, IC51, to select IC52 and using the **WREN bar** line generates a LOW going write enable pulse, **TWR1 bar**, to write to the RAMs in pairs. This is repeated for all RAM locations. **I/PLATCHEN bar** is pulled LOW ready for the next acquisition.

The RAMs are programmed so that output 01 is active HIGH when <WORD 1> is recognised, 02 for <WORD 2> etc. The corresponding outputs of all twelve RAMs, **WORDA** to **WORDD**, are ANDed together with pull up resistors R25 to R28 and XORed with the outputs from the shift register IC46, **Z4** to **Z7**, to produce the enabled trigger word outputs, **TRGA** to **TRGD** which go HIGH if recognised. **WORDA** to **WORDD** are available for test purposes on PJ8 pins 1, 3, 4 and 2 respectively. **TRGA** and **TRGB** are available on the rear panel through IC33-A and IC33-B and PJ7 pins 11 and 12 as **TRIGA bar** and **TRIGB bar** respectively.

Z4 to **Z7** are used to determine the polarity of the trigger words set in each sequence step so that they are set LOW to select a NOT trigger word.

3.5.10. Trigger Word Filter

ref. fig 3, 1,2/E,F & 3,4/E

When the filter is ON, the four counters, IC24 to IC27, are all loaded with the filter count using the outputs from shift register IC46, **Z0** to **Z3**, which are set up for whole acquisition.

3.5.11. Event Trigger Filter,

ref. fig 3, 1,2/D;E

The event trigger filter consists of IC22, IC30, IC71-B and IC24. The 4 x 4 register, IC22, is loaded using write address lines, **WS0** and **WS1**, and, after setting up the data on lines **DH0** to **DH3**, using the write enable line, **TWR7 bar**, to write the data into the register. The outputs from the register determine which trigger words are set up in each sequence step by holding the input to the OR gate, IC30, LOW when selected. When a trigger word is recognised the outputs, **TRGA** to **TRGD**, are also passed into the IC30 to generate a HIGH output into IC71-B. When all selected trigger words are recognised and all inputs to IC71-B are HIGH, the output will go LOW and, through R22, will drive the **EVENTO/R bar** line LOW to load the filter count and enable the clock input from **CLKB**. If the trigger word is present for the correct number of clock inputs the counter will count, via **CLKB**, to terminal count and **EVENT** will go HIGH. **EVENT** passes back to IC24 pin 7 through IC48-D. If the pre-trigger count has been satisfied or the pre-trigger is OFF then **PRGRTDEL bar** will be LOW and IC48-D output will go LOW to disable IC24 from counting until the output from IC71-B goes HIGH and then LOW again to reload the event counter.

EVENTO/R bar can also be driven from the rear panel input, PJ7 pin 3, as **GOTO0/R bar**, being inverted twice through IC33-D and IC32-B, to override the output from IC71-B to terminate EVENT trigger filter counting. R18 ensures that the input is held HIGH to stop false triggering. **EVENTO/R bar** is available on PJ10 pin 4.

EVENT is inverted through IC47-C and passes to IC47-B. **EVENT/CLK bar** is Used to allow **CLKB** through IC47-A when LOW to count trigger word clocks through IC47-B, and block **CLKB** when HIGH to allow event clocks through IC47-B by generating the clock **COUNT**.

The event counter is loaded before an acquisition by generating a clock through IC71-B using the CPU to set up IC22 and IC29 to generate recognised words and then pulsing **CLKB** to load the filter count. The count loaded in this way is always one less than the actual count which is set up ready for the first event in case there is a don't care trigger set up on the first clock, or the trigger word is already on the input, and the counter is counted up by **CLKB** clock.

3.5.12. GOTO Trigger Filter

ref. fig 3, 1/D,E

The GOTO trigger filter consists of IC23, IC31, IC71-A and IC25. The 4 x 4 register is loaded using write address lines, **WS0** and **WS1**, and, after setting up the data on lines **DH0** to **DH3**, using the write enable line, **TWR7 bar**, to write the data into the register. The outputs from

the register determine which trigger words are set up in each sequence step by holding the input to the OR gate. IC31, LOW when selected. When a trigger word is recognised the outputs, TRGA to TRGD, are also passed into the IC31 to generate a HIGH output into IC71-A. When all selected trigger words are recognised and all inputs to IC71-A are HIGH, the output will go LOW and, through R24, will drive the **GOTOO/R bar** line LOW to load the filter count and enable the clock input from **CLKB**. If the trigger word is present for the correct number of clock inputs the counter will count, via **CLKB**, to terminal count and GOTO will go HIGH. **GOTO** passes back to IC25 pin 7 through IC48-C. If the pre-trigger count has been satisfied or the pre-trigger is OFF then **PRTRGDEL bar** will be LOW and IC48-C output will go LOW to disable IC25 from counting until the output from IC71-A goes HIGH and then LOW again to reload the event counter.

GOTO is inverted through IC32-C and passes to IC25 pin 9 to reload the count into IC25.

GOTOO/R bar can also be driven from the rear panel input, PJ7 pin 4, as **EVENTO/R bar**, being inverted twice through IC33-E and IC32-A, to override the output from IC71-A to terminate **GOTO** trigger filter counting. R18 ensures that the input is held HIGH to stop false triggering. **GOTOEN bar** is available on PJ10 pin 3.

The goto counter is loaded before an acquisition by generating a clock through IC71-A using the CPU to set up IC23 and IC29 to generate recognised words and then pulsing **CLKB** to load the filter count.

3.5.13. Trace ON and Trace OFF Trigger Filter

ref. fig 3, 3,4/D,E

The trace trigger filter consists of IC28, IC34, IC35, IC70, IC26 and IC27. The shift register, IC28, is loaded using the serial data and serial clock outputs, **SDATA** and **SCLK** from IC49 to select the TRACE ON and TRACE OFF trigger words. When the selected trigger word into IC34 is recognised to turn the trace recording ON then ON goes LOW out of IC70-A to parallel load IC26 with the filter count. When the filter count has been satisfied IC26 terminal count, **TRACEON**, will go HIGH and through analogue gate, IC68-B, into IC48-B. The output of IC48-B, **TRACE bar** will go LOW to select trace to be turned ON.

When the selected trigger word into IC35 is recognised to turn the trace recording OFF then OFF goes LOW out of IC70-B to parallel load IC27 with the filter count. When the filter count has been satisfied IC27 terminal count, **TRACEOFF**, will go HIGH and into bi-stable gates, IC48-A and IC48-B, to toggle the output of IC48-B, **TRACE bar** HIGH to select trace to be turned OFF. **TRACE bar** is fed back into IC48-A to latch the output until the trace is turned ON again. The analogue gate, IC68-B, and R20 are used before an acquisition is run to select the trace to be turned ON by switching IC68-B, using **RESET bar**, to open circuit which enables R20 to pull IC48-8 input HIGH to pull **TRACE bar** LOW. The output through R1 is available on PJ10 pin 1.

3.5.14. Trigger Word Counter

ref. fig 3, 2,3/E-H

The trigger word counter consists of IC37 to IC41. The 4 x 4 registers, IC40 and IC41, are loaded using write address lines, **WS0** and **WS1**, and, after setting up the data on lines **DH0** to **DH1**, using the write enable line. **TWRB bar**, to write the data into the registers. The outputs from the registers determine the trigger words count in each sequence step by passing their outputs to the 8-bit comparator, IC39. The trigger word counters, IC37 and IC38, are reset to zero by **CLRCNT bar** when the

sequencer steps to the next step. Their outputs are also fed into the 8-bit comparator so that when the COUNT clock increments the trigger word counters so that their outputs equal those of the 4 x 4 register, the comparator output, **EQUAL bar**, will go LOW to activate the left side of the sequencer.

3.5.15. Sequence Step Counter

ref. fig 3, 3,4/F-H

IC42 is the sequencer step counter and can be incremented to the next sequence step as determined by the left-hand side of the sequence menu or jump to a pre-programmed sequence step as determined by the right-hand side of the sequencer menu.

The 4x4 register, IC43, is loaded with the start step data, output from the PIA on lines **DH0** to **DH3** using **WS0** and **WS1** as address lines and **TWR9 bar**, from IC53, which is pulsed LOW through IC51 to write the sequence step data into IC43. At the start of an acquisition **ARESET bar** is pulled LOW which resets the sequencer counter, IC42, and, via the integrator R21 and C18, sets **CLRCNT bar** HIGH and resets **STEPLD bar** out of IC36-A. IC36-A, IC47-D and R33 act as a delay for **GOTO** through IC47-0 to pull **STEPLD bar** HIGH by clocking the latch through R33, after **ARESET bar** has been removed from IC36-B to pulse **CLRCNT bar** LOW to reset trigger word counters, IC37 and IC38. **STEPLD bar** going HIGH is used to parallel load the data from IC43 into IC42. The flip-flop formed by IC56-A and IC56-B is also reset by **ARESET** to pull **TRIGGERED** LOW.

If the trigger word counters, which were set up on the left-hand side of the sequencer menu, reach the programmed count and the **EQUAL bar** line goes LOW then the next **CLKA** will clock **CLRCNT bar** LOW out of IC36-B to reset the trigger counters. **STEPEN bar** will also go HIGH to enable **CLKB** to increment the sequence counter by one and output the next sequence step via **SS0**, **SS1** and **SS2**, the former two being fed back into the sequencer register, IC43, ready for the next step.

If the trigger word, which was set up on the right-hand side of the sequencer menu, is recognised then the **GOTO** line will go HIGH and, through IC47-D, sets IC36-A to pull **STEPLD bar** LOW to parallel load IC42 with the programmed sequence step data from IC43. This also resets IC36-B to pull **CLRCNT bar** LOW to reset the trigger word counters ready for the next step.

When the sequencer reaches the count of four, with **SS0** and **SS1** both **SS2** HIGH, the flip-flop formed by IC56-A and IC56-8 is latched **TRIGGERED** HIGH and **TRIGGERED bar**, which is available through PJ7 pin **TRIGGERED bar**, LOW. This is the trigger step.

3.5.16. Post-trigger Counter

ref. fig 3, 5/F-H

The post-trigger counters are used to store samples after the trigger has been point recognised and they consist of IC44, IC72, IC45 and IC73. These counters are loaded from the serial data, **SDATA1**, clocked into IC46 by the serial clock, **SCLK**. This data is parallel loaded into the counters by the CPU outputs **WS0** and **WS1** before the acquisition starts.

When **TRIGGERED** goes HIGH the counters are enabled and **TRACECLK** is used to increment the counters until the terminal count is reached and **STOPPED** goes HIGH. **TRACECLK** is derived from **CLK1A** and **TRACE bar**. When **TRACE bar** goes LOW to turn trace ON then **TRCLKEN** goes HIGH through

IC63-A. When the next a **CLK1A** enters the latch, IC60-B, **TRACECLK** will go high and, via IC62-A and integrator R19 and C17, go LOW again to produce the positive going pulse, **TRACECLK**. When **TRIGGERD** is HIGH it will increment the post-trigger counters.

3.5.17. Acquisition Status

ref. fig 3, 5/F-H & 5/D,E

During an acquisition the CPU (IC49) repeatedly reads the two lines, **TRIGGERED** and **STOPPED**. **TRIGGERED** is used to detect when the trigger has been seen and display the relevant status message. **STOPPED** is used to detect the end of an acquisition and display the fact. The trigger position and store content are calculated from the user setting of the trigger position and post-trigger delay.

If the user stops the acquisition before the post trigger counter has reached terminal count then **GO bar** is set HIGH to stop any more clocks entering and **PROCCLK** bar is pulled LOW by the CPU to generate **TRACECLK** to increment the post-trigger counters until **STOPPED** goes HIGH so the trigger position can be calculated.

3.5.18. CPU Central and Interface

ref. fig 3, 1-3/A-D

The CPU is a 6303X running at 8MHz which is controlled using XT1, C1 and C2. The MAIN board also contains the circuitry for the RS-232 interface with the CPU board, decoded I/O ports, pod threshold line and the LCD contrast control.

The CPU data bus, **DO-D7**, and address bus, **A0-A15**, connect directly to CPU EPROM, IC50 and PIA, IC51. The MAIN board CPU has the ability to address 32K of EPROM from 8000H to FFFFH of the memory map, controlled by **A15 bar**, but the board only contains an 8K EPROM. The PIA is located between 4000H and 4003H as controlled by **A0**, **A1**, **A14** and **A15**.

The PIA uses its 'A' port to generate a secondary data bus, **DH0-DH7**, which is fed to the various devices on the MAIN board to provide data to set up the sequencer. The PIA also addresses two decoders, IC52 and IC53, using its 'S' port to generate the MAIN board control lines, **RAMRD1 bar - RAMRD6 bar** and **TWR1 bar - TWR9 bar**, which are used to write to or select the various devices. The three top lines from the 'S' port are used to select the various clock inputs to the internal clock multiplexer, IC55.

The threshold to the pods is generated by the CPU. The outputs from the first two internal timers, which are set up according to the voltage required, are XORed together and integrated by R12 and C12 and decoupled by C13, C23 and C33 to produce VREF which is passed to the pods via connectors PJ1, PJ2 and PJ3 respectively.

The MAIN board interfaces with the CPU board via a 16-way flat cable from PJ6. The interface consists of the CPU RS232 signals TX and RX which receive set up information and transmit acquisition data and status respectively. The interface also consists of the system reset signal, **PSUON** which is generated from the Power Supply, via PJ5 pin 5, and used to reset the CPU and PIA on the MAIN board and passed to the CPU board through PJ6.

The Power Supply, as well as generating a +5V and -5V rail via PJ5, also generates a -23V line, **VLCD**, which is used across VR1 to tap off the variable voltage signal, **VLCDON** which is passed, via PJ6, along

with **VLCD** and the power rails to the CPU board. **VLCDCON** is used by the LCD as the contrast control with VR1 operated from the front panel.

3.5.19. MAIN PCB Signal Directory

ACQWR bar	Write clock for the acquisition data rams
ANALFULL	Pre-trigger counter control line to show store full
ARAMRD bar	Input data ram read control line
ARESET	Analyser reset line
ARESET bar	Inverted version of ARESET
A0-A15	CPU address bus
BD0 - BD47	Buffered input data lines
CLKA	Clock line derived from one of the input clocks
CLKB	Delayed version of CLKA
CLKC	Secondary data latch clock line
CLK1 - CLK3	Input clock lines
CLK1 A	Input data latch clock line
CLPOL1 - CLPOL3	Input clock polarity select lines
CL1 - CL3	Input clock lines
CLOCK OUT	Clock line out to rear panel derived from CLKA
CLRCNT bar	Reset line to clear clock/event counter
COUNT	Clock line to increment clock/event counter
CSEL1 - CSEL3	Input clock select lines
DA0 - DA15	Input data pod A signals
DB0 - DB15	Input data pod B signals
DC0 - DC15	Input data pod C signals
DH0 - DH15	PIA data bus A
D0 - D7	CPU data bus
EPROMDATA	Input line for reading EPROM data
EVENT	Event trigger filter terminal count line
EVENT/CLK bar	Event or Clock count select line
EVENTO/R bar	Override signal to stop event trigger filter count
EVENT OVERRIDE bar	Rear panel input to stop event trigger filter count
EQUAL bar	Event/clock counter terminal count line
EXTCLKIN	Rear panel input for external clock (disabled)
GO bar	Acquisition start line
GOTO	Clock trigger filter terminal count line
GOTOO/R	Override signal to stop clock trigger filter count
GOTO OVERRIDE bar	Rear panel input to stop clock trigger filter count
INTCLK	Internal clock line to external clock circuit
ICSEL0 - ICSEL2	Internal clock select lines
IPLATCHEN bar	Data input latch enable
LOAD bar	Disassembler pod data load control signal
LD0 - LD47	Latched input data bus for word recognition
OFF	Trace off recognition output
ON	Trace on recognition output
PB0 - PB2	Select lines for read and write control signals
PODCLK	Clock for High Speed data pod
PODSEL1	Select line for High Speed data pod
PODSEL2	Select line for High Speed data pod
PROCCLK bar	CPU clock for incrementing trace and delay counters
PROCWR bar	CPU clock for generating ACQWR bar
PRTRGDEL	Enable line to activate pre-trigger delay count
PRTRGDEL bar	Inverted version of PRTRGDEL
PSUON	Power supply ON control line for system reset
QPOL1 - QPOL3	Qualifier polarity select lines
QSEL1 - QSEL3	Qualifier select lines
QUAL1 - QUAL3	Qualifier input lines
RAMBUFEN bar	Enable line for selecting input data ram buffers
RAMRD1 bar	- Read control lines for input data rams
RAMRD6 bar	

RA0 - RA12	Address lines for input data rams
RD bar	CPU read control line
RD0 - RD47	CPU data bus
RX	CPU data transmit line to CPU board
SCLK	CPU serial clock for serial acquisition setup data
SDATA	CPU serial acquisition setup data output
SDATA1	Serial data output for post trigger counters
SDATA2	Serial data output for clock and qualifiers
SLOWCLK	CPU internal clock output for slow clocks
SS0 - SS2	Sequencer step number control lines
STEPEN	Enable line to allow stepping to the next step
STEPLD bar	Control line to allow sequencer step loading
STOPPED	Output from post trigger counters when complete
STPCLK bar	Control signal to block clocks when complete
TOUT1	CPU timer output used to generate VREF
TOUT2	CPU timer output used to generate VREF
TRACE bar	Control line gated with STOPPED to enable trace
TRACECLK	Clock used to increment data store counters
TRACEOFF	Control line to turn the trace facility OFF
TRACEON	Control line to turn the trace facility ON
TRACE1 bar	Feedback signal from TRACE bar
TRCLKEN	Trace enable line derived from TRACE bar
TRGA - TRGD	Valid trigger word outputs
TRGLATCHEN bar	CPU output to enable word recognition buffers
TRIGGERED	Output from sequencer when enters step5
TRIGGERED bar	Inverted version of TRIGGERED
TWR1 bar-TWR9 bar	Trigger word recogniser write lines
TX	CPU data receive line from CPU board
VLCD	Supply line to LCD
VLCDCON	Variable supply line to LCD to adjust contrast
VREF	Reference voltage for variable threshold pods
WORDA - WORDD	Trigger word recognition outputs
WORD A TRUE bar	Rear panel trigger word A recognition output
WORD B TRUE bar	Rear panel trigger word B recognition output
WREN bar	PIA write output for read and write control signals
WS0 - WS1	CPU setup registers write address lines
Z0 - Z7	Serial setup data bus
2k/8kSEL bar	Select line for data storage size
2MHz	}
5MHz	}Clocks for internal clock selection
10MHz	}
20Mhz	}
25MHz	}
+5V	+5Volt supply rail
0V	Ground rail
-5V	-5 Volt negative supply rail

3.6. CLOCK AND DATA PODS

3.6.1. General

The analyser uses 4 types of pod. The AP01 has 32 data channels and 3 separate clock inputs each independently qualified by its own qualifier. The AP02 has 48 data channels and 3 separate clock inputs each independently qualified by its own qualifier. Both the AP01 and AP02 have fixed TTL threshold inputs. The AP03 is a High Speed Data Pod with 16 data channels; if an external clock is required with AP03 data-pods then the AP04 High Speed Clock pod must be used. The AP04 High Speed Clock Pod has 3 separate clock inputs each independently qualified by its own qualifier. The AP03V and AP04V are the variable threshold versions of the AP03 and AP04 and again must be used together when an external clock is required. AP03 pods cannot be mixed with AP04V pods and vice-versa. Disassembler pods, except the DP-68000, use an AP01 board with a CPU specific patch board fitted to configure the CPU lines into the analyser. The same applies to the DP-68000 except that AP02 boards are used.

3.6.2. AP01 32 Channel Data and Clock Pod

ref. fig 4

Input data lines, **I0 - I40**, are configured by the patch board and passed to the relevant data channels, **A0 - A15** and **B0 - B15**, clock lines, **CLK1 - CLK3**, and qualifier lines, **CQ1 - CQ3**. All data, clock and qualifier lines have series resistors for overload protection and pull-up resistors to pull any unused lines to a known state.

All lines pass through input latches which have their latch enable inputs pulled HIGH through resistors in RP9. In this way the latches are acting as buffers. Input latch lines, **AL1**, **AL2**, **BL1** and **BL2** can be used as clock lines for the data latches, IC5 to IC8, but in this case are not used.

All lines pass through more series resistors for input protection and then enter the analyser, via the relevant connectors, as data lines to channel A, **BA0 - BA15**, channel B, **BB0 - BB15**, clocks, **BCLK1 - BCLK3** and qualifiers, **BQUAL1 - BQUAL3**.

Components R4 to R6, Q1 and Q2 form a 5 volt isolation circuit so that when the 5 volt rail disappears Q1 is turned OFF which pulls **CS bar** HIGH to disable IC1, IC2 and IC4 to ICB. Q1 turning OFF also turns OFF Q2. This isolates the analyser +5 volt rail so that if the analyser was turned OFF the pod would not use the target signal lines to power up the CMOS devices on the board and, ultimately, the analyser itself.

When the AP01 is used as a disassembler pod a different patch board is used to configure the input lines correctly for the particular CPU. An EPROM is fitted as IC1, which is absent in the AP01, and the disassembler code is loaded by the analyser at start up. Loading is started by resetting IC2 and IC3, due to **SCLK** sitting HIGH, to set all the EPROM address lines to zero. **LOAD bar** is pulled LOW, to parallel load IC11 with the first memory location data from IC1, and then HIGH to clock the counters, IC2 and IC3, to the next memory location. **SCLK** is passed through the integrator, R1 and C1, to pull the master reset lines on the counters below the threshold.

The serial clock, **SCLK**, is then driven to output the serial data, EPRDMDATA, from IC1 a bit at a time, which is read into the CPU on the MAIN board. When all eight bits have been read, **LOAD bar** is pulled LOW

again to parallel load the EPROM data from the second location.

3.6.3. AP01 Signal Directory

A0-A15	Channel A input data lines
AL1 - AL2	Latch clock lines to Channel A latches
B0 - B15	Channel B input data lines
BA0 - BA15	Buffered channel A data lines
BB0 - BB15	Buffered channel B data lines
BCLK1 - BCLK3	Buffered clock lines
BL1 - BL2	Latch clock lines to Channel B latches
BQUAL1 - BQUAL3	Buffered clock qualifier lines
CLK1 - CLK3	Input clock lines
CQ1 - CQ3	Input clock qualifier lines
CS bar	Latches and EPROM chip select line
EPROMDATA	Serial data line to analyser
I0 - I39	Input data lines
LOAD bar	Load control line from analyser
SCLK	Serial clock line from analyser
+5V	5 volt supply line.
+5VA	Isolated 5 volt supply line
0V	Ground line

3.6.4. AP02 48 Channel Data and Clock Pod

ref. fig 5

The AP02 consists basically of an AP01 board with an extra board sited above it which accommodates the extra 16 channels necessary. Consequently the circuit description for the AP01 board should be read in conjunction with the description of the AP02 upper board.

Input data lines, **I0 - I15**, are configured by the patch board and passed to the relevant data channels, **C0 - C15**. All data lines have series resistors for overload protection and pull-up resistors to pull any unused lines to a known state. All data lines pass through input latches which have their latch enable inputs pulled HIGH through resistor R1. In this way the latches are acting as buffers. The latch line, **CL1** can be used as clock lines for the data latches, IC1 and IC2, but in this case are not used.

All data lines pass through more series resistors for input protection and then enter the analyser, via the relevant connector, as data lines to channel C, **BA0 - BA15**.

Components R3, R4, Q1 and Q2 form a 5 volt isolation circuit so that when the 5 volt rail disappears Q1 is turned OFF which turns OFF Q2. This isolates the analyser +5 volt rail so that if the analyser was turned OFF the pod would not use the target signal lines to power up the CMOS devices on the board and, ultimately, the analyser itself.

The remaining input lines, **I16 - I25** are reserved for future use with disassembler pods as are the lines **T0 - T19** which are used to transfer signals from the upper board to the lower board and vice-versa.

3.6.5. AP02 Signal Directory

C0 - C15	Channel C input data lines
BC0 - BC15	Buffered channel C data lines
CL1	Latch clock lines to Channel C Latches
I0 - I25	Input data lines
T0 - T19	Transfer signal lines
+5V	5 volt supply line
+5VA	Isolated 5 volt supply line
0V	Ground line

3.6.6. AP03 16 Channel High Speed Data Pod

ref. fig 6

The AP03 can function in one of three modes; Direct, Glitch or 100MHz mode. The mode is selected by the analyser using the control lines **PODSEL1** and **PODSEL2**. IC23-A, IC23-B and IC23-D are used to select the three modes of operation which involves enabling various combinations of devices which then output their data onto the output data bus, **D0 - D15**. This data is overload protected by RP3, RP4, RP5 and RP6 to produce **DATA0 - DATA15** which is transmitted to the analyser.

The data inputs, **PDO - PD15**, have series resistors for overload protection and pull-up resistors to pull any unused lines to a known state. The data is buffered and inverted by IC24, IC25 and IC26-A to IC26-D to produce **BDO - BD15**. This data bus is routed through to the various combinations of devices selected for each of the three modes of operation.

3.6.6.1. Direct Mode

In Direct Mode the analyser is set to External clock using the High Speed Clock Pod, AP04, and the data seen on the inputs is buffered and passed through to the analyser directly without being latched.

In direct mode PODSEL1 and PODSEL2 are pulled HIGH so that **PODSEL1 bar** goes HIGH and this holds **ENGLITCH bar** HIGH. PODSEL1 and PODSEL2 being HIGH drives **ENDIRECT bar** LOW which enables the outputs from IC13 and IC14 onto the output data bus. **PODCLK** is not used and is blocked by **CLKEN** being driven LOW through IC22-B when **PODSEL2** goes HIGH.

As a result **BDO - BD15** are inverted by buffers IC13 and IC14 to produce output data, **DO - D15**.

3.6.6.2. Glitch Mode

In Glitch mode channels **BDO - BD07** are used to generate eight data outputs and eight glitch outputs to produce sixteen channels of output data, **DO - D15**.

In Glitch mode **PODSEL1** being LOW and **PODSEL2** being HIGH drives **ENDIRECT bar** HIGH which leaves **EN100 bar** HIGH, **PODSEL1** going LOW drives **PODSEL1 bar** HIGH so which, with **PODSEL2** being HIGH, drives **ENGLITCH bar** LOW to enable the outputs from IC15 and IC16 onto the output data bus. **PODCLK** is enabled by **CLKEN** going HIGH through IC22-B when **PODSEL2** goes LOW.

The rising edge of **PODCLK** is used to generate **CLKA**, a narrow positive going pulse of approximately 7nS, using IC23-C, IC21-C and R3. R4 and R7 are used to delay **CLKA** and **CLKB**, and IC22-C, IC26-F and IC26-E is used to generate a delayed and inverted version of **CLKA**, **CLKD**. **CLKB** is used to latch **BDO - BD7** into IC12 which becomes the eight bits of data on **D0 - D7**. **CLKA** is used to latch **BDO - BD7** into IC4. **CLR** is used to hold the JK flip-flops, IC7, IC8, IC9 and IC10 in a reset condition until the data latched into IC4 has propagated through IC5 and IC6 to the clock inputs of the flip-flops.

At the time when **BDO - BD7** is latched into IC4 the same information is present on both inputs to the XOR gates IC5 and IC6 which will hold their outputs LOW. When an input on **BDO - BD7** changes state the XOR output will go HIGH, but it will not be until the input changes state again that the output going LOW will clock the JK flip-flop to register a glitch occurrence.

CLKA used is also delayed through IC21-B, IC21-A and R5 to produce **CLKC** which is at the end of the cycle to latch the glitch data into the

glitch latch, IC11. The glitch data from this latch, **BD8 - BD15**, is passed to the analyser at the same time as the data, **BD0 - BD7** to produce the sixteen channels of glitch and data.

3.6.6.3. 100MHz Mode

In the 100MHz Mode channels **D0 - D3** are used and multiplexed successively four times into different devices to produce sixteen channels of output data, **D0 - D15**.

In 100MHz mode **PODSEL1** and **PODSEL2** are pulled LOW so **ENGLITCH bar** is HIGH. **PODSEL1** and **PODSEL2**, being LOW drives **ENDIRECT bar** HIGH which leaves **EN100 bar** LOW which enables the outputs from IC15 and IC16 onto the output data bus. **PODCLK** is enabled by **CLKEN** going HIGH through IC22-B when **PODSEL2** goes LOW.

The analyser generates **PODCLK** as a 25MHz rectangular clock which is inverted through IC22-D and again through IC22-A to produce **CLK100A** and then successively delayed through IC20-A, IC20-B and IC20-C to produce **CLK100B**, **CLK100C** and **CLK100D** respectively. The clocks are further delayed by C1, C2 and C3 and accurately phased using VR1, VR2 and VR3 which are set to produce successive delays between **CLK100A**, **CLK100B**, **CLK100C** and **CLK100D** of 10 nsec. The first three of these clocks are used to latch the buffered input data lines **BD0 - BD3** to produce **D0CLKA - D3CLKA**, **D0CLKB - D3CLKB** and **D0CLKC - D3CLKC** from IC17, IC18 and IC19 respectively. These outputs, along with **BD0 - BD3** are passed to IC15 and IC16 to be latched by **CLK100D** to produce the output data, **D0 - D15**.

3.6.7. AP03 Signal Directory

BD0-BD7	Buffered and inverted input data lines
CLKA	Positive pulse generated from PODCLK
CLKB	Positive pulse generated from PDDCLK
CLKC	Delayed version of CLKA
CLKEN	Inverted version of PODSEL2
CLK100A	1st. latch clock used in 100MHz mode
CLK100B	2nd. latch clock delayed from CLK100A by 10ns
CLK100C	3rd. latch clock delayed from CLK100B by 10ns
CLK100D	4th. latch clock delayed from CLK100C by 10ns
CLR	Delayed and inverted version of CLKA
DATA0 - DATA15	Output data lines to analyser
D0 - D15	Output data lines
D0CLKA - D3CLKA	Input data lines latched by CLK100A
D0CLKB - D3CLKB	Input data lines latched by CLK100B
D0CLKC - D3CLKC	Input data lines latched by CLK100C
ENDIRECT bar	Select line to enable direct mode output
ENGLITCH bar	Select line to enable glitch mode output
EN100 bar	Select line to enable 100Mhz mode output
PODCLK	Analyser clock output line
PODSEL1	Analyser control output line
PODSEL2	Analyser control output line
PDO - PD7	Input pod data lines
+/-5V	5 volt supply lines
0V	Ground line

3.6.8. AP03V High Speed Variable Threshold Data Pod

ref. fig 7

This pod consists of two boards. The lower board is an AP03 board with connectors fitted to route the input signals, **BDO - BD15**, to an upper variable board. The upper board provides a variable input voltage threshold and any signals satisfying the threshold setting, **OD0 - OD15**, are passed back through another connector to the lower board to continue their path through the AP03, which provides the same Direct, Glitch and 100MHz modes of operation. A five pin connector conveys

power and ground and **VREF**, a threshold control signal, to the upper board.

The AP03 board does not have any input pull-up resistors or series resistors but has a 32-way connector fitted, in their place, to divert the input signals to the upper board.

On the upper board channel 0 will be described in detail as being representative of all channels. **PDO** is passed, via the cable interface, to the upper board where it is attenuated by R1 and R2 with capacitor C21 providing HF compensation. Control of the switching threshold is affected by altering the DC control voltage of **THR1** which is applied to R2. C13 is used to decouple **THR1**. The comparator function is provided by IC1-D whose inputs provide approximately 90 mV of internal hysteresis while the unused input pin 10 is grounded. The output from IC1-D, **CHO**, is buffered by IC5 and damped by RP1-A and passed through the cable interface back to the lower board as **ODO**.

The threshold control voltage, **THR1**, is generated using the **VREF** line, which is either a DC voltage in the range of +10V to -2.5V or a 5V 200Hz pulse width modulated signal varying from 1 to 81% duty cycle over the threshold control range of +10V to -2.5V.

If the analyser generates **VREF** as a DC voltage then the control line of ICB-C, via C4 and R85, will go LOW to allow the output, **PWM bar**, to go HIGH and charge C6 through R84. While **PWM bar** is HIGH IC8-B will select its input from VR6, used with R80 and R81 to provide scale length adjustment with a DC voltage **VREF**, to produce **DCREF** which is decoupled by C9 to provide a stable DC voltage.

If the analyser generates **VREF** as a pulse width modulated signal then the control line of ICB-C, via C4 and R85, will get charged HIGH to switch the output, **PWM bar**, LOW and discharge C6. While **PWM bar** is LOW IC8-B will select its input from IC8-A. VREF drives the control gate of IC8-A and switches the output between the +3.4V stabilised supply and 0V. This output is filtered by R83, C7 and R82 to produce **DCREF** which is decoupled by C9 to provide a stable DC voltage proportional to the incoming duty cycle.

DCREF is amplified by IC7-D, Q1, R71-R74, C12 and VR5 to raise the control voltage, with VR5 being used to provide scale length adjustment. IC7-C and associated components maintain a constant 0.75V across offset controls VR1-VR4 which are factory set to minimise the affects of threshold differences between the individual inputs of the gates of IC1-IC4. **THR1** is generated via VR1 to control the threshold level of the incoming signal.

The voltage regulator system IC7-A, Q2, reference diode D1 and components provides a stable +3.4V supply to IC1-IC4 and IC8-A.

At the factory VR2 is adjusted to provide precisely a 7.17V swing as the PWM signal is varied from 1 to 81 per cent duty cycle, corresponding to the extreme values of +10V to -2.5V of input voltage threshold required. Then with a duty cycle corresponding to -1.3V presets VR1 is adjusted to centralise the spread of the four input thresholds corresponding to each gate of IC1 (which are generally within 30mV). This process is repeated for IC2-IC4 by adjusting the corresponding presets VR2-VR4.

With an appropriate D.C. voltage applied to **VREF** VR5 is adjusted to give the same voltage at TP1 as that obtained after calibration using a PWM signal of 5 per cent duty cycle corresponding to a -1.3V ECL threshold.

3.6.9. AP03V Signal Directory

CH0 - CH15	Threshold dependant output from comparators
DCREF	Threshold DC voltage output
OD0 - OD15	Output data lines
PWM bar	Select line to enable DC input control voltage
PDO - PD7	Input pod data lines
THR1 - THR3	Threshold inputs to the comparators
VREF	Threshold DC voltage output
+/- 5V	5 volt supply lines
+3.4V	Generated 3.4 volt supply line
0V	Ground line

3.6.10. AP04 High Speed Clock Pod

ref. fig 8

The clock inputs, **CLK1 - CLK3**, and qualifier inputs, **QUAL1 - QUAL3** have series resistors for overload protection and pull-up resistors to pull any unused lines to a known state. They are buffered and inverted by IC25-C to IC25-F and IC26-A to IC26-D to produce **BCLK1 - BCLK3** and **BQUAL1 - BQUAL3**. These are further buffered and inverted by IC12 and passed through overload protection resistors in RP3 and RP4 to produce the outputs to the analyser, **CLK 1 - CLK 3** and **QUAL 1 - QUAL 3**.

The AP04 board is a depopulated version of the AP03 board and so LK1 is fitted to pull the output enable lines on IC12 LOW to enable it. LK2, LK3 and LK4 are all fitted to tie the inputs of the spare gates in IC25 and IC26 to eliminate noise on the inputs and hence minimise current consumption. C4 and C5 are used to decouple the spare lines to the analyser.

3.6.11. AP04 Signal Directory

BCLK1 - BCLK3	Buffered and inverted clock input lines
BQUAL1 - BQUAL3	Buffered and inverted qualifier input lines
CLK1 - CLK3	Clock input lines
CLK 1 - CLK 3	Clock output lines
QUAL1 - QUAL3	Qualifier input lines
QUAL 1 - QUAL 3	Qualifier output lines
+5V	5 volt supply line
0V	Ground line

3.6.12. AP04V Variable Threshold High Speed Clock Pod

ref. fig 9

This pod consists of two boards. The lower board is an AP04 board with connectors fitted to route the input signals, **BDO - BD15**, to an upper variable threshold board. The upper board provides a variable input voltage threshold comparator and any signals satisfying the threshold setting, **OD0 - OD15**, are passed back through another connector to the lower board to continue their path through the AP04, which provides the same Direct, Glitch and 100MHz modes of operation. A five pin connector conveys power and ground and VREF, a threshold control signal, to the upper board.

The AP0 3/4 board does not have any input pull-up resistors or series resistors but has a 32-way connector fitted, in their place, to divert the input signals to the upper board.

On the upper board channel 0 will be described in detail as being representative of all channels. **PDO** is passed, via the cable interface, to the upper board where it is attenuated by R1 and R2 with capacitor C21 providing HF compensation. Control of the switching threshold is affected by altering the DC control voltage of **THR1** which is applied to R2. C13 is used to decouple **THR1**. The comparator function is provided

by IC1-D whose inputs provide approximately 90 mV of internal hysteresis while the unused input pin 10 is grounded. The output from IC1-D, **CH0**, is buffered by IC5 and damped by RP1-A and passed through the cable interface back to the lower board as **D0**.

The threshold control voltage, **THR1**, is generated using the **VREF** line, which is either a DC voltage in the range of +10V to -2.5V or a 5V 200Hz pulse width modulated signal varying from 1 to 81% duty cycle over the threshold control range of +10V to -2.5V.

If the analyser generates VREF as a DC voltage then the control line of IC8-C, via C4 and R85, will go LOW to allow the output, **PWM bar**, to go HIGH and charge C6 through R84. While **PWM bar** is HIGH IC8-B will select its input from VR6, used with R80 and R81 to provide scale length adjustment with a DC voltage **VREF**, to produce **DCREF** which is decoupled by C9 to provide a stable DC voltage.

If the analyser generates **VREF** as a pulse width modulated signal then the control line of IC8-C, via C4 and R85, will get charged HIGH to switch the output, **PWM bar**, LOW and discharge C6. While **PWM bar** is LOW IC8-B will select its input from IC8-A. **VREF** drives the control gate of IC8-A and switches the output between the +3.4V stabilised supply and 0V. This output is filtered by R83, C7 and R82 to produce **DCREF** which is decoupled by C9 to provide a stable DC voltage proportional to the incoming duty cycle.

DCREF is amplified by IC7-D, Q1, R71-R74, C12 and VR5 to raise the control voltage, with VR5 being used to provide scale length adjustment. IC7-C and associated components maintain a constant 0.75V across offset controls VR1-VR4 which are factory set to minimise the effects of threshold differences between the individual inputs of the gates of IC1-IC4. **THR1** is generated via VR1 to control the threshold level of the incoming signal.

The voltage regulator system IC7-A, Q2, reference diode D1 and components provides a stable +3.4V supply to IC1-IC4 and IC8-A.

At the factory VR2 is adjusted to provide precisely a 7.17V swing as the PWM signal is varied from 1 to 81 per cent duty cycle, corresponding to the extreme values of +10V to -2.5V of input voltage threshold required. Then with a duty cycle corresponding to -1.3V presets VR1 is adjusted to centralise the spread of the four input thresholds corresponding to each gate of IC1 (which are generally within 30mV). This process is repeated for IC2-IC4 by adjusting the corresponding presets VR2-VR4.

With an appropriate D.C. voltage applied to **VREF** VR5 is adjusted to give the same voltage at TP1 as that obtained after calibration using a PWM signal of 5 per cent duty cycle corresponding to a -1.3V ECL threshold.

3.6.13. AP04V Signal Directory

CH0 - CH15	Threshold dependant output from comparators
DCREF	Threshold DC voltage output
OD0 - OD15	Output data lines
PWM bar	Select line to enable DC input control voltage
PD0 - PD7	Input pod data lines
THR1 - THR3	Threshold inputs to the comparators
VREF	Threshold DC voltage output
+/- 5 V	5 volt supply lines
+3.4V	Generated 3.4 volt supply line
0V	Ground line

3.7. GP500A IEEE-488 INTERFACE OPTION

ref. fig 10

The IEEE-488 circuit connects to the CPU board via CON1 and the two serial lines, **TXD** and **RXD**, pass directly into the corresponding CPU serial input and output lines on U1 pin 11 and pin 12. The **CTS bar** and **RTS bar** signals pass to the CPU I/O lines on U1 pin 13 and pin 14 respectively. Power to the board is taken from the CPU connector, CON1.

The 6303 CPU is driven by the oscillator components, XL1, C2 and C3. The CPU mode input lines on U1 pins 8 and 9 are pulled LOW by R1 and R2 and the third CPU mode line is pulled HIGH at reset. At reset U8-D pin 13 will be LOW and will be held LOW by C4. C1 will delay the rise on the input of U9-D and this will continue to hold **RESET bar** LOW until after the mode pins have been latched. The mode pins set the CPU into multiplexed mode so the data bus, **D0 - D7**, is multiplexed with the lower address bus, **A0 - A7**. **RESET bar** is used to reset the CPU and IEEE-488 controller and hold off the chip selection of the EPROM until after **RESET bar** goes HIGH.

U2 is used to latch the address bus using **AS** during the first half of the CPU cycle. The data bus is also connected to the EPROM1, U3, the RAM, U4, IEEE-488 controller, U5. The latched lower address bus and the upper address bus, **A8 - A15** are connected to the EPROM and the RAM.

Chip selection is accomplished using U8-A, U9-B, U8-C and U9-C and the top four address lines, **A12 - A15**. The 16K EPROM, U3, is selected when **RESET bar** and **A15** are HIGH, generating **CS1 bar**, placing it in either of the top 16K address blocks from 8000H to FFFFH. The 8K RAM, U4, is selected when **A15** and **A14** are LOW and **A13** is HIGH, generating **CS2 bar**, placing it in the address map from 4000H to 7FFFH. The IEEE-488 controller is selected when **A15**, **A14**, **A13** and **A12** are all LOW to generate **CS3 bar** and using **A0**, **A1** and **A2** to select internal registers to place the controller between address 0000H and 0007H.

Data is read serially from the CPU board and after every eight bits is converted into a byte of data which is sent to the IEEE-488 controller, U5. The controller operates all IEEE-488 control lines automatically and the data is put out onto the bus as eight parallel bits as **IB0 bar - IB7 bar**. The data and control lines are buffered and inverted through U6 and U7 and the data is then passed to the GPIB connector, CON4, as **DIO0 - DIO7**. When data is received by the controller the **IRQ bar** line is pulled LOW by the controller and the CPU reads the data byte from the controller data bus. This is converted to serial data and passed to the CPU board via the serial link, CON1.

When the GPIB interface is addressed correctly the CPU pulls port 17, U1 pin 20, HIGH so that the output of U9-A goes HIGH. This turns ON LED1, which situated on the rear panel, and the current through LED1 is limited by R4.

3.7.1. GP500A IEEE-488 Signal Directory

A0-A7	CPU lower address bus
A8-A15	CPU upper address bus
AS	Address strobe output from the processor
CS1 bar	EPROM chip select line
CS2 bar	RAM chip select line
CS3 bar	IEEE-488 controller chip select line
CTS bar	Serial link clear to send line
D0 - D7	CPU data bus
D0/A0 - D7/A7	Multiplexed address/data lines from the processor
DIO0 - DIO7	Buffered and inverted IEEE controller data lines
IB0 bar - IB7 bar	IEEE controller data lines
IRQ bar	IEEE controller interrupt lines
RESET bar	Board reset line
RTS bar	Serial link ready to send line
RXD	Serial link data receive line
TXD	Serial link data transmit line
+5V	5 volt supply line
0V	Ground line

Section 4 - Parts Lists

4.1. PCB Assembly Main

Consisting of: Resistors

Ref	Description	Part No	Ref	Description	Part No
R1	470RJ W25 CF	23185-1470	*RP21	1K X 4S SIL	23301-9108
R2	10MJ W25 CF	23185-6100	*RP22	1K X 4S SIL	23301-9108
R3	10MJ W25 CF	23185-6100	*RP23	1K X 4S SIL	23301-9108
R4	470RJ W25 CF	23185-1470	*RP24	1K X 4S SIL	23301-9108
R5	470RJ W25 CF	23185-1470			
R6	470RJ W25 CF	23185-1470			
R7	10KJ W25 CF	23185-3100			
R8	10KJ W25 CF	23185-3100			
R9	47RJ W25 CF	23185-0470			
R10	47RJ W25 CF	23185-0470	VR1	10K Vert CF	23347-9206
R11	47RJ W25 CF	23185-0470			
R12	470RJ W25 CF	23185-1470			
R13					
to					
R16	Not used				
R17	10KJ W25 CF	23185-3100	C1	10PG 100V Cer	23428-0100
R18	10KJ W25 CF	23185-3100	C2	10PG 100v Cer	23428-0100
R19	470RJ W25 CF	23185-1470	C3	10PG 100V Cer	23428-0100
R20	10KJ W25 CF	23185-3100	C4	33PG 100V Cer	23428-0330
R21	10KJ W25 CF	23185-3100	C5	10PG 100v Cer	23428-0100
R22	10CRJ W25 CF	23185-1100	C6	10PG 100V Cer	23428-0100
R23	33KJ W25 CF	23185-3330	C7	33PG 100V Cer	23428-0330
R24	10CRJ W25 CF	23185-1100	C8	10PG 100V Cer	23428-0100
R25	10CRJ W25 CF	23185-1100	C9	22PG 100V Cer	23428-0220
R26	100RJ W25 CF	23185-1100	C10	22PG 100V Cer	23428-0220
R27	10CRJ W25 CF	23185-1100	C11	22PG 100V Cer	23428-0220
R28	10CRJ W25 CF	23185-1100	C12	1NOK 100V Cer	23428-2100
R29	1K0J W25 CF	23185-2100	C13	INOK 100V Cer	23428-2100
R30	470RJ W25 CF	23185-1470	C14	10NZ 63V cer	23428-3100
R31	2K0J W25 CF	23187-2200	C15	10NZ 63V Cer	23428-3100
R32	150RJ W25 CF	23185-1150	C16	10UF 35V Elec	23557-0647
R33	1K2J W25 CF	23185-2120	C17	22PG 100V Cer	23428-0220
R34	150RJ W25 CF	23185-1150	C18	Not -fitted	
R35	10KJ W25 CF	23185-3100	C23	1NOK 100V Cer	23428-2100
R36	150RJ W25 CF	23185-1150	C24	10NZ	23428-3100
			C25	10NZ 63V Cer	23428-3100
RP1	1K X 4S SIL	23301-9108			
RP2	1K X 4S SIL	23301-9108	C33	1NOK 100V Cer	23428-2100
RP3	1K X 4S SIL	23301-9108	C34	10NZ 63V Cer	23428-3100
RP4	1K X 4S SIL	23301-9108	C35	10NZ 63V Cer	23428-3100
RP5	Not used				
RP6	1K X 8 SIL	23301-9109	CD1		
			to		
RP7	47R X 4S SIL	23301-9103	CD87	10NZ 63V Cer	23428-3100
RP8	47R X 4S SIL	23301-9103	CD88		
			&		
RP9 &			CD89	Not used	
RP10	Not used		CD90	10NZ 63V Cer	23428-3100
RP11	1K X 4S SIL	23301--9108	CD91	10NZ 63V Cer	23428-3100
RP12	1K X 4S SIL	23301--9108			
RP13	1K X 4S SIL	23301-9108			
RP14	1K X 4S SIL	23301-9108			

Semiconductors

Ref	Description	Part No	Ref	Description	Part No
IC1	74AC161	27234-1610	IC59	74AC74	27234-0740
IC2	74AC161	27234-1610	IC60	74AC74	27234-0740
IC3	74AC161	27234-1610	IC61	74AC20	27234-0200
IC4	74AC161	27234-1610	IC62	74AC04	27234-0040
IC5	74HC14	27231-0140	IC63	74AC02	27234-0020
IC6	74AC574	27234-5740	IC69	74AC04	27234-0040
IC7	74AC574	27234-5740	IC70	74PC20	27234-0200
ICB	74AC14	27231-0140	IC71	74AC20	27234-0200
IC9	74AC574	27234-5740	IC72	74AC161	27234-1610
IC10	74AC574	27234-5740	IC73	74AC161	27234-1610
IC11	8KX8 RAM 81C78	27241-9204	IC74	74AC20	27234-0200
IC12	8KX8 RAM 81C78	27241-9204	IC105	74HC14	27231-0140
IC13	74AC245	27254-2450	IC106	74AC574	27234-5740
IC14	74AC574	27234-5740	IC107	74AC574	27234-5740
IC15	74PC245	27234-2450	IC108	74HC14	27231-0140
IC16	74AC574	27234-5740	IC109	74AC574	27234-5740
IC17	74AC02	27234-0020	IC110	74AC574	27234-5740
IC18	74S289	27241-9301	IC111	8KX8 RAM 81C78	27241-9204
IC19	74S289	27241-9301	IC112	8KX8 RAM 81C78	27241-9204
IC20	74S289	27241-9301	IC113	74AC245	27234-2450
IC21	74S289	27241-9301	IC114	74AC574	27234-5740
IC22	74HC670	27241-9302	IC115	74AC245	27234-2450
IC23	74HC670	27241-9302	IC116	74AC574	27234-5740
IC24	74AC161	27234-1610	IC117	Not used	
IC25	74AC161	27234-1610	IC118	74S289	27241-9301
IC26	74AC161	27234-1610	IC119	74S289	27241-9301
IC27	74AC161	27234-1610	IC120	745289	27241-9301
IC28	74HC164	27231-1640	IC121	748289	27241-9301
IC30	74AC32	27234-0320			
IC31	74AC32	27234-0320	IC205	74HC14	27231-0140
IC32	74F38	27224-0380	IC206	74AC574	27234-5740
103	74AC04	27234-0040	IC207	74AC574	27234-5740
IC34	74AC32	27234-0320	IC208	74HC14	27231-0140
IC35	74AC32	27234-0320	IC209	74AC574	27234-5740
106	74AC74	27234-0740	IC210	74AC574	27234-5740
IC37	74AC161	27234-1610	*IC211	8KX8 RAM 81C78	27241-9204
IC38	74AC161	27234-1610	*IC212	8KX8 RAM 81C78	27241-9204
IC39	74F521	27224-5210	*IC213	74AC245	27234-2450
IC40	74HC670	27241-9302	IC214	74AC574	27234-5740
IC41	74HC670	27241-9302	*IC215	74AC245	27234-2450
IC42	74AC161	27234-1610	IC216	74AC574	27234-5740
IC43	74HC670	27241-9302			
IC44	74AC161	27234-1610	*IC218	74S289	27241-9301
IC45	74AC161	27234-1610	*IC219	74S289	27241-9301
IC46	74HC164	27231-1640	*IC220	74S289	27241-9301
IC47	74AC02	27234-0020	*IC221	74S289	27241-9301
IC48	74AC02	27234-0020			
IC49	6303X	27240-9404	*IC305	74HC14	27231-0140
IC50	27C64	27242-9105	*IC308	74HC14	27231-0140
IC51	6821	27240-9806			
IC52	74HC138	27231-1380	* Not fitted on LA3200		
IC53	74HC138	27231-1380			
IC54	74HC390	27231-3900			
IC55	74HC151	27231-1510			
IC56	74AC02	27234-0020			
IC57	74HC164	27231-1640			
IC58	74HC164	27231-1640			

Other Parts on Main PCB Assy

Description	Part No
Header 36 Way right angle latched 3 off (Con1,2,3)	22574-9303
Header 20 Way right angle latched (Con4)	22574-9304
Header 6 Way 0.156 (Con5)	22573-9116
Header 8 Way Dual cut from 2 off (Con6,7)	22573-9115
Header 4 Way SIL cut fm 3 off (Con8,9,10)	22573-9110
Skt DIL 14 pin 38 off	22574-0119
Skt DIL 16 pin 36 off	22574-0120
Skt DIL 20 pin 25 off	22574-0141
Skt DIL 28 pin 22574-0122	
Skt DIL 28 pin/0.3 6 off	22574-9110
Skt DIL 40 pin 22574-0125	
Xtal 8MHz (X1) 28500-9008	
Xtal 25MHz (X2) 28500-9009	
Xtal 20MHz (X3) 28500-9002	
PCB 35565-9170	
Skt LA3200 31512-9100*	
	* Not fitted on LA4800

4.2. PCB Assy CPU Board

Consisting of:

Resistors			Semiconductors (cont)		
Ref	Description	Part No	Ref	Description	Part No
R1	220RJ W25 CF	23185-1220	IC1	6303	27240-9404
R2	220RJ W25CF	23185-1220	IC2	6255	27268-9601
R3	10MJ W25 CF	23185-6100	IC3	6850	27240-9807
R4	10KJ W25 CF	23185-3100	IC4	27C512	27242-9110
R5	220RJ W25 CF	23185-1220	IC5	32K X 8 RAM	27241-9203
R6	220RJ W25 CF	23185-1220	IC6	32K X 8 RAM	27241-9203
R7	4K7J W25 CF	23185-2470	IC7	74HC138	27231-1380
R8	1K0J W25 CF	23185-2100	IC8	74HC4078	27230-0780
R9	10KJ W25 CF	23185-3100	IC9	32K X 8 RAM	27241-9203
R10	4K7J W25 CF	23185-2470	IC10	74HCT245	27229-2450
R11	100KJ W25 CF	23185-4100	IC11	74HC161	27231-1610
R12	1K0J W25 CF	23185-2100	IC12	TL072	27106-0618
R13	10KJ W25 CF	23185-3100	IC13	74HC32	27231-0320
			IC14	74HC08	27231-0080
RP1	10K X 8 SIL	23301-9102	IC15	74HC138	27231-1380
RP2	10K X 4S SIL	23301-9104	IC16	Not used	
RP3	10K X 4S SIL	23301-9104	IC17	74HC00	27231-0000
RP4	10K X 4S SIL	23301-9104			
RP5	10K X 4S SIL	23301-9104			
Capacitors			Other Parts Processor PCB Assy		
Ref	Description	Part No	Description	Part No	
C1	47U 10V Elec	23557-0611	Skt 9 Way right angle D (Con 1)	22572-9205	
C2	33PG 100v Cer	23428-0330	Header 7 Way out (Con 2)cut from	22573-9703	
C3	22PG 63V Cer	23428-0220	Header 16 Way dual, (Con 3)cut from	22573-9115	
C4	22PG 63V Cer	23428-0220	Header 16 Way latching (Con 4)	22573-0060	
C5	10PG 100v Cer	23428-0100	Header 34 Way dual (Con 5)cut from	22573-9115	
C6	10PG 100v Cer	23428-0100	Skt DLL 24 pin	22574-0139	
C7	22LJ 16V Elec	23557-0644	Skt DLL 28 pin 4 off	22574-0122	
C8	33PG 100v Cer	23428-0330	Buzzer	28151-9001	
CD1	To		Xtal 1 , 8MHz	28500-9008	
CD18	10NM 100V Cer	23428-3100	Xtal 2, 4.9152MHz	28500-9007	
			PCB	35565-9160	
Semiconductors					
Ref	Description	Part No			
			Battery 2.4V	22010-9101	
D1	1N4148	25021-0901			
D2	1N4148	25021-0901			
D3	1N4148	25021-0901			
D4	1N4148	25021-0901			
D5	1N4148	25021-0901			
D6	1N4148	25021-0901			
Q1	ZTX239	25380-9251			
Q2	ZTX239	25380-9251			
Q3	ZTX239	25380-9251			
Q4	ZTX214	25341-9200			
Q5	ZTX214	25341-9200			
Q6	ZTX239	25380-9251			
Q7	ZTX239	25380-9251			

4.3. PCB Assy Keyboard & PSU

Consisting of:

Resistors

Ref	Description	Part No	Semiconductors		
Ref	Description	Part No	Ref	Description	Part No
R1	R027 350-8	23315-9004	D1	1N4003	25115-9001
R2	22RJ W25 CF	23185-0220	D2	1N4148	25021-0901
R3	1K00F W25 MF	23202-2100	D3	IN4003	25115-9001
R4	82K0F W25 MF	23202-3820	D4	1N4003	25115-9001
R5	1KSJ W25 CF	23185-2150	D5	1N4148	25021-0901
R6	47K0F W25 MF	23202-3470	D6	1N4148	25021-0901
R7	1K00F W25 MF	23202-2100	D7	1N4148	25021-0901
R8	47KJ W25 CF	23185-3470	ZD1	ZN404	27161-0120
R9	2K20F W25 MF	23202-2220	Q1	TIP42A	25386-9303
R10	2K20F W25 MF	23202-2220	Q2	TIP32A	25386-9301
R11	2K20F W25 MF	23202-7770	Q3	ZTX750	25384-9001
R12	22KJ W25 CF	23185-3220	Q4	ZTX750	25384-9001
R13	2K20F W25 MF	23202-2220	SR1	KBU4A	25211-9404
R14	10KJ W25 CF	23185-3100	BR2	W01M	25211-9302
R15	1M0J W25 CF	23185-5100	IC1	LM324	27106-0512
R16	10KJ W25 CF	23185-3100	IC2	78L05	27160-0011
R17	10KJ W25 CF	23185-3100	IC3	LM317LZ	27160-0230
R18	100RJ W25 CF	23185-1100			
R19	220RJ W25 CF	23185-1220			
R20	4K7J W25 CF	23185-2470			
R21	390RJ W25 CF	23185-1390			
R22	2K2J W25 CF	23185-2220			

Other Parts Processor PCB Assy		
	Description	Part No
LK1	Zero Ohm	23185-0000
LK2	Zero Ohm	23185-0000
LK3	Zero Ohm	23185-0000
LK4	Zero Ohm	23185-0000
TH1	Thermistor VA1106	23388-9102
PR1	470R CF PS/H	23377-1470
PR2	2K2 CF PS/H	23377-2220
VR1	10K CF Pot	23347-9204

Capacitors

Ref	Description	Part No		
C1	10000U 16V Elec	23557-9117	2 Way Rt ang locking header	22573-9119
C2	470U 16V Elec	23557-0615	Polarising Key	22573-9570
C3	100U 50V Elec	23557-0610	Bracket, heatsink	31531-9650
C4	470U 16V Elec	23557-0615	Cable Assy, Keyboard	43185-9120
C5	470U 16V Elec	23557-0615	PCB -	35515-9180
C6	1U0 50V Elec	23557-0612	Keyboard/PSU	
C7	1U0 50V Elec	23557-0612		
C	On inverter PCB			
	47U 10V Elec	23557-0611		

Front Panel Assy consisting of:		Chassis Assy Consisting of:	
Description	Part No	Description	Part No
Front Moulding	33562-9500	Chassis	31567-9090
Display Window	31335-9080	Foot, self adhesive	20662-9301
Display Bracket	33111-9040	4 off	
Board Support	33562-9510	Cable Assy PCB	43185-9100
Moulding		Cable Assy	43185-9110
LCD Module	43601-9020	Display	
LCD Backlight	43601-9030	Skt 2 Way 0.1 IDC	22573-9540
Header SIL Cut from	22573-9703	Spacer Hex M3 x 8	20661-0238
Spacer Hex M3 x 3 off	20661-0238	Spacer 2" plastic	20661-9404
Screw M3 x 5mmL	20234-0017	Washer M3 spring	20038-9501
Screw M3 x 8mmL	20234-0012	Washer M3 s/proof	20037-0301
Screw No 4 x 3/8"	20062-9801	Screw No 4 x 3/8"	20062-9301
Screw No 4 x 3/4"	20062-9309	Screw No 6 x 1/2"	20062-9308
Screw No 4 x 0.25" plastite	20073-9801	Screw M3 x 8	20234-0012
Washer M3 spring	20038-9501	Screw M3 x 5	20234-0017
Washer M3 plain	20030-0263	Screw M4 x 8	20234-0023
Washer M3 s/proof	20030-0301	Screw M3 x 5 black	20234-9401

Rear Panel Assy consisting of:		Case Parts consisting of:	
Description	Part No	Description	Part No
Rear Panel	31567-9110	Cover, grey	31567-9100
Transformer	43751-9130	Handle, left	47311-9010
Spacing Plate (transformer)	31332-9090	Handle, right	47311-9020
Screwlock D Type	2 off	Extrusion, handle	47311-9040
Mains input	22538-9403	Label Made in England	37522-0150
IEC Skt		Label LA4800 Logo or	37535-9370
Boot, insulating	22538-9404	Label LA3200 Logo	37535-9380
Switch, rocker DPST	22219-9301	Label LA4800 Skt or	37541-9200
D Connector Assy	43185-9090	Label LA3200 Skt	37541-9220
Blanking plate	31334-9080	Label Ser No	37522-0160
IEEE		Label Volt/Fuse Rating	37541-0680
Foot, instrument	4 off		
Spacer Hex M3 x 8	20661-0238		
Spacer Hex M3.5 x 12	20661-9110		
Wire Set	10190-9134	Packaging Parts	

consisting of:

			Description	Part No
Washer M3 spring	7 off	20038-9501		
Washer M4 spring	5 off	20038-9502	Poly bag, box type	10615-9402
Washer 4BA plain	8 off	20030-9101	Poly bag, for mains lead	10615-9301
Solder tag 6BA s/proof		20037-0400	Carton	38114-9090
Nut 4BA	5 Off	20100-9201	Left carton cheek	38614-9270
Screw 4BA x 5/8	4 off	20134-9008	Right carton cheek	38614-9280
Nut M3	9 off	20210-0101	Instruction Book	48583-0570
Screw M3 x 8	9 off	20234-0012	Mains Lead (for 240V) or	22491-0010
Screw M3 x 5	8 off	20234-0017	Mains Lead (for 220V) or	22491-0020
Screw M3.5 x 30	4 off	20234-9012	Mains Lead (for 110V)	22491-0040
Screw M3.5 x 6	4 off	20234-9013		
Screw No 4 x 1/4" Plastite	2 off	20073-9801		
Bush. T0220	2 off	20611-9304		
Cable tie	2 off	20653-0204		
Fuse 500mA(220/240) or	2 off	22315-9504		
Fuse 1A (110V)	2 off	22315-9501		

4.4. AP01 Pod

consisting of:
PCB ASSY AP01 **45713-9100**

Resistors			Other parts on PCB Assy		
Ref	Description	Part No	Description	Part No	
R1	100KJ W25 CF	23185-4100	Header 40 Way Rt ang (PJ1)	22573-0049	
R2	47RJ W25 CF	23158-0470	Header SIL (PJ5,6) cut from	22573-9110	
R3	47RJ W25 CF	23185-0470	Skt DIL 20 pin 5 off	22574-0141	
R4	100RJ W25 CF	23185-1100	Skt PJL 28 pin	22574-9112	
R5	100RJ W25 CF	23185-1100	Spacer, patch board 4 off	33562-9110	
R6	1K0J W25 CF	23185-2100	Cable Assy 34 way	43185-9130	
R7	47RJ W25 CF	23185-0470	Cable Assy 20 way	43185-9140	
R8	47RJ W25 CF	23185-0470	PCB	35565-9140	
R9	1K0J W25 CF	23185-2100			
RP1	To				
RP8	100R x 8 DIL	23330-9001			
RP9	10K x 4S SIL	23301-9104			
RP10	47R x 4S SIL	23301-9103			
RP11	1M0 x 8 SIL	23301-0404			
RP12	47R x 4S SIL	23301-9103			
RP13	To				
RP16	1M0 x 8 SIL	23301-0404			
Capacitors			Casing and Packaging Parts		
Ref	Description	Part No	Description	Part No	
C1	10NZ 63V cer	23428-3100	Case Set	33561-9040	
C2	680PK 100V cer	23428-1680	Front Panel	31333-9010	
CD1	10NZ 63V cer	23428-3100	Rear Panel	31333-9030	
CD7	to		Label - AP01	37535-9420	
CD15	10NZ 63V cer	23428-3100	Label Cable Set	37541-9260	
Semiconductors			Cable Assy 40 way	46713-9101	
Ref	Description	Part No	Instruction Leaflet	48583-0610	
Q1	ZTX239	25380-9251	Carton & Insert	38210-9010	
Q2	ZTX214	25341-9200			
IC1	Not fitted				
IC2	74HC393	27231-3930			
IC3	74HC393	27231-3930			
IC4	74ACT573	27232-5730			
IC5	To				
IC8	74HCT573	27229-5730			
IC11	74HC165	27231-1650			

4.5. AP02 Pod**consisting of:****PCB Assy AP01 - See detail in 4.4 plus PCB Assy AP02****PCB ASSY AP02****45713-9370****Resistors****Other parts on PCB Assy**

Ref	Description	Part No	Description	Part No
R1	10KJ W25 CF	23185-3100	Header 26W Rt Ang (PJ1)	22573-0042
R2	100RJ W25 CF	23185-1100	Header SIL (PJ3,4) cut from	22573-0042
R3	10KJ W25 CF	23185-3100	Cable Assy 34 way	43185-9130
R4	10KJ W25 CF	23185-3100	PCB	35555-1620

RP1 To

RP4 100R x8 DIL 23330-9001

Casing and Packaging Parts

Ref	Description	Part No
RP5	1M0 x8 SIL	23301-0404
RP6	1M0 x8 SIL	23301-0404

Description	Part No
Case Set	33561-9040
Front Panel	31333-9070
Rear Panel	31333-9030

Capacitors

Ref	Description	Part No	Description	Part No
C1	47U 16V Elec	23557-0631	Spacer Hex M3 x 8 2 off	20661-0238
C2	To		Screw M3 x 5mm 4 off	20234-0017
C4	100NK 63V P/E	23620-0246	Screw M2 x 16mm 2 off	20234-0035
			Washer M3 spring 4 off	20038-9501
			Nut M2 2 off	20210-0100

Semiconductors

Label - AP02 37538-2210

Ref	Description	Part No	Description	Part No
Q1	BC559	25341-0214	Cable Assy 40 way	46713-9101
Q2	BC549	25380-0229	Cable Assy 20 way	46713-9371
IC1	74HCT573	27229-5730	Instruction Leaflet	48583-0620
IC2	74HCT573	27229-5730	Carton & Insert	38210-9010

4.6. AP03 Pod

consisting of:
PCB Assy AP03 **45713-9150**

Resistors			Semiconductors		
Ref	Description	Part No	Ref	Description	Part No
R1	47RJ W25 CF	23185-0470	IC6	74AC86	27234-0861
R2	Not Used		IC7	to	
R3	470RJ W25 CF	23185-1470	IC10	74AC112	27234-1120
R4	47RJ W25 CF	23185-0470	IC11	74AC574	27234-5740
R5	47RJ W25 CF	23185-0470	IC12	74AC574	27234-5740
R6	Not used		IC13	74HC540	27231-5400
R7	200RJ W25 CF		IC14	74HC540	27231-5400
		23187-1200	IC15	74AC574	27234-5740
RP1	100R x 8 DIL	23330-9001	IC16	74AC574	27234-5740
RP2	100R x 8 DIL	23330-9001	IC17	To	
RP3	To		IC19	74AC174	27234-1740
RP6	47R x 4S SIL	23301-9103	IC20	74AC08	27234-0080
RP7	100K x 8 SIL	23301-9101	IC21	74AC08	27234-0080
RP8	100K x 8 SIL	23301-9101	IC24	To	
			IC26	74ACT04	27232-0040
VR1	To				
VR3	470R preset	23376-9004			
Capacitors			Other Parts Processor PCB Assy		
Ref	Description	Part No	Description	Part No	
C1	To		Header 10 Way Rt ang (PJ2,3)2 off	22573-0049	
C3	47PG 100v Cer	22573-9110	Skt DIL 14 pin 3 off	22574-0019	
C4	To		Cable Assy 34 way 2 off	43185-9130	
C6	10NZ 63V cer	23427-9215	PCB	35565-9150	
CD1	To		Casing and packaging parts		
CD5	10NZ 63V cer	23427-9215	Description	Part No	
CD7	10NZ 63V cer	23427-9215	Case Set	33561-9040	
CD11	To		Front Panel	31333-9020	
CD16	10NZ 63V cer	23427-9215	Rear Panel	31333-9040	
CD18	To		Label - AP03	37535-9430	
CD22	10NZ 63V cer	23427-9215	Cable Assy 10 way 2 off	46713-9151	
CD24	To		Instruction Leaflet	48583-0630	
CD27	10NZ 63V cer	23427-9215	Carton & Insert	38210-9010	
Semiconductors					
Ref	Description	Part No			
IC1	To				
IC3	Not used				
IC4	74AC574	27234-5740			
IC5	74AC86	27234-0861			

4.7. AP03V Pod**Consisting of:****PCB Assy AP03V Upper 45713-9160**

Resistors			Resistors (cont)			
Ref	Description	Part No	Ref	Description	Part No	
R1	68K0F W125	MF	23201-3680	R86	56K0F W25 MF	23202-3560
R2	39K0F W125	MF	23201-3390	R87	68K0F W25 MF	23202-3680
R3	68K0F W125	MF	23201-3680	RP1	47R x 8 DIL	23301-0610
R4	39K0F W125	MF	23201-3390	RP2	47R x 8 DIL	23301-0610
R5	39K0F W125	MF	23201-3390			
R6	68K0F W125	MF	23201-3680	VR1	To	
R7	39K0F W125	MF	23201-3390	VR4	200R PS/H Cermet	23376-9602
R8	68K0F W125	MF	23201-3680	VR5	47K PS/H Cermet	23382-3470
R9	68K0F W125	MF	23201-3680	VR6	47K PS/H Cermet	23382-3470
R10	39K0F W125	MF	23201-3390			
RH	68K0F W125	MF	23201-3680		Capacitors	
R12	39K0F W125	MF	23201-3390			
R13	39K0F W125	MF	23201-3390	Ref	Description	Part no
R14	68K0F W125	MF	23201-3680	C1	100NM 63V Cer SM	23461-0010
R15	39K0F W125	MF	23201-3390	C2	To	
R16	68K0F W125	MF	23201-3680	C4	1N0K 100v Cer	23427-0254
R17	68K0F W125	MF	23201-3680	C5	100NM 63V Cer SM	23461-0010
R18	39K0F W125	MF	23201-3390	C6	100NK 63V P/E	23620-0246
R19	68K0F W125	MF	23201-3680	C7	2U2 63V Elec	23557-0500
R20	39K0F W125	MF	23201-3390	C8	100NM 63V Cer SM	23461-0010
R21	39K0F W125	MF	23201-3390	C9	2U2 63V Elec	23557-0500
R22	68K0F W125	MF	23201-3680	C10	2U2 63V Elec	23557-0500
R23	39K0F W125	MF	23201-3390	C11	100NM 63V Cer SM	23461-0010
R24	68K0F W125	MF	23201-3680	C12	1N0K 100v Cer	23427-0254
R25	68K0F W125	MF	23201-3680	C13	To	
R26	39K0F W125	MF	23201-3390	C16	100NM 63V Cer SM	23461-0010
R27	68K0F W125	MF	23201-3680	C17	47U 100 Elec	23557-0510
R28	39K0F W125	MF	23201-3390	C18	2U2 63V Elec	23557-0500
R29	39K0F W125	MF	23201-3390	C19	47U 10V Elec	23557-0510
R30	68K0F W125	MF	23201-3680	C20	47U 10V Elec	23557-0510
R31	39K0F W125	MF	23201-3390	C21	To	
R32	68K0F W125	MF	23201-3680	C36	3P9C 63V Cer	23427-0356
R65	1K0J W25	CF	23185-2100	C37	100NM 63V Cer SM	23461-0010
R66	1K0J W25	CF	23185-2100	C38	100NM 63V Cer BM	23461-0010
R67	3K90F W25	MF	23202-2390	C41	47U 10V Elec	23557-0510
R68	1K0J W25	CF	23185-2100			
R69	10K0F W25	MF	23202-3100			
R71	560KF W25	MF	23202-4560		Semiconductors	
R72	47K0F W25	Mf	23202-3470			
R73	4K7J W25	CF	23185-2470	Ref	Description	Part No
R74	15KJ W25	CF	23185-3150			
R75	47K0F W25	MF	23202-3470	D1	ZN404	27161-0120
R76	47K0F W25	MF	23202-3470			
R77	220KF W25	MF	23202-4220	Q1	ZTX750	25384-9001
R78	100KF W25	MF	23202-4100	Q2	ZTX750	25384-9001
R79	68K0F W25	MF	23202-3680			
R80	220KF W25	MF	23202-4220	IC1	To	
R81	68K0F W25	MF	23202-3680	IC4	74AC11032	27236-0320
R82	22KJ W25	CF	23185-3220	IC5	74ACT541	27232-5410
R83	22KJ W25	CF	23185-3220	IC6	74ACT541	27232-5410
R84	220KJ W25	CF	23185-4220	IC7	LM324	27106-0506
R85	100KJ W25	CF	23185-4100	IC8	74HC4053	27230-0530

Other Parts on PCB Assy AP03 Upper

Ref	Description	Part No
	Header 34way Rt ang (PJ1,2) 2 off	22575-0008
	SKT 5 way SIL cut from	22574-0140
	TP1 cut from	22573-0041
	PCB	35555-1640

PCB Assy AP03V Lower 45713-9170**Consisting of:****Resistors**

Ref	Description	Part No	Semiconductors (cont)	Ref	Description	Part No
R1	47RJ W25 CF	23185-0470	IC1	To		
R3	470RJ W25CF	23185-1470	IC3	Not used		
R4	47RJ W25 CF	23185-0470	IC4	74AC575		
R5	47RJ W25 CF	23185-0470	IC5	74AC86	27234-0861	
			IC6	74AC86	27234-0861	
RP3	To		IC7	To		
RP6	47R x4S SIL	23301-9103	IC10	74AC112	27234-1120	
VR1	To		IC11	74AC574	27234-5740	
VR3	470R Preset	23376-9004	IC12	74AC574	27234-5740	

Capacitors

Ref	Description	Part No	Ref	Description	Part No
C1	To		IC15	74AC574	27234-5740
C3	47PG 100V cer	23427-9215	IC16	74AC574	27234-5740
C4	To		IC17	To	
C6	10NZ 63V cer	23427-9215	IC19	74AC174	27234-1740
CD1	To		IC20	74AC08	27234-0080
CD5	10NZ 63V cer	23427-9215	IC21	74AC08	27234-0080
CD7	To		IC24	To	
CD11	10NZ 63V cer	23427-9215	IC26	74ACT04	27234-0040
CD16	10NZ 63V cer	23427-9215			
CD18	To				
CD22	10NZ 63V cer	23427-9215			

Casing and Packaging Parts**Description Part No**

CD24	To	Case set	33561-9040
CD27	10NZ 63V cer	Front Panel	31333-9060
		Rear Panel	31333-9040
		Washer M3 spring 4 off	20038-9501

Other Parts on PCB Assy AP03V Lower

Description	Part No	Description	Part No
Header 10 Way Rt ang (PJ2,3) 2 off	22573-0049	Spacer M3 x 10mm 4 off	20661-0222
Header (PJ4) 5 Way SIL cut from	22573-9110	Adhesive foam strip cut from	10366-9801
Skt DIL 14 pin 3 off	22574-0019	Label - AP03V	37538-2220
Cable Assy 34 way 2 off	43185-9130	Cable Assy 10 way 2 off	46713-9151
PCB	35565-9150	Instruction Leaflet	48583-0640
		Carton & Insert	38210-9010

4.8. AP04 Pod

Consisting of:

PCB Assy AP04	45713-9200	Other Parts on PCB Assy AP04V Upper		
Resistors		Description		
Ref	Description	Part No		
RP2	100R x 8 DIL	23330-9001		
RP3	47R x 4 SIL	23301-9103		
RP4	47R x 4 SIL	23301-9103		
RP8	100K x 8 DIL	23301-9101		
		Res Zero ohm 4 off (LK1,2,3,4)		
		Header 10 way (PJ3)		
		Header 5 way Cut from SIL(PJ4)		
		Skt DIL 14 pin		
		Cable Assy 20 way		
		PCB		
		2 off		
		43185-9140		
		35565-9150		
Capacitors		Case and Packaging Parts		
Ref	Description	Part No		
C4 to		23427-9215		
C6	10NZ 63V cer	23427-9215		
CD6	10NZ 63V cer	23427-9215		
CD15	10NZ 63V cer	23427-9215		
CD22	10NZ 63V cer	23427-9215		
		Case set		
		Front Panel		
		Rear Panel		
		Label - AP04		
		Cable Assy 10 way		
		Instruction Leaflet		
		33561-9040		
		31333-9060		
		31333-9040		
		37538-2220		
		46713-9151		
		48583-0640		
Semiconductors				
Ref	Description	Part No	Description	Part No
IC13	74AC540	24234-5400	Carton & Insert	38210-9010
IC25	74ACT04	27232-0040		
IC26	74ACT04	27232-0040		

4.9. AP04V Pod**Consisting of:**

PCB Assy AP04V Upper	45113-9200	Capacitors			
Resistors		Ref	Description	Part No	
Ref	Description	Part No	Ref	Description	
R1	to		C1	Not fitted	
R16	Not fitted		C2	To	
R17	68K0F W125 MF	23201-3680	C4	1N0K 100v Cer	23427-0254
R18	39K0F W125 MF	23201-3390	C5	Not Fitted	
R19	68K0F W125 MF	23201-3680	C6	100NK 63V P/E	23620-0246
R20	39K0F W125 MF	23201-3390	C7	2U2 63V Elec	23557-0500
R21	39K0F W125 MF	23201-3390	C8	100NM 63V Cer SM	23461-0010
R22	68K0F W125 MF	23201-3680	C9	2U2 63V Elec	23557-0500
R23	39K0F W125 MF	23201-3390	C10	2U2 63V Elec	23557-0500
R24	68K0F W125 MF	23201-3680	C11	100NM 63V Cer SM	23461-0010
R25	68K0F W125 MF	23201-3680	C12	1N0K 100v Cer	23427-0254
R26	39K0F W125 MF	23201-3390	C13	Not fitted	
R27	68K0F W125 MF	23201-3680	C14	Not fitted	
R28	39K0F W125 MF	23201-3390	C15	100NM 63V Cer SM	23461-0010
R65	1K0J W25CF	23185-2100	C16	100NM 63V Cer SM	23461-0010
R66	1K0J W25CF	23185-2100	C17	47U 10V Elec	23557-0510
R67	3K9CF W25MF	23202-2390	C18	2U2 63V Elec	23557-0500
R68	1K0J W25CF	23185-2100	C19	47U 10V Elec	23557-0510
R69	10K0F W25MF	23202-3100	C20	47U 10V Elec	23557-0510
R71	560KF W25MF	23202-4560	C21	to	
R72	47K0F W25MF	23202-3470	C28	Not fitted	
R73	4K7J W25CF	23185-2470	C29	to	
R74	15KJ W25CF	23185-3150	C34	3P9C 63V Cer	23427-0356
R75	47K0F W25MF	23202-3470	C35	to	
R76	47K0F W25MF	23202-3470	C37	Not fitted	
R77	220KF W25MF	23202-4220	C38	100NM 63V Cer SM	23461-0010
R78	100KF W25MF	23202-4100	C41	47U 10V Elec	23557-0510
R79	68K0F W25MF	23202-3680	Semiconductors		
R80	220KF W25MF	23202-4220	Ref	Description	Part No
R81	68K0F W25MF	23202-3680			
R82	22KJ W25CF	23185-3220			
R83	22KJ W25CF	23185-3220	D1	ZN404	27161-0120
R84	220KJ W25CF	23185-4220			
R85	100KJ W25CF	23185-4100	Q1	ZTX750	25384-9001
R86	56K0F W25MF	23202-3560	Q2	ZTX750	25384-9001
R87	68K0F W25MF	23202-3680			
RP1	Not fitted		IC1	Not fitted	
RP2	47R x 8 DIL	23301-0610	IC2	Not fitted	
			IC3	74AC11032	27236-0320
			IC4	74AC11032	27236-0320
VR1	Not fitted		IC5	Not fitted	
VR2	Not fitted		IC6	74ACT541	27232-5410
VR3	200R PS/H Cermet	23376-9602	IC7	LM324	27106-0506
VR4	200R PS/H Cermet	23376-9602	IC8	74HC4053	27230-0530
VR5	47K PS/H Cermet	23382-3470			
VR6	47K PS/H Cermet	23382-3470			

**PCB Assy AP04V Upper
(continued)**

Description		Part No
Header 16W	2 of	22575-0008
Rt ang (PJ1,2)		
Skt 5W SIL (PJ4)	Cut from	22574-0140
TP1	Cut From	22573-0041
Zero ohm resistor (LK1,2)	2 of	23185-0000
PCB		35555-1640
PCB Assy AP04V Lower		45713-9410

**Other Parts on PCB Assy AP04V
Upper**

Description		Part No
Res Zero ohm (LK1,2,3,4)	4 off	23185-0000
Header 10 way (PJ3)		22573-9305
Header 5 way SIL(PJ4) Cut from		22573-9110
Cable Assy 20 way		43185-9140
Connector Assy 16W input coupling		43185-9220
Connector Assy 16W output coupling		43185-9230
PCB		35565-9150

Resistors

Ref	Description	Part No	Casing and Packaging Parts
RP3	47R x 4S SIL		Description
RP4	47R x 4S SIL		Part No

Capacitors

Ref	Description	Part No	
C4	10NZ 63V cer	23427-9215	Washer M3 spring
C5	10NZ 63V cer	23427-9215	Screw M3 x 5mm
C6	1N0K 100Vcer	23427-0254	Spacer M3 x 10mm
CD6	10NZ 63V cer	23427-9215	Adhesive foam strip cut from
CD15	10NZ 63V cer	23427-9215	Label AP04V
CD22	10NZ 63V cer	23427-9215	Cable Assy 10 way
			Instruction
			Leaflet
			Carton and insert

Semiconductors

Ref	Description	Part No
IC13	74AC540	24234-5400
IC25	74AC04	27234-0040
IC26	74AC04	27234-0040

4.10. GP500A IEEE-488 Interface Option

Consisting of:

PCB Assy

Resistors

Ref	Description		Part No
R1	100KJ	W25 CF	23185-4100
R2	100KJ	W25 CF	23185-4100
R3	100KJ	W25 CF	23185-4100
R4	680RJ	W25 CF	23185-1680
R5	10KJ	W25 CF	23185-3100
R6	10KJ	W25 CF	23185-3100
R7	22KJ	W25 CF	23185-3220
R8	100KJ	W25 CF	23185-4100
R9	10KJ	W25 CF	23185-3100
R10	100KJ	W25 CF	23185-4100
R11	100KJ	W25 CF	23185-4100
R12	100KJ	W25 CF	23185-4100
R13	100KJ	W25 CF	23185-4100
R14	100KJ	W25 CF	23185-4100
R15	6K8J	W25 CF	23185-2680
R16	100KJ	W25 CF	23185-4100
R17	100KJ	W25 CF	23185-4100
R18	3K0J	W25 CF	23187-2300
RP1	100K	x 8 SIL	23301-9101

Capacitors

Ref	Description		Part No
C1	10UM	16V Elec	23557-9114
C2	15PG	100v Cer	23427-9206
C3	15PG	100v Cer	23427-9206
C4	47NZ	63V Cer	23424-9401
C5	220UM	10V Elec	23557-9111
C6	47NZ	63V Cer	23424-9401
C8	47NZ	63V Cer	23424-9401
C9	47NZ	63V Cer	23424-9401

Semiconductors

Ref	Description		Part No
Q1	ZXT239		25380-9251
IC1	HD6303		27240-9403
IC2	74HC373		27231-3730
IC3	27C64		27242-9105
IC4	6264		27241-9006
IC6	MC68488		27250-0420
IC7	MC3447		27250-0430
IC8	74HC00		27231-0000
IC9	74HC32		27231-0320

Section 5 – Circuit Diagrams

- Fig 1 LA4800/LA3200 CPU BOARD
- Fig 2 LA4800 MAIN PCB – SHEET 1
- Fig 3 LA4800 MAIN PCB – SHEET 2
- Fig 4 AP01: 32-CHANNEL DATA AND CLOCK POD
- Fig 5 16 CHANNEL BOARD TO CONVERT AP01 TO AP02 (48-CHANNEL DATA AND CLOCK PODS)
- Fig 6 GLITCH BOARD FCR AP03/AP03V DATA PODS
- Fig 7 UPPER VARIABLE THRESHOLD BOARD FCR AP03V DATA PODS
- Fig 8 CLOCK POD BOARD FOR AP04/AP04V CLOCK PODS
- Fig 9 UPPER VARIABLE THRESHOLD BOARD FOR AP04V CLOCK PODS
- Fig 10 GP500A IEEE-488 INTERFACE BOARD
- Fig 11 LA4800/3200 POWER SUPPLY

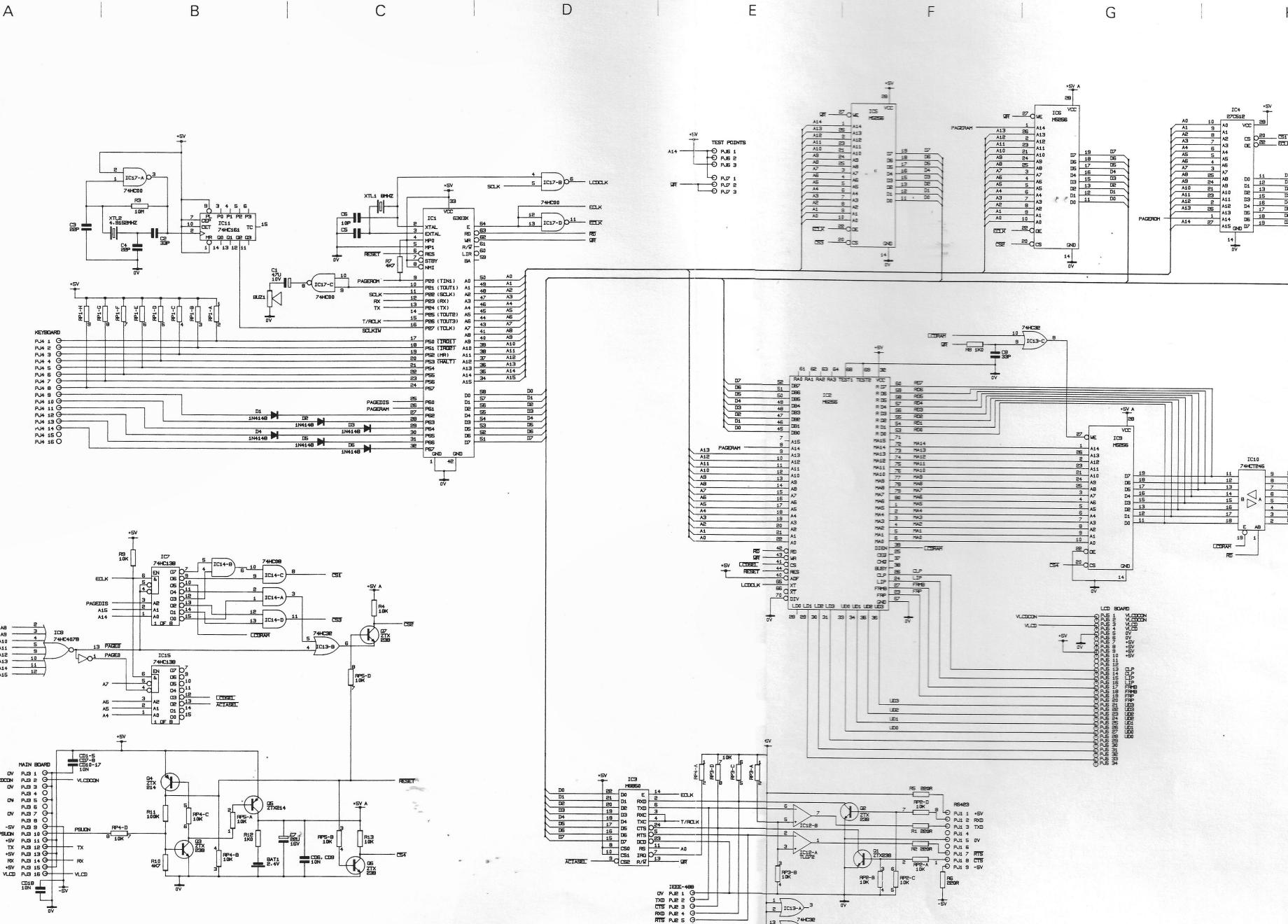


Fig 1 LA4800/LA3200 CPU BOARD

A

B

C

D

E

F

G

H

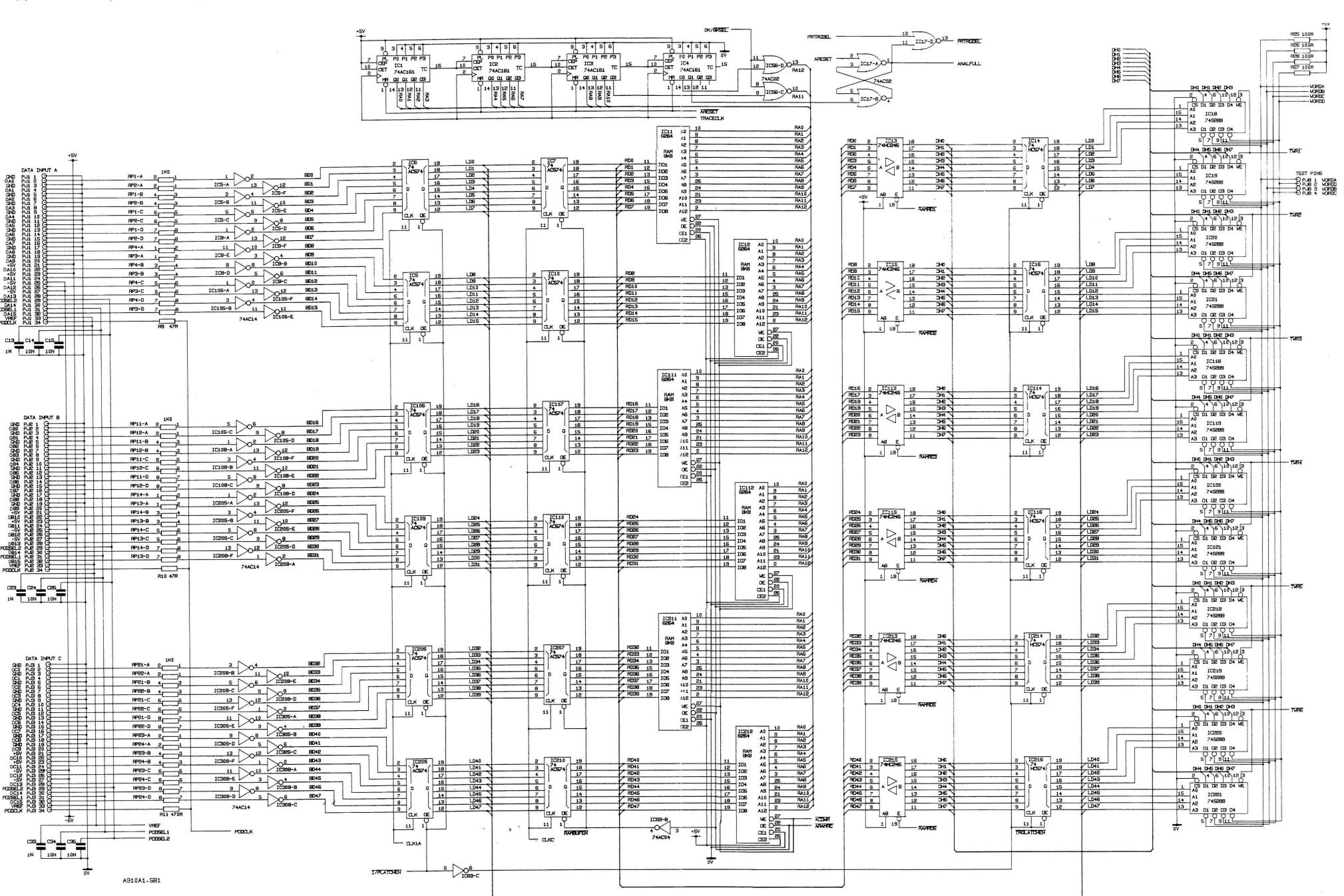


Fig 2 LA4800 MAIN PCB - SHEET 1

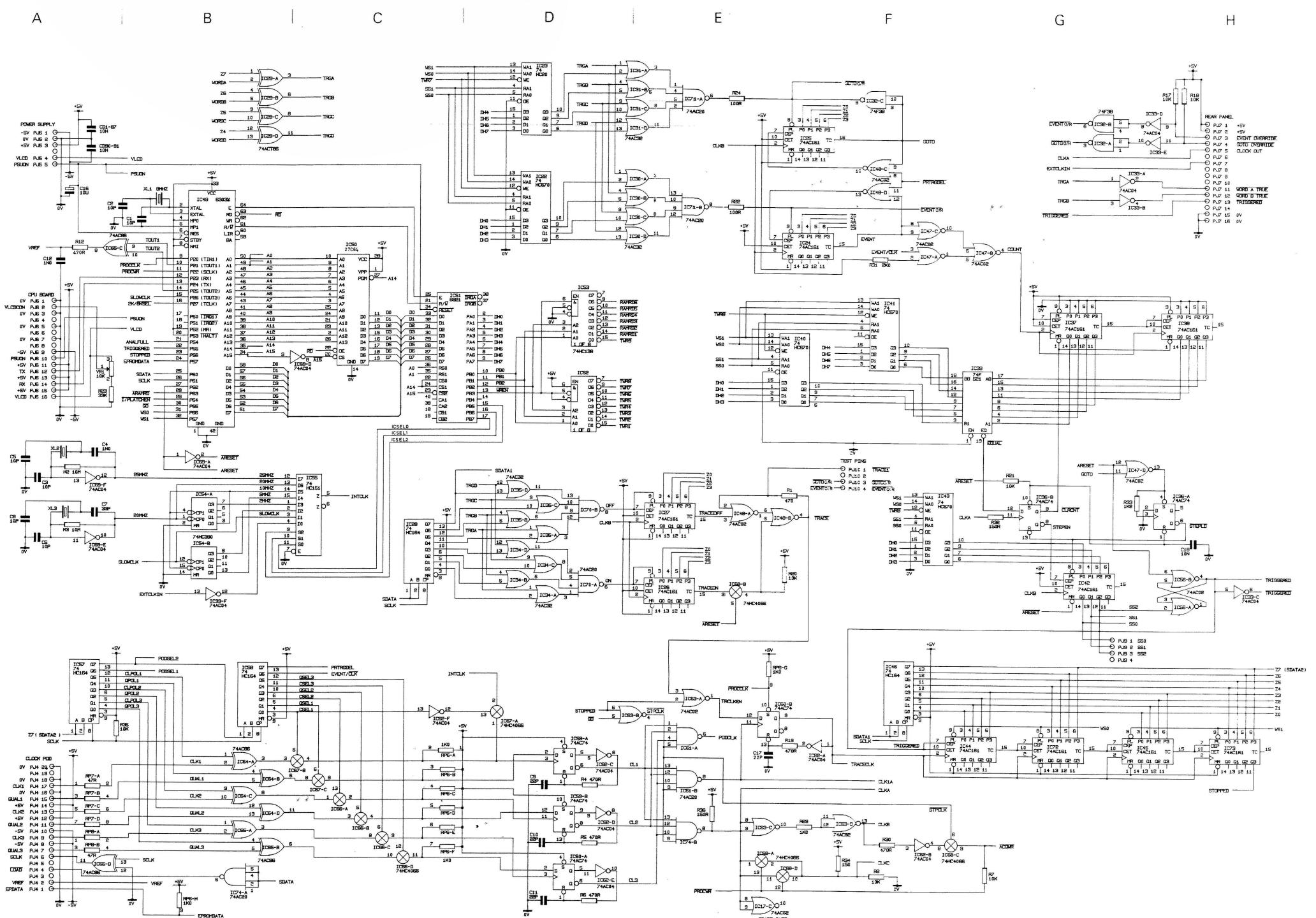


Fig 3 LA4800 MAIN PCB - SHEET 2

A

B

C

D

E

F

1

2

3

4

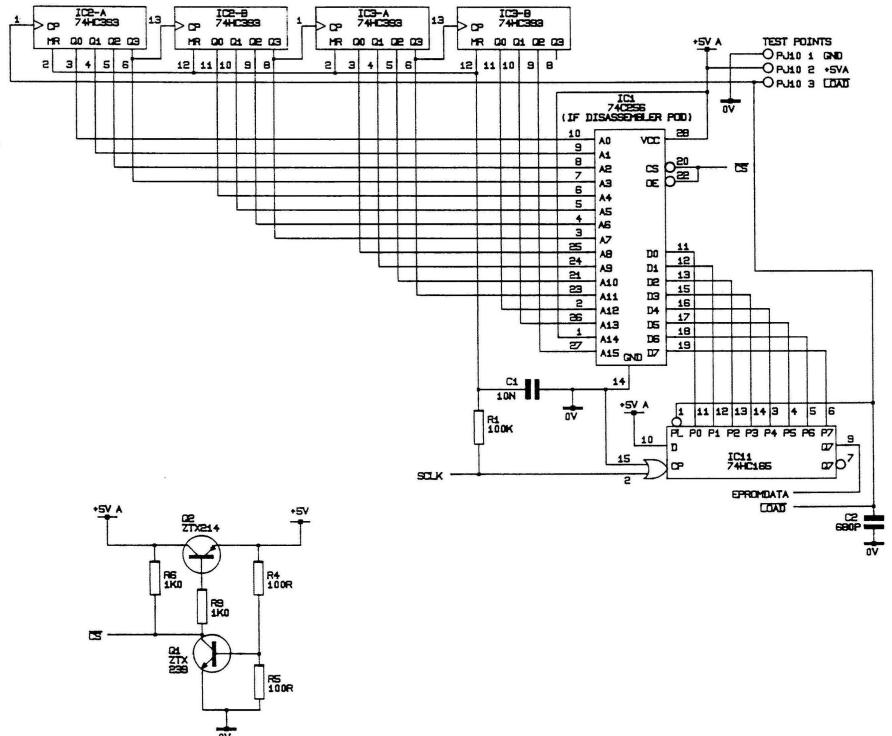
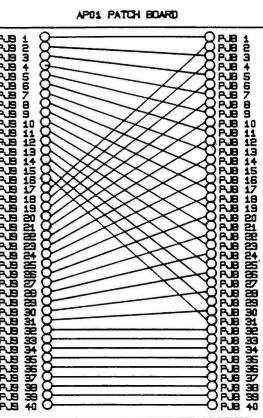
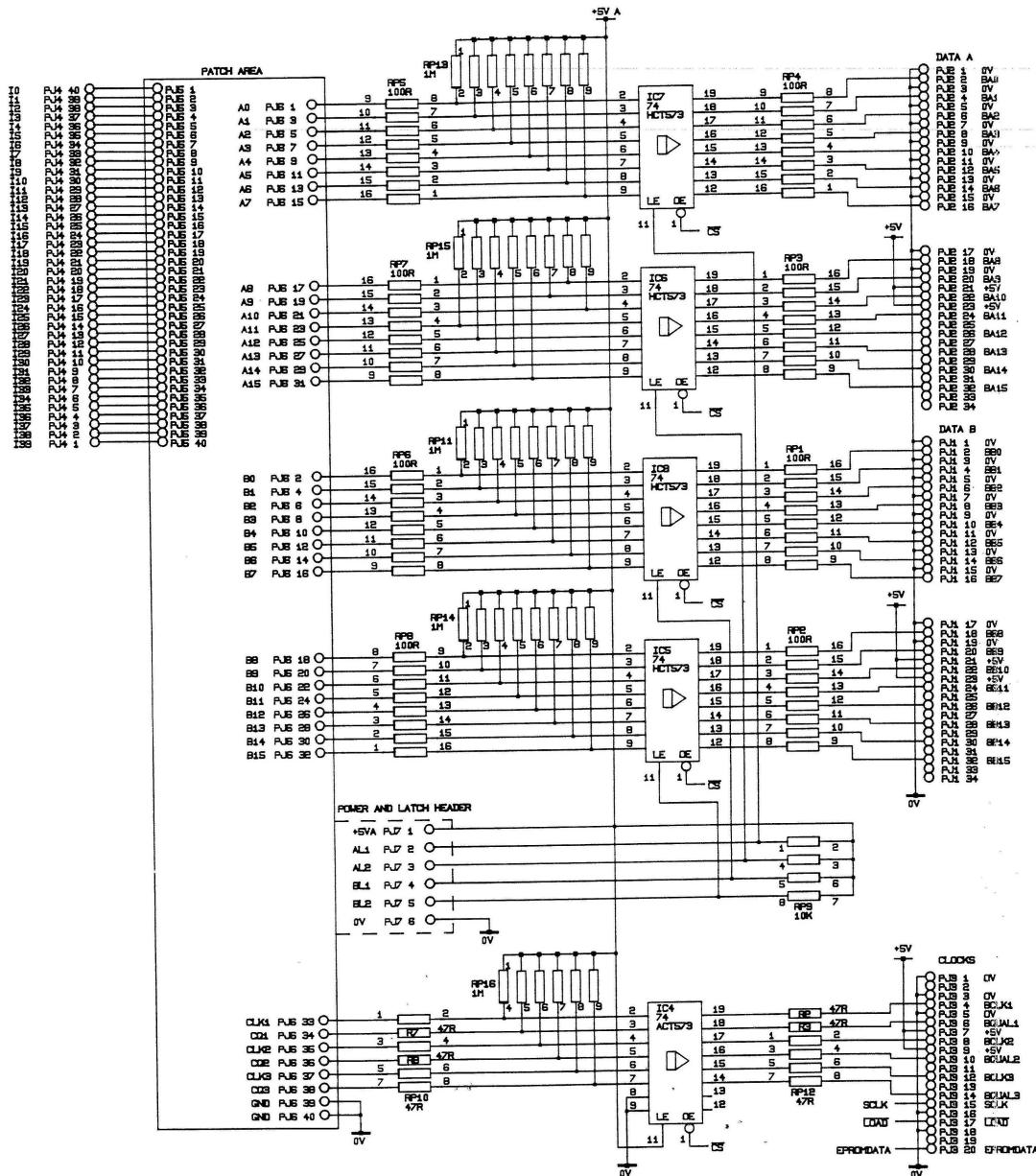


Fig 4 AP01: 32-CHANNEL DATA AND CLOCK POD

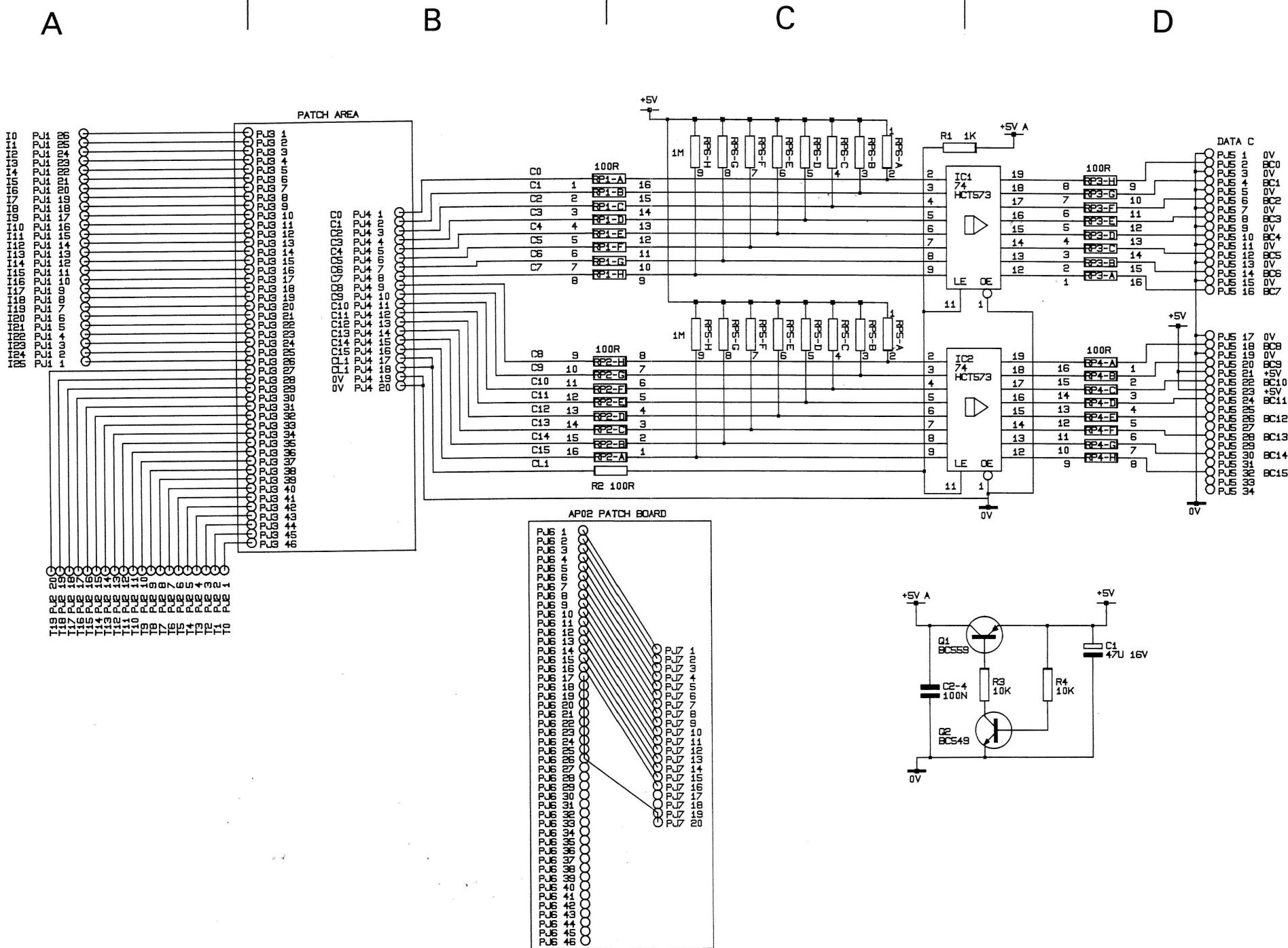


Fig 5 16 CHANNEL BOARD TO CONVERT AP01 TO AP02 (48-CHANNEL DATA AND CLOCK PODS)

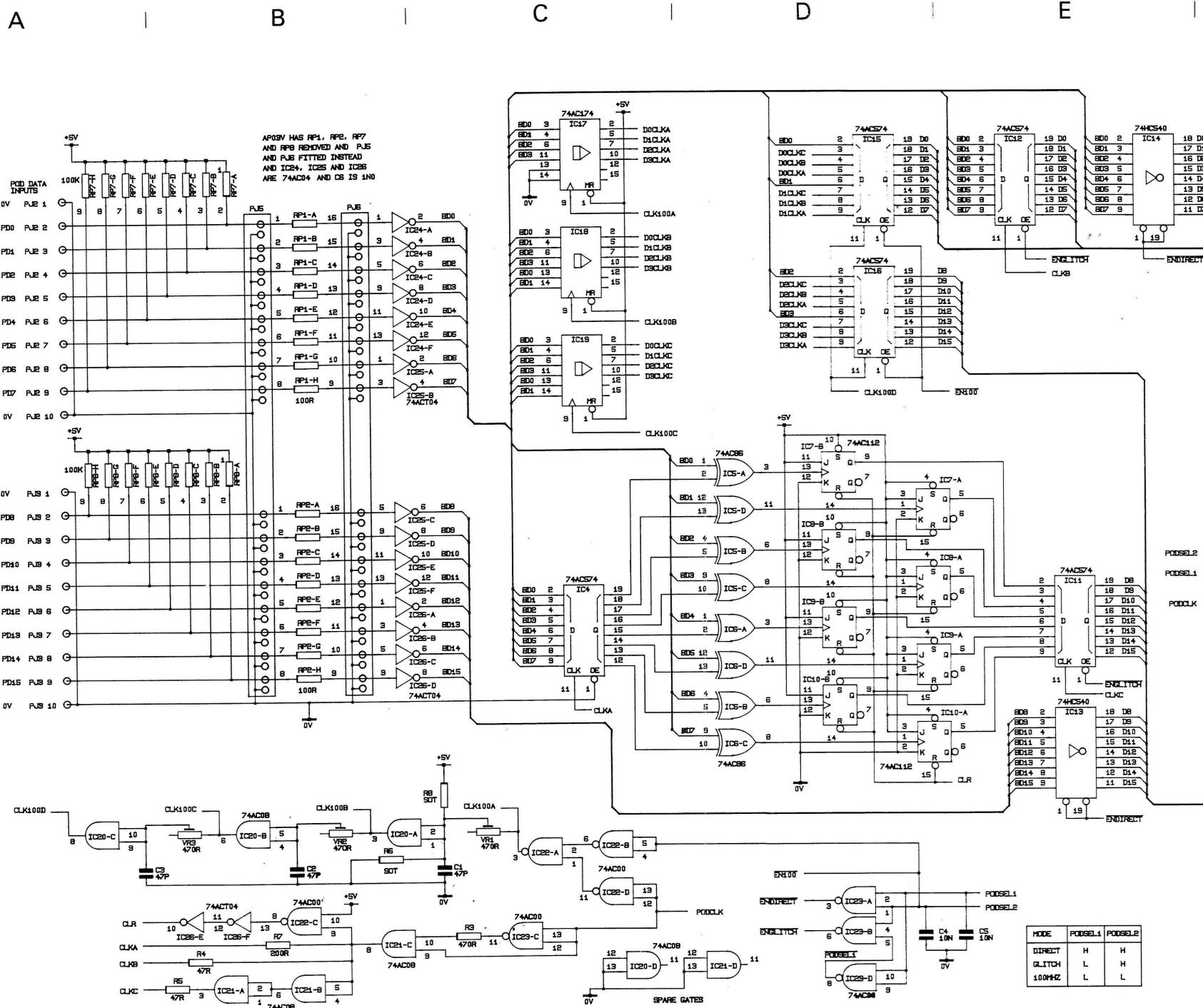
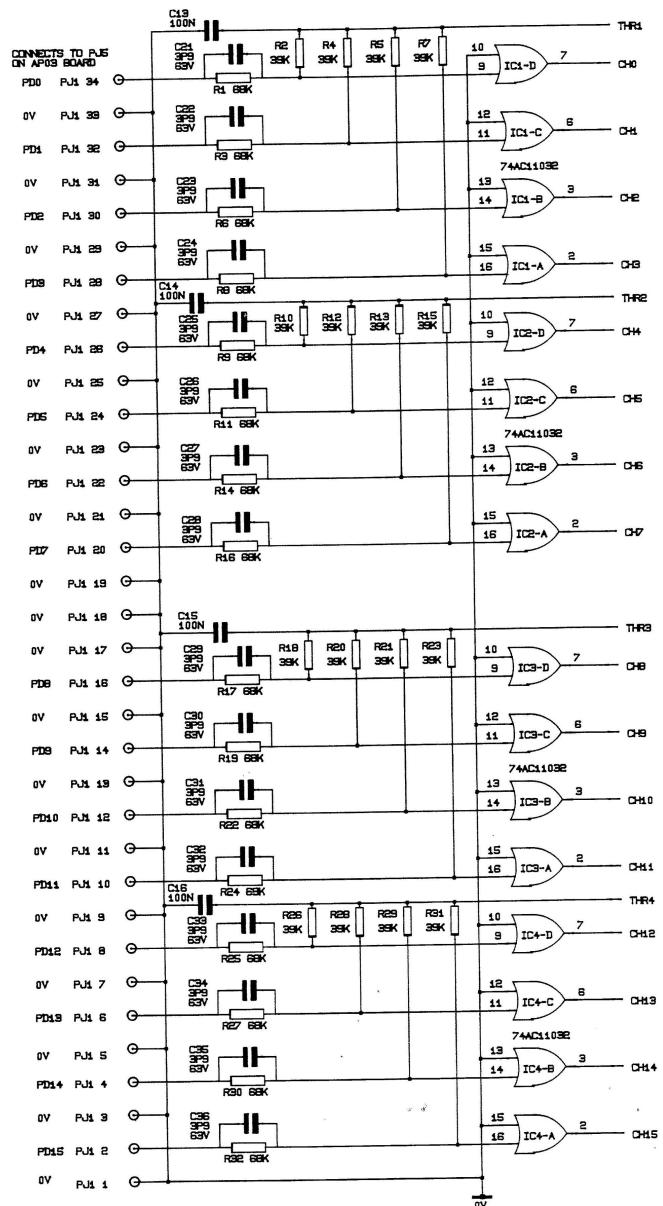


Fig 6 GLITCH BOARD FOR AP03/AP03V DATA PODS

A



B

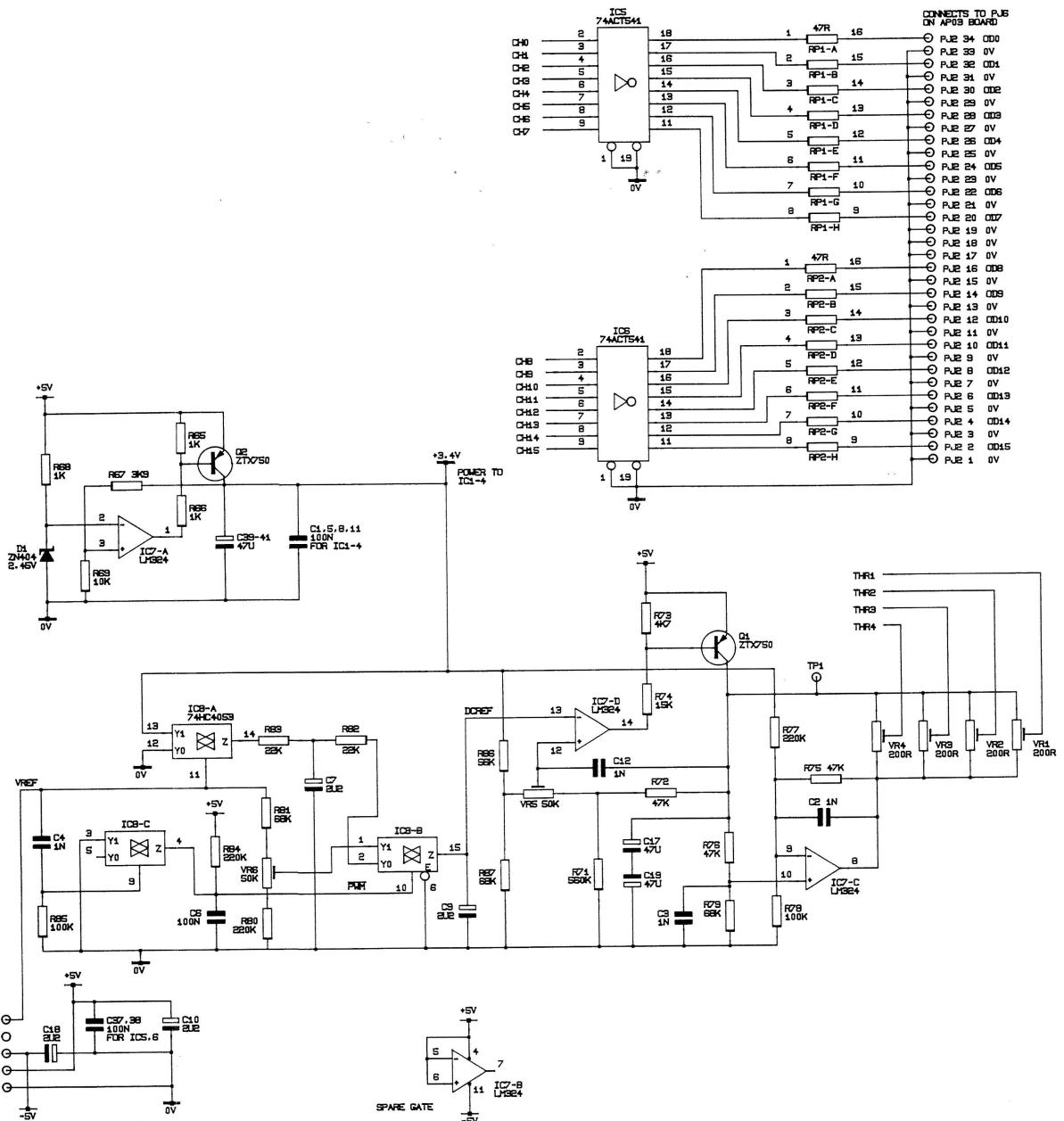
C

D

E

F

1



2

3

4

Fig 7 UPPER VARIABLE THRESHOLD BOARD FOR APO3V DATA PODS

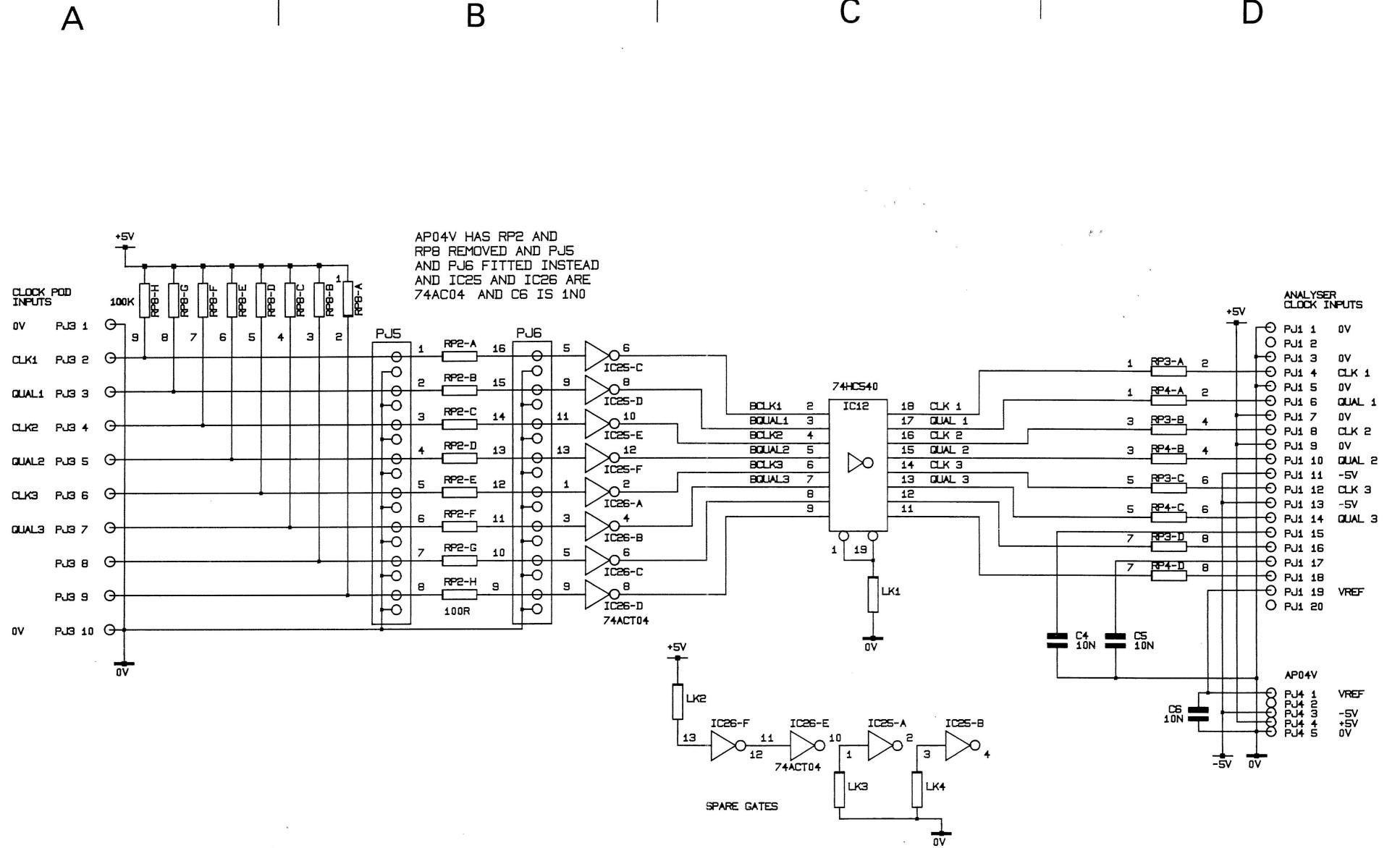
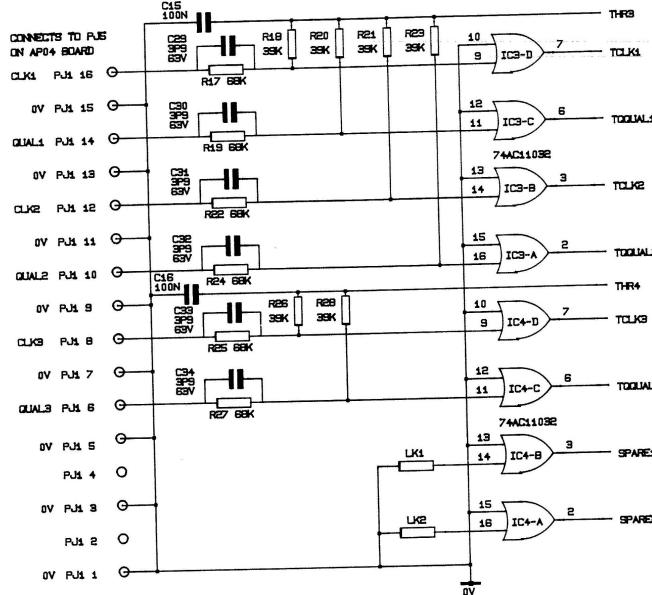


Fig 8 CLOCK POD BOARD FOR AP04/AP04V CLOCK PODS

A



B

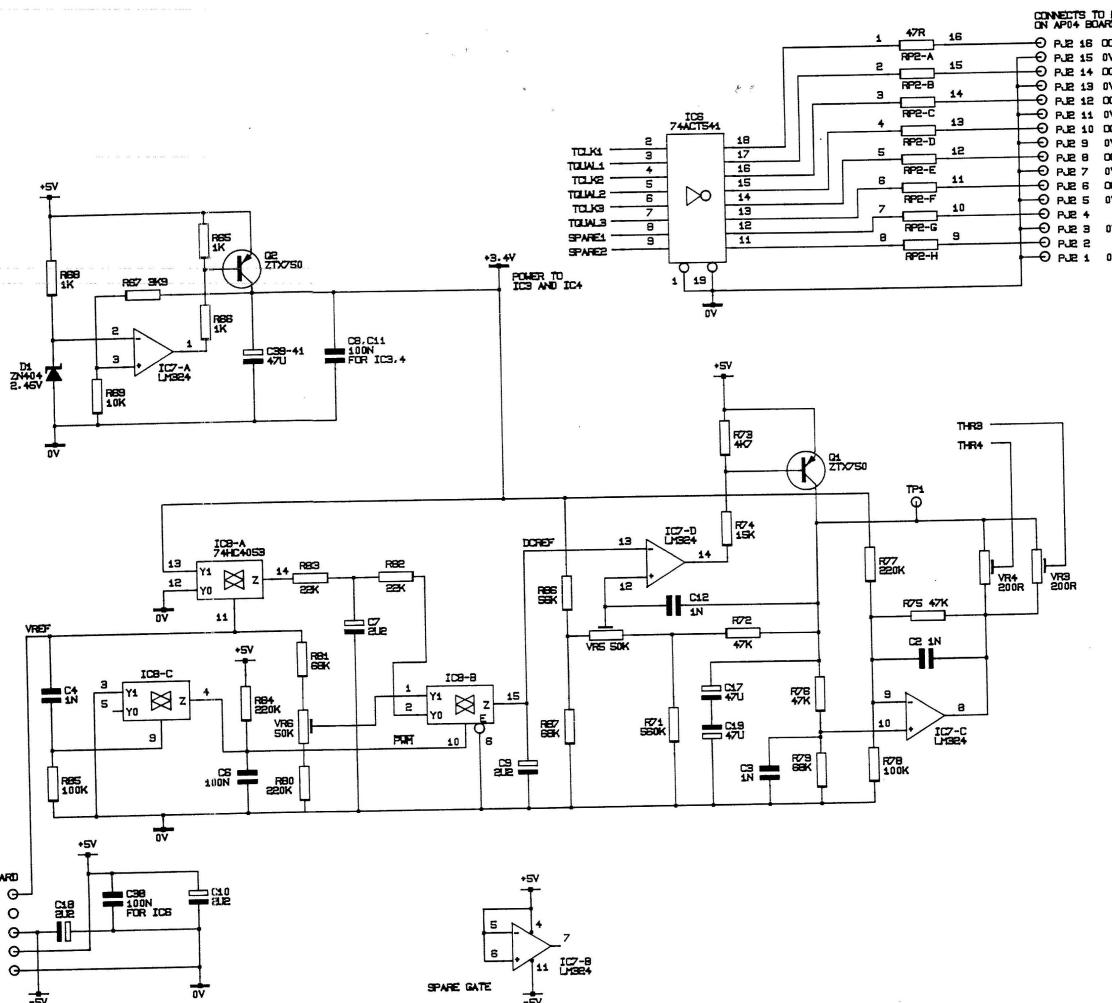
C

D

E

F

1



2

3

4

Fig 9 UPPER VARIABLE THRESHOLD BOARD FOR AP04V CLOCK PODS

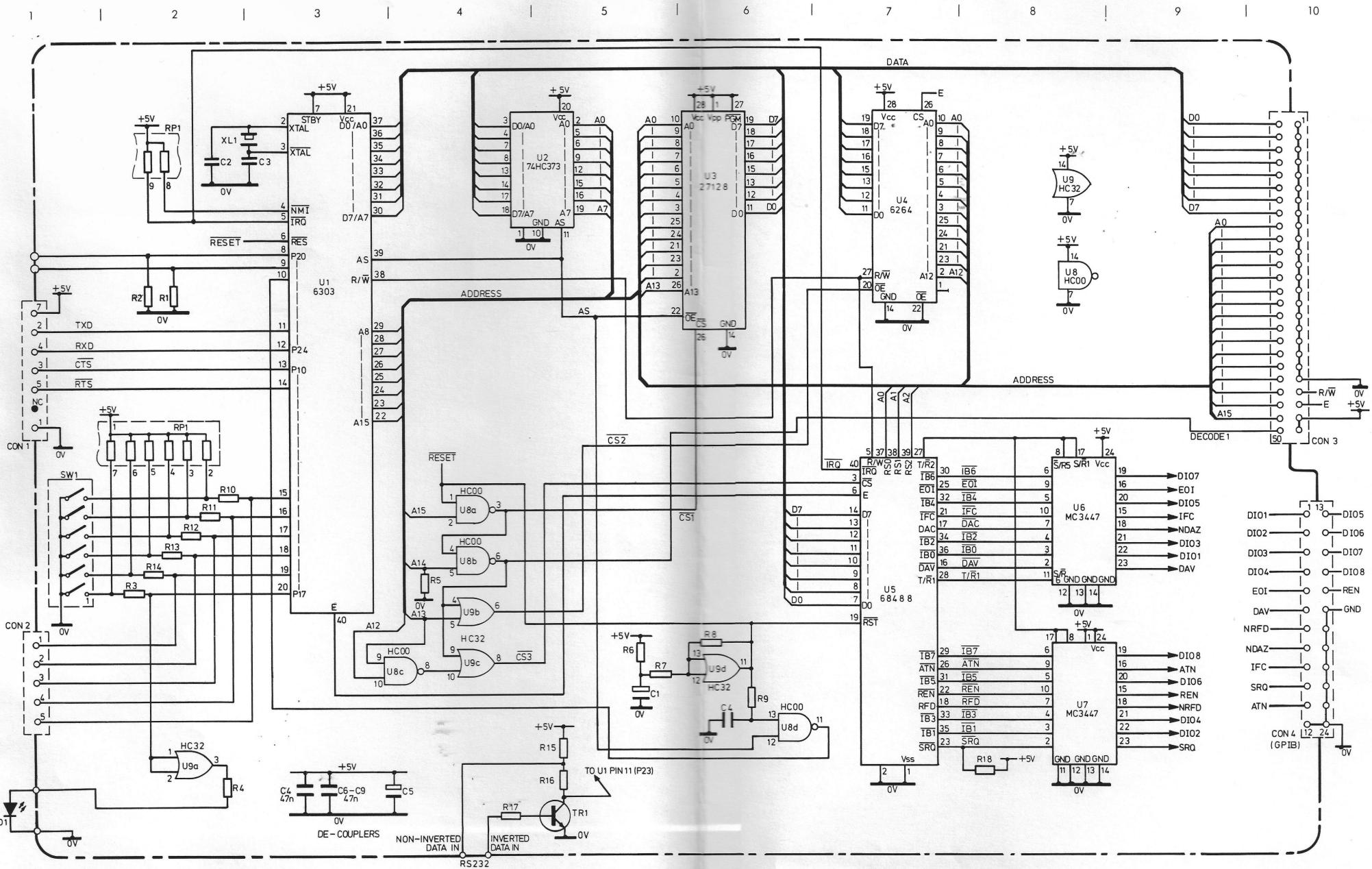


Fig 10 GP500A IEEE-488 INTERFACE BOARD

A

B

C

D

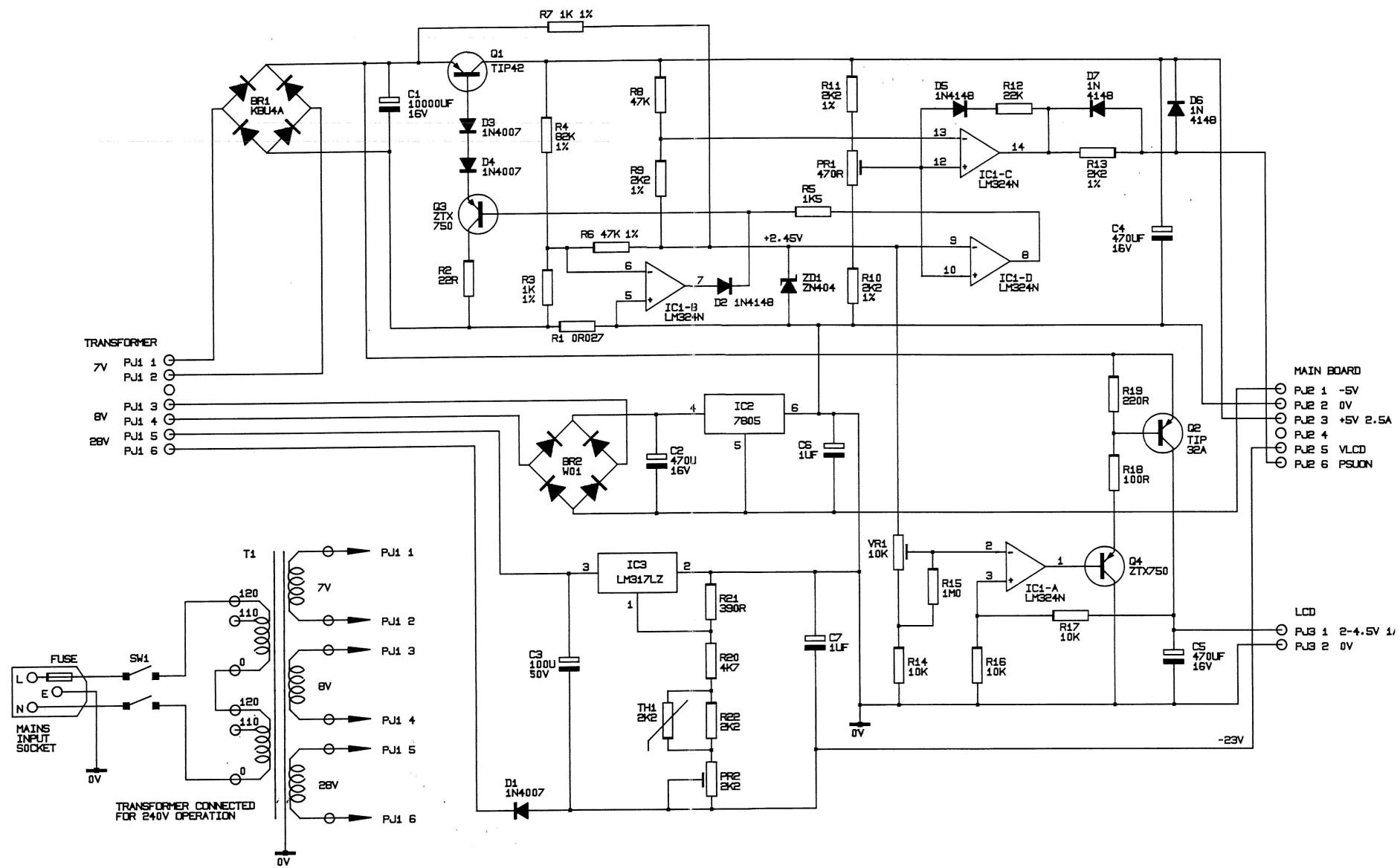


Fig 11 LA4800/3200 POWER SUPPLY