****

THURLBY LA3200/4800

MICROPROCESSOR DISASSEMBLER POD DP-Z80

OPERATING MANUAL

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1. Introduction

The DP-Z80 is a disassembler pod for use with the Thurlby LA3200 and LA4800 logic analysers. The pod includes the hardware necessary to connect the microprocessor under test to the analyser's inputs and the special software to enable the acquired data to be disassembled into standard processor mnemonics and cycle types.

2. Specification

Processor types supported	Z80, Z80A, z80B, Z80C
Maximum Processor Clock Speed	8MHz
Input Connector	40-way dual row latched header
Input Impedance	100k Ohm / 8pF
Threshold	TTL level (+1.4V)
Maximum Input Voltage	+10V / -5V

3. Connecting the Pod to the Logic Analyser

Before connecting the disassembler pod to the analyser turn the power to the analyser off.

Plug the three cables marked DATA A, DATA B, and CLOCKS into the appropriately labelled sockets on the analyser.

4. Connecting the Pod to the Microprocessor under test

The pod is designed to be connected to the microprocessor under test by using either a 40-way sprung test clip (Thurlby type LC-92 or LC-93) or by using a 40-way I.C. replacement connector (Thurlby type LC-91). Both types plug directly into the pod by means of a bump-polarised connector.

When using a sprung test clip ensure that the clip is correctly orientated by locating pin 1 as marked on the pod. When working with uPs that use an on-chip oscillator it is possible for the extra capacitance of the cable to stop the oscillator from working. In this case the relevant connections must be removed from the test clip end of the cable.

When using an I.C. replacement connector (type LC-91), remove the uP from the target system and plug it into the gold plated connector on the LC-91. The DIL socket is then plugged into the target system in place of the uP.

Note that if power to the analyser is turned off when the pod is still connected to the target system then current may be drawn from the target system which could cause the target system to crash.

5. Z80 Connection List

CPU SIGNAL	CPU PIN	Analyser Input
A15	5	A15
A14	4	A14
A13	3	A13
A12	2	A12
A11	1	A11
A10	40	A10
A9	39	A9
A8	38	A8
A7	37	A7
A6	36	A6
A5	35	A5
A4	34	A4
A3	33	A3
A2	32	A2
A1	31	A1
A0	30	A0
D7	13	B7
D6	10	B6
D5	9	B5
D4	7	B4
D3	8	B3
D2	12	B2
D1	15	B1
D0	14	B0
M1	27	B8
MREQ	19	B9
IORQ	20	B10
RD	21	B11
WR	22	B12
RFSH	28	B13
BUSAK	23	B14
HALT	18	B15
MREQ	19	CLK 1
IORQ	20	CLK 2
CPU CLK	6	CLK 3

6. Loading the Disassembler Software

The disassemb1er software is located within the pod and is loaded into the analyser by a serial interface every time that the analyser is switched on.

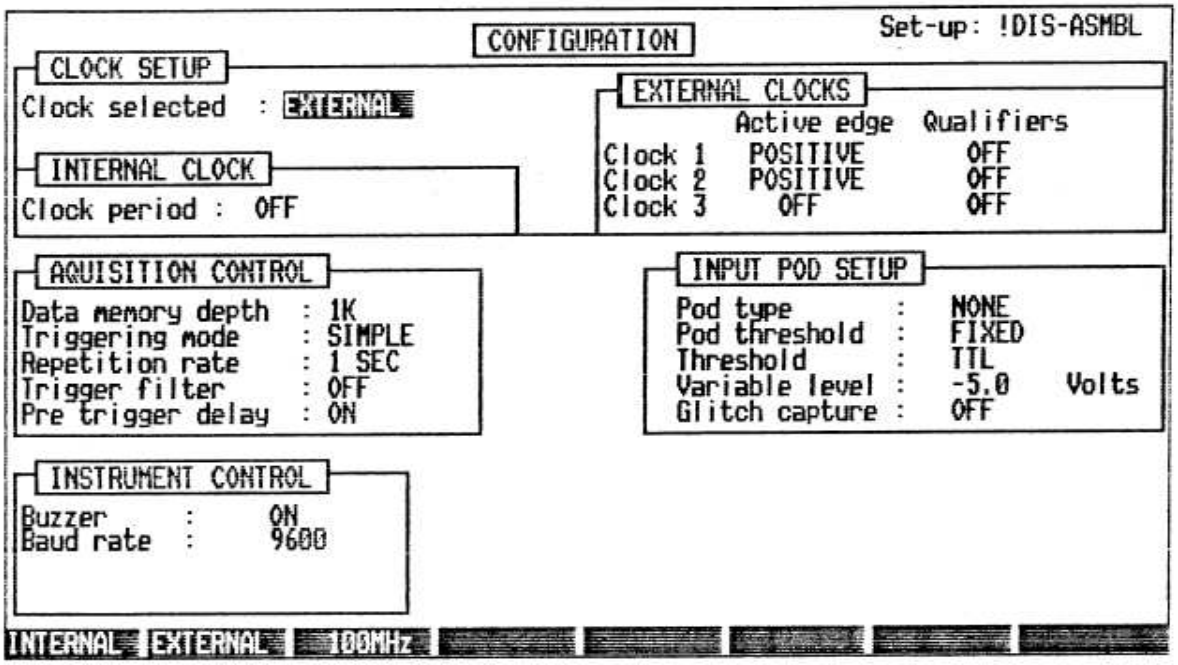
The Main Menu of the analyser will then be modified so that option 7 becomes *Z80 DISASSEMBLER* (along with a software revision number).

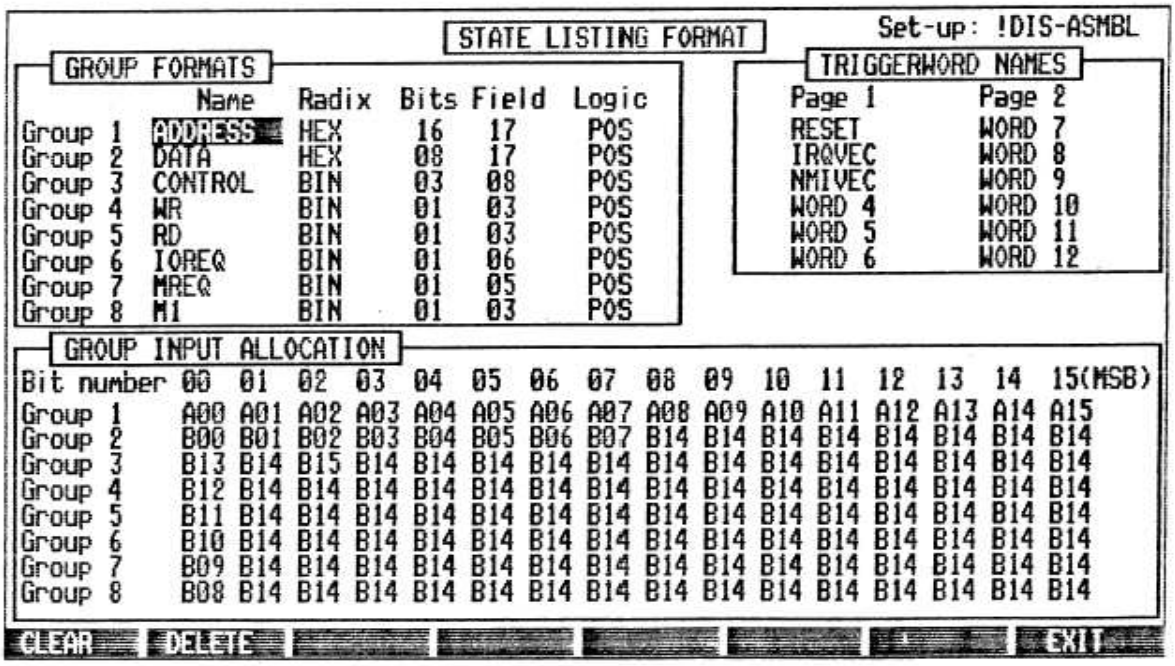
When the analyser is switched on with the pod connected, the display will show the message "Reading Disassembler from Pod" followed by "Verifying Disassembler from Pod". When the loading and verification have been completed a window will appear giving the user the option of loading the default set-up for the disassembler. Note that loading the default setup will destroy the set-up currently in use. If the default is not loaded at this time, it can be loaded later by selecting option 6 from the main menu and selecting Defaults.

7. The Default Set-Up

The Disassembler software includes a default set-up suitable for the microprocessor. The set-up can be loaded immediately after switch-on or at any other time (by selecting Defaults from the Store Recall screen).

The default set-up for the DP-Z80 sets the Configuration Screen and State Listing Format screens as shown below. Changes may be made to the default (such as adding appropriate trigger conditions), and the modified default stored in one of the user-defined set–up stores (setup 01 to setup 10).



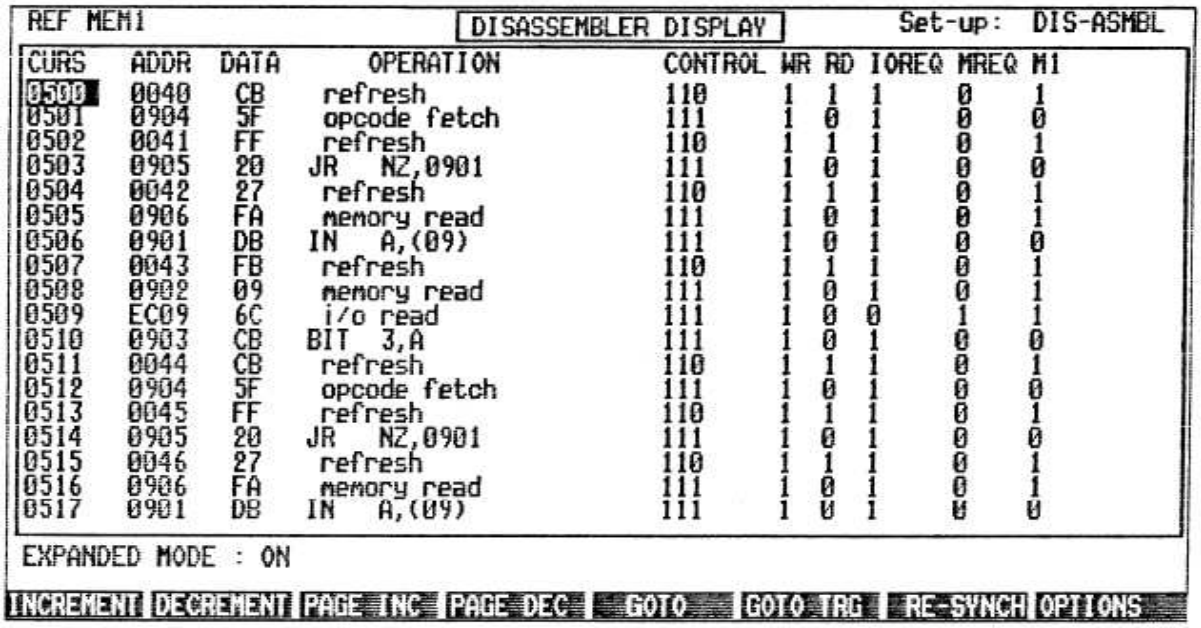


8. The Disassembler Listing Screen

Selecting option 7 from the main menu brings up the disassembler listing screen. This differs from the state listing in that the display shows actual microprocessor machine cycles and includes the microprocessor specific mnemonics.

To change the memory being disassembled, tab the cursor to the top of the screen and choose the appropriate memory.

There are two versions of the disassembler listing, expanded mode and non–expanded mode. In expanded mode, every machine cycle is shown whilst in non-expanded mode only op-code cycles are shown. To change between the two modes tab down to the Expanded Mode line and turn it on or off.

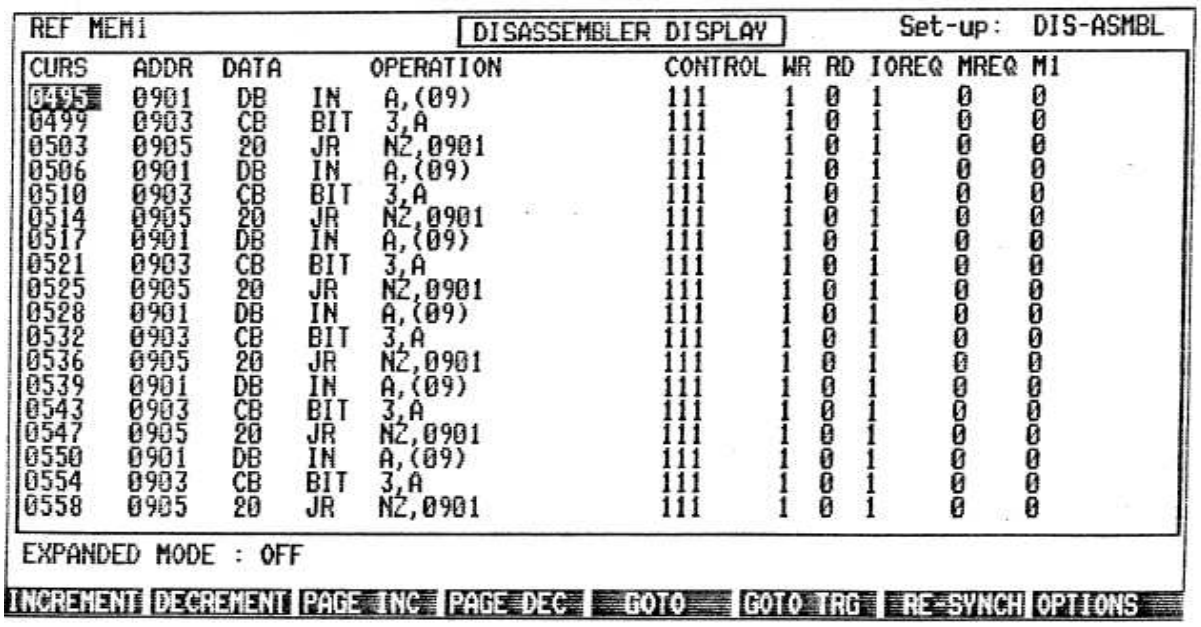


REF MEM1 — DISASSEMBLER DISPLAY — Set-up: DIS-ASMBL

CURS	ADDR	DATA	OPERATION	CONTROL	WR	RD	IOREQ	MREQ	M1
0500	0040	CB	refresh	110	1	1	1	0	1
0501	0904	5F	opcode fetch	111	1	0	1	0	0
0502	0041	FF	refresh	110	1	1	1	0	1
0503	0905	20	JR NZ,0901	111	1	0	1	0	0
0504	0042	27	refresh	110	1	1	1	0	1
0505	0906	FA	memory read	111	1	0	1	0	1
0506	0901	DB	IN A,(09)	111	1	0	1	0	0
0507	0043	FB	refresh	110	1	1	1	0	1
0508	0902	09	memory read	111	1	0	1	0	1
0509	EC09	6C	i/o read	111	1	0	0	1	1
0510	0903	CB	BIT 3,A	111	1	0	1	0	0
0511	0044	CB	refresh	110	1	1	1	0	1
0512	0904	5F	opcode fetch	111	1	0	1	0	0
0513	0045	FF	refresh	110	1	1	1	0	1
0514	0905	20	JR NZ,0901	111	1	0	1	0	0
0515	0046	27	refresh	110	1	1	1	0	1
0516	0906	FA	memory read	111	1	0	1	0	1
0517	0901	DB	IN A,(09)	111	1	0	1	0	0

EXPANDED MODE : ON

INCREMENT | DECREMENT | PAGE INC | PAGE DEC | GOTO | GOTO TRG | RE-SYNCH | OPTIONS



REF MEM1 — DISASSEMBLER DISPLAY — Set-up: DIS-ASMBL

CURS	ADDR	DATA	OPERATION	CONTROL	WR	RD	IOREQ	MREQ	M1
0495	0901	DB	IN A,(09)	111	1	0	1	0	0
0499	0903	CB	BIT 3,A	111	1	0	1	0	0
0503	0905	20	JR NZ,0901	111	1	0	1	0	0
0506	0901	DB	IN A,(09)	111	1	0	1	0	0
0510	0903	CB	BIT 3,A	111	1	0	1	0	0
0514	0905	20	JR NZ,0901	111	1	0	1	0	0
0517	0901	DB	IN A,(09)	111	1	0	1	0	0
0521	0903	CB	BIT 3,A	111	1	0	1	0	0
0525	0905	20	JR NZ,0901	111	1	0	1	0	0
0528	0901	DB	IN A,(09)	111	1	0	1	0	0
0532	0903	CB	BIT 3,A	111	1	0	1	0	0
0536	0905	20	JR NZ,0901	111	1	0	1	0	0
0539	0901	DB	IN A,(09)	111	1	0	1	0	0
0543	0903	CB	BIT 3,A	111	1	0	1	0	0
0547	0905	20	JR NZ,0901	111	1	0	1	0	0
0550	0901	DB	IN A,(09)	111	1	0	1	0	0
0554	0903	CB	BIT 3,A	111	1	0	1	0	0
0558	0905	20	JR NZ,0901	111	1	0	1	0	0

EXPANDED MODE : OFF

INCREMENT | DECREMENT | PAGE INC | PAGE DEC | GOTO | GOTO TRG | RE-SYNCH | OPTIONS

Normal control of the disassemble screen is obtained when the tab bar is positioned over the cursor position. The screen may be decremented by line or page or redrawn at the cursor number from the numeric keypad is obtained when the tab bar is screen can be incremented or any memory position by overwriting and pressing GOTO.

The Options key gives access to a screen of options for alternative microprocessor types. For the DP-Z80 there are no alternative types.

The Re-synch key is not necessary with the DP-Z80.

Note that attempting to use the disassembler listing screen on data that was not acquired using an appropriate set-up or an appropriate pod will produce meaningless data.

8.1 Error Messages

The following error messages in the Mnemonics listing may be encountered:

<Invalid Opcode>	The opcode stored is not a valid manufacturer's opcode and is consequently undefined. As a result the action of the microprocessor in this case is unknown.
<Partial Opcode>	One or more bytes of a multi-byte instruction have not been stored and the mnemonics cannot be evaluated. This is likely to occur with cycle qualification.
<Unknown Cycle>	This will occur when the combination of Z80 control lines is not recognisable as a valid machine cycle. This will usually be the result of a hardware error.

8.2 Omissions

Omissions in the mnemonics listing will be designated by a pair of asterisks (**) which will appear in the listing in place of each missing operand. Omissions will normally be the result of storage qualification. Examples of omissions which may be encountered are shown below.

LD A,**	single operand missing
LD (IX+**),28	index register offset operand missing
JR Z,****	jump relative offset operand missing
JP NZ,**05	high order byte of destination address missing
JP NZ,21**	low order byte of destination address missing
LD HL,****	both operands missing

8.3 Clocking the Analyser

The default set-up configures the analyser to clock data in on the positive edge of both the MREQ and IOREQ signals (clocks 1 and 2). If timing information is required, clocks 1 and 2 should be turned off and clock 3

should be turned on (this clocks the analyser from the processor clock). Data acquired in this way will not disassemble correctly.

9. Triggering

The default set-up for the DP-Z80 sets Simple trigger and sets the trigger word to all don't cares. The trigger can be set to any combination of the address, data and control lines, but the most common requirement is to trigger on an address.

When a more complex trigger pattern is required the trigger type on the Configuration screen should be changed to Complex.

10. Trace

The trace facility of the analyser allows the selective capture of data depending on the state of the lines. When using a disassembler, Trace must be used with care as it is easy to remove part of the instruction. Particular care must be used when working with microprocessors which do not have an op-code sync output.

11. Cycle Types and Control Status

The State Listing screen (using the default set-up) shows the status of the Z80 control bus in binary. This can be used as part of the trigger or trace setting. The relationship between control bus and the cycle type is as follows:

Cycle Type	BUSAK	RFSH	WR	RD	IORQ	MREQ	M1
Opcode fetch	1	1	1	0	1	0	0
Memory read	1	1	1	0	1	0	1
Memory write	1	1	0	1	1	0	1
I/O read	1	1	1	0	0	1	1
I/O write	1	1	0	1	0	1	1
Refresh	1	0	1	1	1	0	1
Interrupt ack.	1	1	1	1	0	1	0
DMA Memory read	0	1	1	0	1	0	1
DMA Memory write	0	1	0	1	1	0	1
DMA I/O read	0	1	1	0	0	1	1
DMA I/O write	0	1	0	1	0	1	1

12. Acquiring Data

Acquiring data for disassembly is done in exactly the same way as for normal operation. Pressing the Run key will bring up the normal window of options.

Note that Repeat Acquisition will be slower than normal when using the Disassembler Listing screen because of the time taken to perform the disassembly.

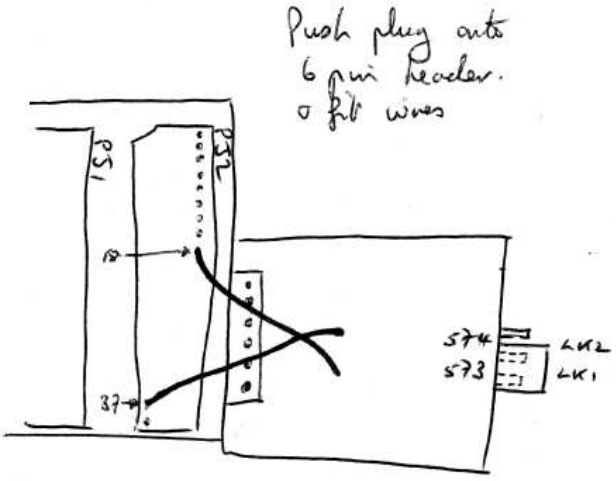
28/11/90

Graham,

Fit the board as shown below - it is preferable to use the 573's and the link is positioned for 573's. Let me know if you have any problems.

John Timms.

pink to PJ2 pin 18
green to PJ2 pin 37



LK2 inverts the latch signal for 574's
574's fitted to those marked * only.