EECS478 Project 3

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1. Tasks

Task 1: Topological sorting

In this task, first I add a new variable "vector<Node*> fanout" to the Node class. And when Node A is added as the fan-in of Node B, I also add Node B into the fan-out vector of Node A. I also add an integer variable called fanin_num and assign the size of fanin vector to it. When implementing topological sorting, I first start from the primary input nodes and explore their fan-out. When a Node is reached by one node, its fanin_num will be decreased by one. If the fanin_num is equal to zero, which means that all its fan-in have been visited, we can record this node into topological sorting list. We explore the whole circuit by BFS search method, and in the end we will have a complete topological sorting sequence.

Task 2: Functional simulation

Again before implementing the function, we add new variable value, whose type is integer, in Node class to represent the output value of this Node. First of all, we call the topological sorting function to obtain the sequence. Then we read in the value of primary inputs and set the value variable in those Nodes. Then we pick out one node each time according to the topological order, decide the gate type of this current node (AND/OR/NOT/XOR), and evaluate its output value from the fan-in value. Since we follow the topological order, the fan-in value must be ready when we pick up the node.

2. Verification

I choose the 16-bit subtractor as the BLIF file used for verification since it contains all kinds of four gates. I write a small program on C++ to randomly generate input patterns and run the simulation on my program. I also run the same input pattern on the simulation program provided by project 2 and compare the results. I randomly generate 5000 input patterns and the simulation results of my program are the same as the one from simulation program.