

1) {ADD, ADC, ADZ, AND, NDC, NDZ}

PC  $\rightarrow$  mem.a, alu.a, t3  
 mem.d  $\rightarrow$  ir  
 +1  $\rightarrow$  alu.b  
 alu.out  $\rightarrow$  PC

ir<sub>9-11</sub>  $\rightarrow$  rf-a<sub>1</sub>  
 ir<sub>6-8</sub>  $\rightarrow$  rf-a<sub>2</sub>  
 ir<sub>0-7</sub>  $\rightarrow$  PEN  
 rf-d<sub>1</sub>  $\rightarrow$  t<sub>1</sub>  
 rf-d<sub>2</sub>  $\rightarrow$  t<sub>2</sub>

~~if (ir<sub>15</sub> == 1) {~~

if (ir<sub>15</sub> == 1) {  
 t<sub>1</sub>  $\rightarrow$  alu.a  
 t<sub>2</sub>  $\rightarrow$  alu.b  
 alu.out  $\rightarrow$  t<sub>3</sub> } SUB

elseif

if (ir<sub>0</sub> == 0 & ir<sub>1</sub> == 0) || (ir<sub>0</sub> == 0 & ir<sub>1</sub> == 1 & C == 1) || (ir<sub>0</sub> == 1 & ir<sub>1</sub> == 0 & Z == 1)

{  
 t<sub>1</sub>  $\rightarrow$  alu.a  
 t<sub>2</sub>  $\rightarrow$  alu.b  
 alu.out  $\rightarrow$  t<sub>3</sub> } ADD

else {S1}

★ ALU control in S3:

ir<sub>15</sub> + ir<sub>1</sub> Z + ir<sub>0</sub> C + ir<sub>0</sub> · ir<sub>1</sub>

t<sub>3</sub>  $\rightarrow$  rf-d<sub>3</sub>

if (ir<sub>14</sub> == 1) { ir<sub>9-11</sub>  $\rightarrow$  rf-a<sub>3</sub> }

else { if (ir<sub>12</sub> == 0) { ir<sub>3-5</sub>  $\rightarrow$  rf-a<sub>3</sub> }

else

{ ir<sub>6-8</sub>  $\rightarrow$  rf-a<sub>3</sub> }

t<sub>2</sub>  $\rightarrow$  Z

Update Z flag

(update PC/R7)

if (rf-a<sub>3</sub> == 111) { t<sub>3</sub>  $\rightarrow$  PC }

else { PC  $\rightarrow$  R7 }

Carry updation not in AND, NDC, NDZ

0<sub>15</sub> 0<sub>14</sub> 0<sub>13</sub>

④ ADI

S1  
S2

$t1 \rightarrow \text{alu.a}$   
 $r_{0-5} \rightarrow \text{SE6} \rightarrow \text{alu.b}$   
 $\text{alu.out} \rightarrow t3$

~~S5~~

0100

S4

S4 (update PC/R7)

⑧ LHI

S1  
S2

$r_{0-8} \rightarrow \text{FS} \rightarrow \text{rf.d3}$   
 $r_{9-11} \rightarrow \text{rf.a3}$

~~S6~~

0101

S5

(update PC/R7)

⑨ LW

S1  
S2

$t2 \rightarrow \text{alu.a}$   
 $r_{0-5} \rightarrow \text{SE6} \rightarrow \text{alu.b}$   
 $\text{alu.out} \rightarrow t2$

S6

~~S7~~

0110

$t2 \rightarrow \text{mem.a}$   
 $\text{mem.d} \rightarrow t3$

~~S8~~

S7

0111

S4 (update PC/R7)

⑩ SW

S1  
S2  
S7

S6

$t2 \rightarrow \text{mem.a}$   
 $t1 \rightarrow \text{mem.d}$

~~S9~~

update (PC/R7)

~~S8~~ S8

1000



⑪ LM

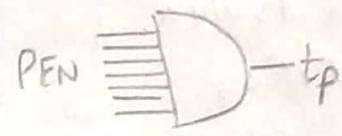
S1  
S2

t1 → mem.a, alu.a  
mem.d → t3  
t1 → alu.b  
alu.out → t1

S10

if  
tp == 1

1001



PEN → PEN - i  
PEN - o → rf - d3  
t3 → rf - d3  
if (tp == 1) { go to s10 }  
else { s13 }

S10

update PC/R7  
update PEN

1010

⑫ SM

S1  
S2

PEN → PEN - i  
PEN - o → rf - a1  
rf - d1 → t2

S11

S12

(tp == 1)

update PEN

1011

t1 → mem.a, alu.a  
t2 → mem.d  
t1 → alu.b  
alu.out → t1  
if (tp == 1) { go to s12 }  
else { s13 }

S12

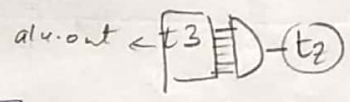
S13

update PC/R7

1100

⑬ BEQ

S1  
S2  
S3



PC → alu.a  
ix0-5 → SEB → alu.b  
if (t2 == 1) { alu.out → PC }  
else { PC → R7 }

S13

S14

update PC/R7

1101

14 JAL

S1  
S2

~~S15~~

$t_3 \rightarrow rf-d3, alu.a$   
 $ir_{q-11} \rightarrow rf-a3$   
 $ir_{o-8} \rightarrow SE9 \rightarrow alu.b$   
 $alu.out \rightarrow PC, R7$

S14

1110

15 JLR

S1  
S2

~~S16~~

$t_3 \rightarrow rf-d3$   
 $ir_{q-11} \rightarrow rf-a3$   
 $t_2 \rightarrow PC, R7$

S15

1111

update PC/R7