# Op Amp Applications Handbook



Analog Devices, Inc.

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SECTION 1-2

# *Op Amp Topologies*

*Walt Kester, Walt Jung, James Bryant*

The previous section examined op amps without regard to their internal circuitry. In this section the two basic op amp topologies—voltage feedback (VFB) and current feedback (CFB)—are discussed in more detail, leading up to a detailed discussion of the actual circuit structures in Section 1-3.

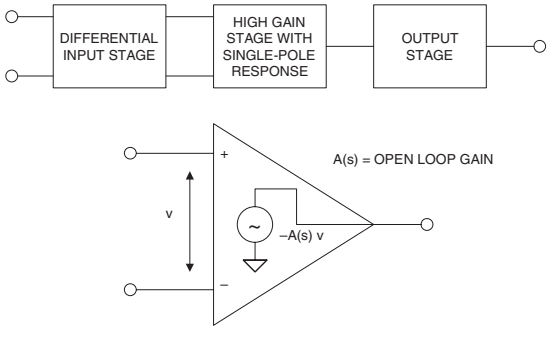



**Figure 1-12: Voltage feedback (VFB) op amp**

Although not explicitly stated, the previous section focused on the voltage feedback op amp and the related equations. In order to reiterate, the basic voltage feedback op amp is repeated here in Figure 1-12 (without the feedback network) and in Figure 1-13 (with the feedback network).

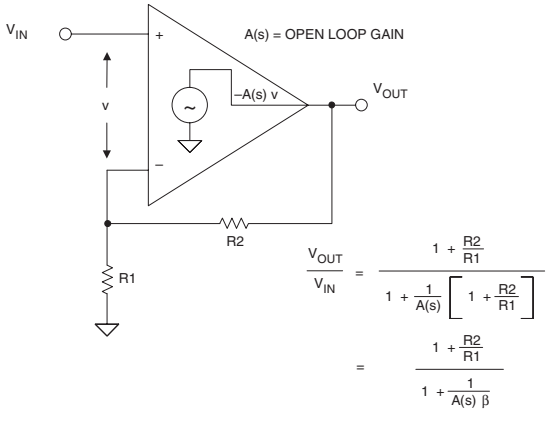



**Figure 1-13: Voltage feedback op amp with feedback network connected**

It is important to note that the error signal developed because of the feedback network and the finite open-loop gain A(s) is in fact a small voltage, v.

## Current Feedback Amplifier Basics

The basic *current feedback* amplifier topology is shown in Figure 1-14. Notice that within the model, a unity gain buffer connects the noninverting input to the inverting input. In the ideal case, the output impedance of this buffer is zero ($R_O = 0$), and the error signal is a small current, i, which flows into the inverting input. The error current, i, is mirrored into a high impedance, T(s), and the voltage developed across T(s) is equal to T(s) · i. (The quantity T(s) is generally referred to as the *open-loop transimpedance gain*.)

This voltage is then buffered and connected to the op amp output. If $R_O$ is assumed to be zero, it is easy to derive the expression for the closed-loop gain, $V_{OUT}/V_{IN}$, in terms of the R1-R2 feedback network and the *open-loop* transimpedance gain, T(s). The equation can also be derived quite easily for a finite $R_O$, and Figure 1-14 gives both expressions.

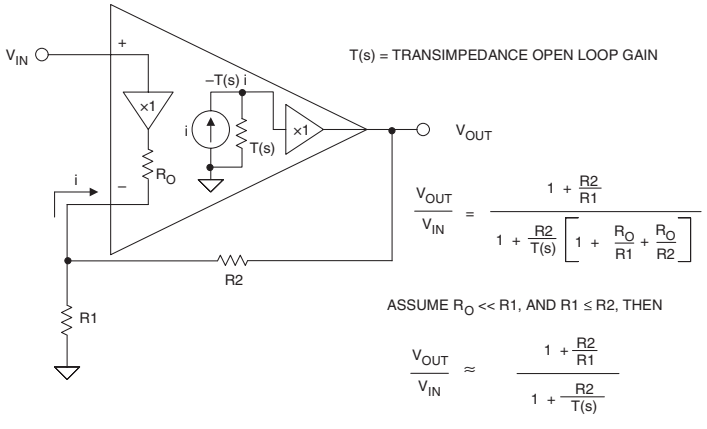



**Figure 1-14: Current feedback (CFB) op amp topology**

At this point it should be noted that current feedback op amps are often called *transimpedance* op amps, because the *open-loop* transfer function is in fact an impedance as described above. However, the term *transimpedance amplifier* is often applied to more general circuits such as current-to-voltage (I/V) converters, where either CFB or VFB op amps can be used. Therefore, some caution is warranted when the term *transimpedance* is encountered in a given application. On the other hand, the term *current feedback op amp* is rarely confused and is the preferred nomenclature when referring to op amp topology.

From this simple model, several important CFB op amp characteristics can be deduced.

- Unlike VFB op amps, CFB op amps *do not have balanced inputs.* Instead, the noninverting input is high impedance, and the inverting input is low impedance.
- The open-loop gain of CFB op amps is measured in units of Ω (transimpedance gain) rather than V/V as for VFB op amps.
- For a fixed value feedback resistor R2, the closed-loop gain of a CFB can be varied by changing R1, without significantly affecting the closed-loop bandwidth. This can be seen by examining the simplified equation in Figure 1-14. The denominator determines the overall frequency response; and if R2 is constant, then R1 of the numerator can be changed (thereby changing the gain) without affecting the denominator—hence the bandwidth remains relatively constant.

The CFB topology is primarily used where the ultimate in high speed and low distortion is required. The fundamental concept is based on the fact that in bipolar transistor circuits currents can be switched faster than voltages, all other things being equal. A more detailed discussion of CFB op amp ac characteristics can be found in Section 1-5.

Figure 1-15 shows a simplified schematic of an early IC CFB op amp, the AD846—introduced by Analog Devices in 1988 (see Reference 1). Notice that full advantage is taken of the complementary bipolar (CB) process which provides well matched high $f_t$ PNP and NPN transistors.

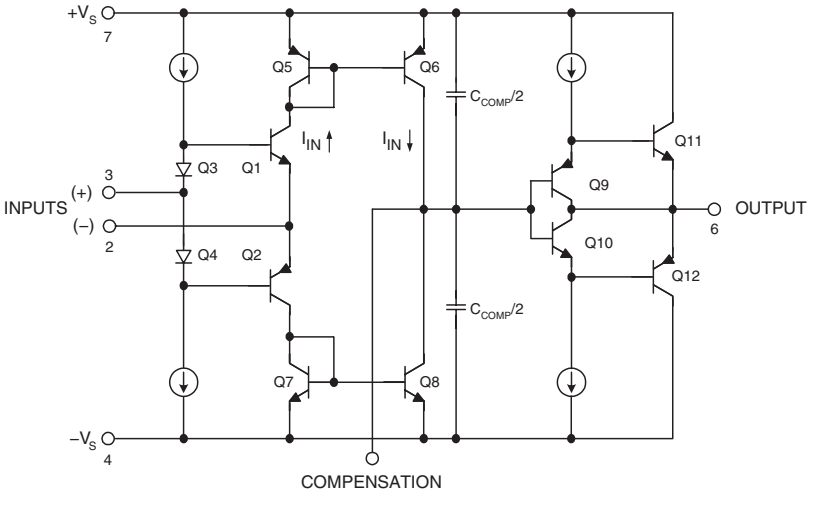



**Figure 1-15: AD846 current feedback op amp (1988)**

Transistors Q1–Q2 buffer the noninverting input (Pin 3) and drive the inverting input (Pin 2). Q5–Q6 and Q7–Q8 act as current mirrors that drive the high impedance node. The $C_{COMP}$ capacitor provides the dominant pole compensation; and Q9, Q10, Q11, and Q12 comprise the output buffer. In order to take full advantage of the CFB architecture, a high speed complementary bipolar (CB) IC process is required. With modern IC processes, this is readily achievable, allowing direct coupling in the signal path of the amplifier.

However, the basic concept of current feedback can be traced all the way back to early vacuum tube feedback circuitry, which used negative feedback to the input tube cathode. This use of the cathode for feedback would be analogous to the CFB op amp's low impedance (–) input, in Figure 1-15.

SECTION 1-3

# Op Amp Structures

*Walt Kester, Walt Jung, James Bryant*

This section describes op amps in terms of their *structures*, and Section 1-4 discusses op amp *specifications*. It is hard to decide which to discuss first, since discussion of specifications, to be useful, entails reference to structures, and discussion of structures likewise requires reference to the performance feature that they are intended to optimize.

Since the majority of readers will have at least some familiarity with operational amplifiers and their specifications, we shall discuss structures first, and assume that readers will have at least a first-order idea of the definitions of the various specifications. Where this assumption proves ill-founded, the reader should look ahead to the next section to verify any definitions required.

Because single-supply devices permeate practically all modern system designs, the related design issues are integrated into the following op amp structural discussions.

## Single-Supply Op Amp Issues

Over the last several years, single-supply operation has become an increasingly important requirement because of market demands. Automotive, set-top box, camera/camcorder, PC, and laptop computer applications are demanding IC vendors to supply an array of linear devices that operate on a single-supply rail, with the same performance of dual supply parts. Power consumption is now a key parameter for line or battery-operated systems, and in some instances, more important than cost. This makes low voltage/low supply current operation critical; at the same time, however, accuracy and precision requirements have forced IC manufacturers to meet the challenge of "doing more with less" in their amplifier designs.

In a single-supply application, the most immediate effect on the performance of an amplifier is the reduced input and output signal range. As a result of these lower input and output signal excursions, amplifier circuits become more sensitive to internal and external error sources. Precision amplifier offset voltages on the order of 0.1 mV are less than a 0.04 LSB error source in a 12-bit, 10 V full-scale system. In a single-supply system, however, a "rail-to-rail" precision amplifier with an offset voltage of 1 mV represents a 0.8 LSB error in a 5 V full-scale system (or 1.6 LSB for 2.5 V full-scale).

To keep battery current drain low, larger resistors are usually used around the op amp. Since the bias current flows through these larger resistors, they can generate offset errors equal to or greater than the amplifier's own offset voltage.

Gain accuracy in some low voltage single-supply devices is also reduced, so device selection needs careful consideration. Many amplifiers with ~120 dB open-loop gains typically operate on dual supplies—for example OP07 types. However, many single-supply/rail-to-rail amplifiers for precision applications typically have open-loop gains between 25,000 and 30,000 under light loading (>10 kΩ). Selected devices, like the OP113/OP213/OP413 family, do have high open-loop gains (>120 dB), for use in demanding applications. Another example would be the AD855x chopper-stabilized op amp series.

Many trade-offs are possible in the design of a single-supply amplifier circuit—speed versus power, noise versus power, precision versus speed and power, and so forth. Even if the noise floor remains constant (highly unlikely), the signal-to-noise ratio will drop as the signal amplitude decreases.

Besides these limitations, many other design considerations that are otherwise minor issues in dual-supply amplifiers now become important. For example, signal-to-noise (SNR) performance degrades as a result of reduced signal swing. "Ground reference" is no longer a simple choice, as one reference voltage may work for some devices, but not others. Amplifier voltage noise increases as operating supply current drops, and bandwidth decreases. Achieving adequate bandwidth and required precision with a somewhat limited selection of amplifiers presents significant system design challenges in single-supply, low power applications.

Most circuit designers take "ground" reference for granted. Many analog circuits scale their input and output ranges about a ground reference. In dual-supply applications, a reference that splits the supplies (0 V) is very convenient, as there is equal supply headroom in each direction, and 0 V is generally the voltage on the low impedance ground plane.

In single-supply/rail-to-rail circuits, however, the ground reference can be chosen anywhere within the supply range of the circuit, since there is no standard to follow. The choice of ground reference depends on the type of signals processed and the amplifier characteristics. For example, choosing the negative rail as the ground reference may optimize the dynamic range of an op amp whose output is designed to swing to 0 V. On the other hand, the signal may require level shifting in order to be compatible with the input of other devices (such as ADCs) that are not designed to operate at 0 V input.

Very early single-supply "zero-in, zero-out" amplifiers were designed on bipolar processes, which optimized the performance of the NPN transistors. The PNP transistors were either lateral or substrate PNPs with much less bandwidth than the NPNs. Fully complementary processes are now required for the new breed of single-supply/rail-to-rail operational amplifiers. These new amplifier designs don't use lateral or substrate PNP transistors within the signal path, but incorporate parallel NPN and PNP input stages to accommodate input signal swings from ground to the positive supply rail. Furthermore, rail-to-rail output stages are designed with bipolar NPN and PNP common-emitter, or N-channel/P-channel common-source amplifiers whose collector-emitter saturation voltage or drain-source channel on resistance determine output signal swing as a function of the load current.

The characteristics of a single-supply amplifier input stage (common-mode rejection, input offset voltage and its temperature coefficient, and noise) are critical in precision, low voltage applications. Rail-rail input operational amplifiers must resolve small signals, whether their inputs are at ground, or in some cases near the amplifier's positive supply. Amplifiers having a minimum of 60 dB common-mode rejection over the entire input common-mode voltage range from 0 V to the positive supply are good candidates. It is not necessary that amplifiers maintain common-mode rejection for signals beyond the supply voltages. *But, what* is *required is that they do not self-destruct for momentary overvoltage conditions.* Furthermore, amplifiers that have offset voltages less than 1 mV and offset voltage drifts less than 2 µV/°C are also very good candidates for precision applications. Since *input* signal dynamic range and SNR are equally if not more important than *output* dynamic range and SNR, precision single-supply/rail-to-rail operational amplifiers should have noise levels referred-to-input (RTI) less than 5 µV p-p in the 0.1 Hz to 10 Hz band.

The need for rail-to-rail amplifier output stages is also driven by the need to maintain wide dynamic range in low supply voltage applications. A single-supply/rail-to-rail amplifier should have output voltage swings that are within at least 100 mV of either supply rail (under a nominal load). The output voltage swing is very dependent on output stage topology and load current.

Generally, the voltage swing of a good rail-to-rail output stage should maintain its rated swing for loads down to 10 kΩ. The smaller the $V_{OL}$ and the larger the $V_{OH}$, the better. System parameters, such as "zero-scale" or "full-scale" output voltage, should be determined by an amplifier's $V_{OL}$ (for zero-scale) and $V_{OH}$ (for full-scale).

- Single Supply Offers:
  - Lower Power
  - Battery-Operated Portable Equipment
  - Requires Only One Voltage

- Design Trade-Offs:
  - Reduced Signal Swing Increases Sensitivity to Errors Caused by Offset Voltage, Bias Current, Finite Open-Loop Gain, Noise, etc.
  - Must Usually Share Noisy Digital Supply
  - Rail-to-Rail Input and Output Needed to Increase Signal Swing
  - Precision Less than the best Dual Supply Op Amps but not Required for All Applications
  - Many Op Amps Specified for Single Supply, but do not have Rail-to-Rail Inputs or Outputs

**Figure 1-20: Single-supply op amp design issues**

Since the majority of single-supply data acquisition systems require at least 12-to 14-bit performance, amplifiers which exhibit an open-loop gain greater than 30,000 for all loading conditions are good choices in precision applications. Single-supply op amp design issues are summarized in Figure 1-20.

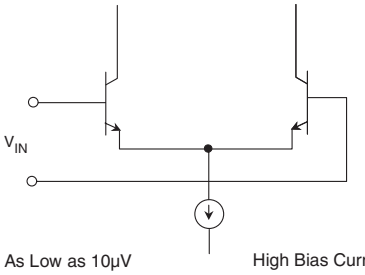
## *Op Amp Input Stages*

It is extremely important to understand input and output structures of op amps in order to properly design the required interfaces. For ease of discussion, the two can be examined separately, as there is no particular reason to relate them at this point.

### Bipolar Input Stages

The very common and basic bipolar input stage of Figure 1-21 consists of a "long-tailed pair" built with bipolar transistors. It has a number of advantages: it is simple, has very low offset, the bias currents in the inverting and noninverting inputs are well-matched and do not vary greatly with temperature. In addition, minimizing the initial offset voltage of a bipolar op amp by laser trimming also minimizes its drift over temperature. This architecture was used in the very earliest monolithic op amps such as the μA709. It is also used with modern high speed types, like the AD829 and AD8021.

Although NPN bipolars are shown, the concept also applies with the use of PNP bipolars.




Low Offset: As Low as 10μV

Low Offset Drift: As Low as 0.1μV/ºC

Temperature Stable $I_B$

Well-Matched Bias Currents

Low Voltage Noise: As Low as 1nV/$\sqrt{Hz}$

High Bias Currents: 50nA – 10μA

(Except Super-Beta: 50pA – 5nA, More Complex and Slower)

Medium Current Noise: 1pA/$\sqrt{Hz}$

Matching source impedances minimize offset error due to bias current

**Figure 1-21: A bipolar transistor input stage**

The AD829, introduced in 1990, is shown in Figure 1-22. This op amp uses a bipolar differential input stage, Q1–Q2, which drives a "folded cascode" gain stage which consists of a fast pair of PNP transistors, Q3–Q4 (see Reference 1). These PNPs drive a current mirror that provides the differential-to-single-ended conversion. The output stage is a two-stage complementary emitter follower.

The AD829 is a wideband video amplifier with a 750 MHz uncompensated gain-bandwidth product, and it operates on ±5 V to ±15 V supplies. For added flexibility, the AD829 provides access to the internal compensation node ($C_{COMP}$). This allows the user to customize frequency response characteristics for a particular application where the closed-loop gain is less than 20. The RC network connected between the output and the high impedance node helps maintain stability, when driving capacitive loads.

Input bias current is 7 μA maximum at 25°C, input voltage noise is $1.7\ nV/\sqrt{Hz}$, and input current noise is $1.5\ pA/\sqrt{Hz}$. Laser wafer trimming reduces the input offset voltage to 0.5 mV maximum for the "A" grade. Typical input offset voltage drift is 0.3 μV/°C.

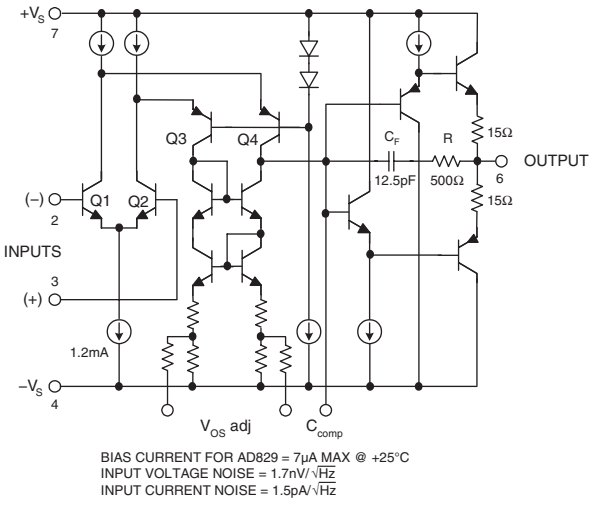



**Figure 1-22: AD829 op amp simplified schematic**

In an op amp input circuit such as Figure 1-22, the input bias current is the base current of the transistors comprising the long-tailed pair, Q1–Q2. It can be quite high, especially in high speed amplifiers, because the collector currents are high. It is typically ~3 μA, for the AD829. In amplifiers where the bias current is *uncompensated* (as true in this case), the bias current will be equal to one-half of the Q1–Q2 emitter current, divided by the $H_{FE}$.

The bias current of a simple bipolar input stage can be reduced by a couple of measures. One is by means of *bias current compensation*, to be described further below.

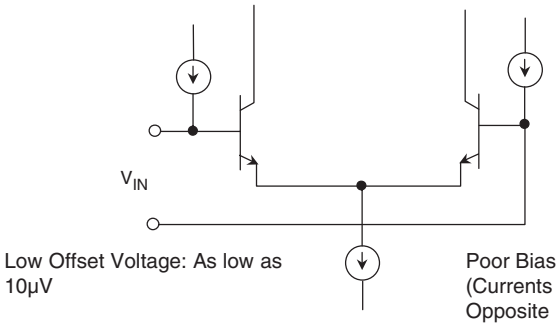
Another method of reducing bias current is by the use of *superbeta* transistors for Q1–Q2. Superbeta transistors are specially processed devices with a very narrow base region. They typically have a current gain of thousands or tens of thousands (rather than the more usual hundreds). Op amps with superbeta input stages have much lower bias currents, but they also have more limited frequency response.

Since the breakdown voltages of superbeta devices are quite low, they also require additional circuitry to protect the input stage from damage caused by overvoltage (for example, they wouldn't operate in the circuit of Figure 1-22).

Some examples of superbeta input bipolar op amps are the AD704/AD705/AD706 series, and the OP97/OP297/OP497 series (single, dual, quad). These devices have typical 25°C bias currents of 100 pA or less.

## Bias Current Compensated Bipolar Input Stage

A simple bipolar input stage such as used in Figure 1-22 exhibits high bias current because the currents seen externally are in fact the base currents of the two input transistors.




| | |
|---|---|
| Low Offset Voltage: As low as 10µV | Poor Bias Current Match (Currents May Even Flow in Opposite Directions) |
| Low Offset Drift: As low as 0.1µV/°C | Higher Current Noise |
| Temperature Stable $I_{bias}$ | Not Very Useful at HF |
| Low Bias Currents: <0.5nA – 10nA | Matching source impedances makes offset error due to bias current worse because of additional impedance |
| Low Voltage Noise: As low as 1nV/√Hz | |

**Figure 1-23: A bias current compensated bipolar input stage**

By providing necessary bias currents via an internal current source, as in Figure 1-23, the only *external* current then flowing in the input terminals is the difference current between the base current and the current source, which can be quite small.

Most modern precision op amps use some means of internal bias current compensation; examples would be the familiar OP07 and OP27 series.

The well-known OP27 op amp family is good example of bias-compensated op amps (see References 2 and 3). The simplified schematic of the OP27, shown in Figure 1-24, shows that the multiple-collector transistor Q6 provides the bias current compensation for the input transistors Q1 and Q2. The "G" grade of the OP27

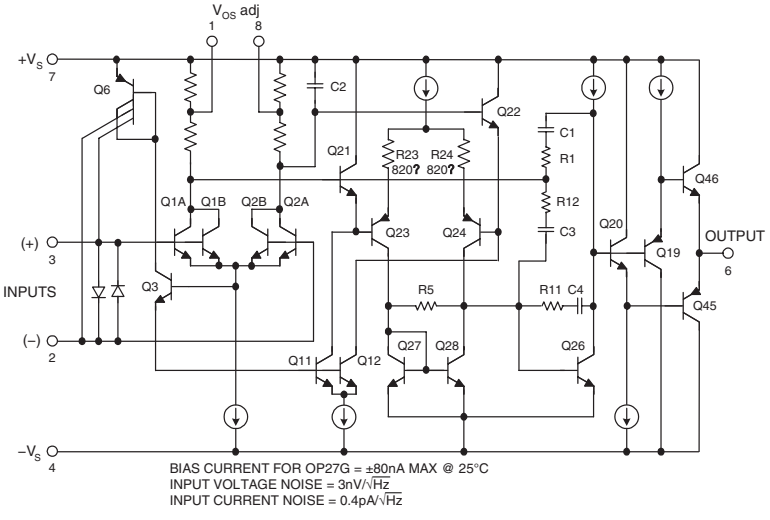



**Figure 1-24: OP27 op amp uses bias current compensated input stage**

has a maximum input bias current specification of ±80 nA at 25°C. Input voltage noise is $3\ nV/\sqrt{Hz}$, and input current noise $0.4\ pA/\sqrt{Hz}$. Offset voltage trimming by "Zener-zapping" reduces the input offset voltage of the OP27 to 50 µV maximum at 25°C for the "E" grade device (see Reference 4 for details of this trim method).

Bias-current-compensated input stages have many of the good features of the simple bipolar input stage, namely: low voltage noise, low offset, and low drift. Additionally, they have low bias current which is fairly stable with temperature. However, their current noise is not very good, and their bias current matching is poor.

These latter two undesirable side effects result from the external bias current being the *difference* between the compensating current source and the input transistor base current. Both of these currents inevitably have noise. Since they are uncorrelated, the two noises add in a root-sum-of-squares fashion (even though the dc currents subtract).

Since the resulting external bias current is the difference between two nearly equal currents, there is no reason why the net current should have a defined polarity. As a result, the bias currents of a bias-compensated op amp may not only be mismatched, they can actually flow in opposite directions. In most applications this isn't important, but in some it can have unexpected effects. (For example, the droop of a sample-and-hold [SHA] built with a bias-compensated op amp may have either polarity.)

In many cases, the bias current compensation feature is not mentioned on an op amp data sheet, and a simplified schematic isn't supplied. It is easy to determine if bias current compensation is used by examining the bias current specification. If the bias current is specified as a "±" value, the op amp is most likely compensated for bias current.

Note that this can easily be verified by examining the *offset current* specification (the difference in the bias currents). If internal bias current compensation exists, the offset current will be of the same magnitude as the bias current. Without bias current compensation, the offset current will generally be at least a factor of 10 smaller than the bias current. Note that these relationships generally hold, regardless of the exact magnitude of the bias currents.

It is also a well-known fact that, within an op amp application circuit, the effects of bias current on the output offset voltage of an op amp can often be cancelled by making the source resistances at the two inputs equal. However, there is an important caveat here. The validity of this practice holds true only for bipolar input op amps *without* bias current compensation; that is, where the input currents are well matched. In a case of an op amp using internal bias current compensation, adding an extra resistance to either input will usually make the output offset worse.

### Bias Current Compensated Superbeta Bipolar Input Stage

As mentioned above, the OP97/297/OP497-series are high performance superbeta op amps, that also use input bias current compensation. As a result, their input bias currents are ±150 pA max at 25°C. Note that in this case the "±" prefix to the bias current magnitude indicates that the amplifier uses internal bias current compensation.

A simplified schematic of an OP97 (or one-quarter of the OP497) is shown in Figure 1-25. Note that the Q1–Q2 superbeta pair is protected against large destructive differential input voltages, by the use of both back-to-back diodes, and series current-limiting resistors. Note also that the Q1–Q2 superbeta pair is also protected against excessive collector voltage, by an elaborate bias and bootstrapping network.

As a result of these clamping and protection circuits, the input common-mode voltage of this op amp series can safely vary over the full range of the supply voltages used.

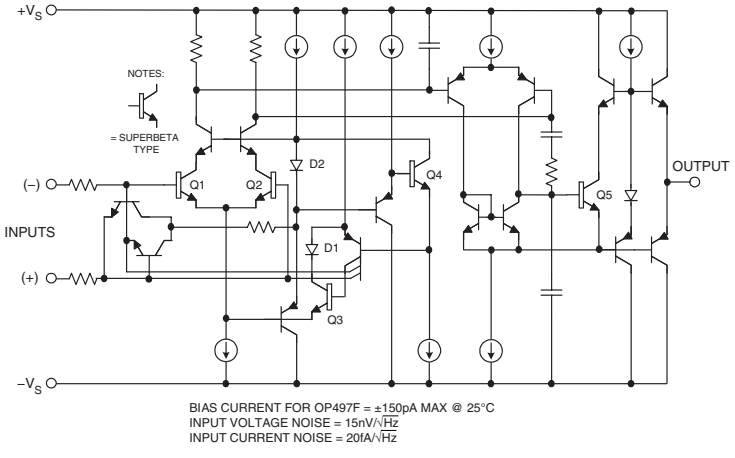



**Figure 1-25: The OP97, OP297 and OP497 op amp series uses superbeta input stage transistors and bias current compensation**

## FET Input Stages

Field-Effect Transistors (FETs) have much higher input impedance than do bipolar junction transistors (BJTs) and would therefore seem to be ideal devices for op amp input stages. However, they cannot be manufactured on all bipolar IC processes, and when a process does allow their manufacture, they often have their own problems.

FETs have high input impedance, low bias current, and good high frequency performance. (In an op amp, the lower $g_m$ of the FET devices allows higher tail currents, thereby increasing the maximum slew rate.) FETs also have much lower current noise.

On the other hand, the input offset voltage of FET long-tailed pairs is not as good as the offset of corresponding BJTs, and trimming for minimum offset does not simultaneously minimize drift. A separate trim is needed for drift, and as a result, offset and drift in a JFET op amp, while good, aren't as good as the best BJTs. A simplified trim procedure for an FET input op amp stage is shown in Figure 1-26.

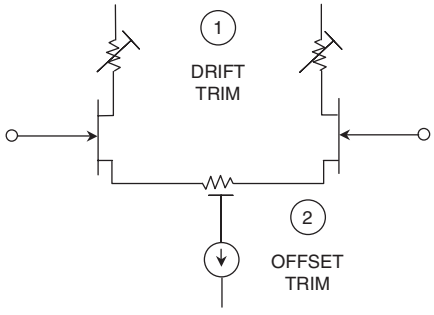



**Figure 1-26: Junction field effect transistor (JFET) input op amp stage showing offset and drift trims**

It is possible to make JFET op amps with very low voltage noise, but the devices involved are very large and have quite high input capacitance, which varies with input voltage, and so a trade-off is involved between voltage noise and input capacitance.

The bias current of an FET op amp is the leakage current of the gate diffusion (or the leakage of the gate protection diode, which has similar characteristics for a MOSFET). Such leakage currents double with every 10°C increase in chip temperature so that a FET op amp bias current is *one thousand times greater* at 125°C than at 25°C. Obviously this can be important when choosing between a bipolar or FET input op amp, especially in high temperature applications where bipolar op amp input bias current actually decreases.

Thus far, we have spoken generally of all kinds of FETs, that is, junction (JFETs) and MOS (MOSFETs). In practice, combined bipolar/JFET technology op amps (i.e., BiFET) achieve better performance than op amps using purely MOSFET or CMOS technology. While ADI and others make high performance op amps with MOS or CMOS input stages, in general these op amps have worse offset and drift, voltage noise, high-frequency performance than the bipolar counterparts. The power consumption is usually somewhat lower than that of bipolar op amps with comparable, or even better, performance.

JFET devices require more headroom than do BJTs, since their pinch-off voltage is typically greater than a BJTs base-emitter voltage. Consequently, they are more difficult to operate at very low power supply voltages (1–2 V). In this respect, CMOS has the advantage of requiring less headroom than JFETs.

## Rail-Rail Input Stages

Today, there is common demand for op amps with input CM voltage that includes *both* supply rails, i.e., *rail-to-rail* CM operation. While such a feature is undoubtedly useful in some applications, engineers should recognize that there are still relatively few applications where it is absolutely essential. These applications should be distinguished from the many more applications where a CM range *close* to the supplies, or one that includes *one* supply, is necessary, but true input rail-to-rail operation is not.

In many single-supply applications, it is required that the input CM voltage range extend to one of the supply rails (usually ground). High side or low side current-sensing applications are examples of this. Many amplifiers can handle 0 V CM inputs, and they are easily designed using PNP differential pairs (or N-channel JFET pairs) as shown in Figure 1-27. The input CM range of such an op amp generally extends from about 200 mV below the negative rail ($-V_S$ or ground), to about 1 V–2 V of the positive rail, $+V_S$.

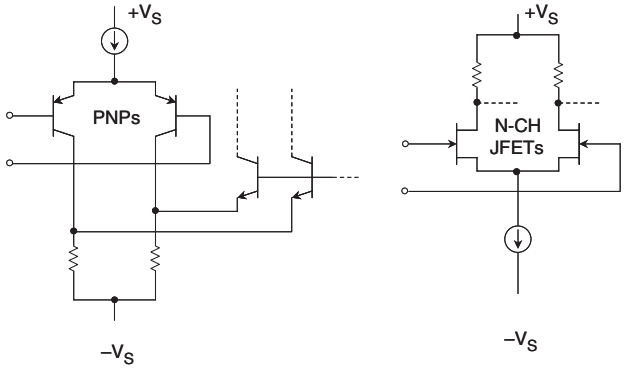



**Figure 1-27: PNP or N-channel JFET stages allow CM inputs to the negative rail**

An input stage could also be designed with NPN transistors (or P-channel JFETs), in which case the input CM range would include the positive rail, and go to within about 1 V–2 V of the negative rail. This requirement typically occurs in applications such as high-side current sensing. The OP282/OP482 input stage uses a P-channel JFET input pair whose input CM range includes the positive rail, making it suitable for high-side sensing.

The AD823 is a dual 16 MHz (G = +1) op amp with an N-channel JFET input stage (as in Figure 1-27). A simplified schematic of the AD823 is shown in Figure 1-28. This device can operate on single-supply voltages from +3 V to +36 V. This range also allows operation on traditional ±5 V, or ±15 V dual supplies if desired. Similar devices in a related (but lower power) family include the AD820, the AD822, and the AD824.

The AD823 JFET input stage allows the input common-mode voltage to range from200 mV below the negative supply to within about 1.5 V of the positive supply. Input offset voltage is 0.8 mV maximum at 25°C, input bias current is 25 pA maximum at 25°C, offset voltage drift is 2 µV/°C, and input voltage noise is $16\ \text{nV}/\sqrt{\text{Hz}}$ . Current noise is only $1\ \text{fA}/\sqrt{\text{Hz}}$. The AD823 is laser wafer trimmed for both offset voltage and offset voltage drift as described above.

A simplified diagram of a true rail-to-rail input stage is shown in Figure 1-29. Note that this requires use of *two* long-tailed pairs: one of PNP bipolar transistors Q1–Q2, the other of NPN transistors Q3–Q4. Similar input stages can also be made with CMOS pairs.

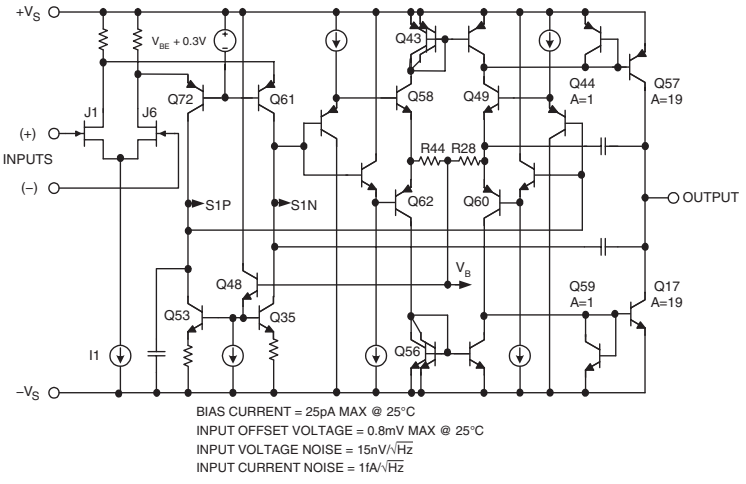



**Figure 1-28: AD823 JFET input op amp simplified schematic**

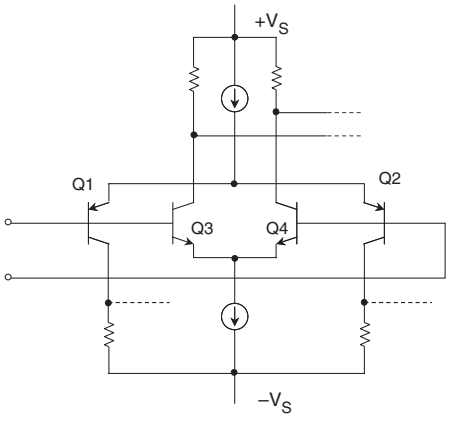



**Figure 1-29: A true rail-to-rail bipolar transistor input stage**

It should be noted that these two pairs will exhibit *different* offsets and bias currents, so when the applied CM voltage changes, the amplifier input offset voltage and input bias current does also. In fact, when both current sources remain active throughout most of the entire input common-mode range, amplifier input offset voltage is the *average* offset voltage of the two pairs. In those designs where the current sources are alternativelyswitched off at some point along the input common-mode voltage, amplifier input offset voltage is dominated by the PNP pair offset voltage for signals near the negative supply, and by the NPN pair offset voltage for signals near the positive supply. As noted, a true rail-to-rail input stage can also be constructed from CMOS transistors, for example as in the case of the CMOS AD8531/AD8532/AD8534 op amp family.

Amplifier input bias current, a function of transistor current gain, is also a function of the applied input common-mode voltage. The result is relatively poor common-mode rejection (CMR), and a changing common-mode input impedance over the CM input voltage range, compared to familiar dual-supply devices. These specifications should be considered carefully when choosing a rail-to-rail input op amp, especially

for a noninverting configuration. Input offset voltage, input bias current, and even CMR may be quite good over *part* of the common-mode range, but much worse in the region where operation shifts between the NPN and PNP devices, and vice versa.

True rail-to-rail amplifier input stage designs must transition from one differential pair to the other differential pair, somewhere along the input CM voltage range. Some devices like the OP191/OP291/OP491 family and the OP279 have a common-mode crossover threshold at approximately 1 V below the positive supply (where signals do not often occur). The PNP differential input stage is active from about 200mV below the negative supply to within about 1 V of the positive supply. Over this common-mode range, amplifier input offset voltage, input bias current, CMR, input noise voltage/current are primarily determined by the characteristics of the PNP differential pair. At the crossover threshold, however, amplifier input offset voltage becomes the average offset voltage of the NPN/PNP pairs and can change rapidly.

Also, as noted previously, amplifier bias currents are dominated by the PNP differential pair over most of the input common-mode range, and change polarity and magnitude at the crossover threshold when the NPN differential pair becomes active.

Op amps like the OP184/OP284/OP484 family, shown in Figure 1-30, utilize a rail-to-rail input stage design where both NPN and PNP transistor pairs are active throughout most of the entire input CM voltage range. With this approach to biasing, there is no CM crossover threshold. Amplifier input offset voltage is the average offset voltage of the NPN and the PNP stages, and offset voltage exhibits a smooth transition throughout the entire input CM range, due to careful laser trimming of input stage resistors.

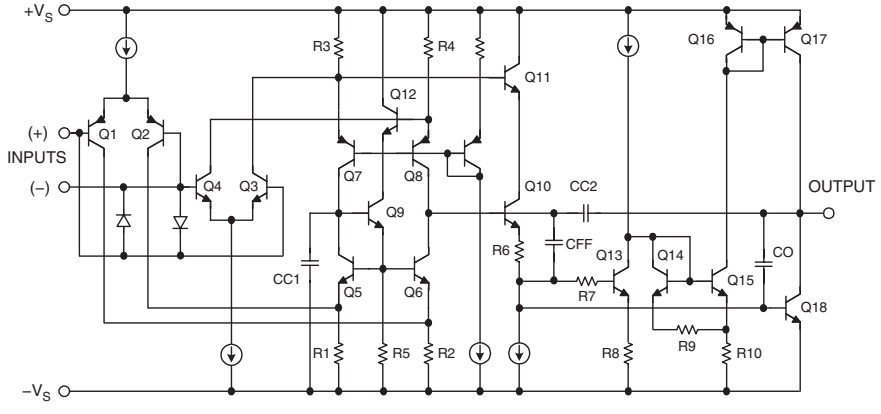



**Figure 1-30: OP284 op amp simplified schematic shows true rail-to-rail input stage**

In the same manner, through careful input stage current balancing and input transistor design, the OP184 family input bias currents also exhibit a smooth transition throughout the entire CM input voltage range. The exception occurs at the very extremes of the input range, where amplifier offset voltages and bias currents increase sharply, due to the slight forward-biasing of parasitic p-n junctions. This occurs for input voltages within approximately 1 V of either supply rail.

When *both* differential pairs are active throughout most of the entire input common-mode range, amplifier transient response is faster through the middle of the common-mode range by as much as a factor of 2 for bipolar input stages and by a factor of $\sqrt{2}$ for JFET input stages. This is due to the higher transconductance of two operating input stages.

Input stage $g_m$ determines the slew rate and the unity-gain crossover frequency of the amplifier, hence response time degrades slightly at the extremes of the input common-mode range when either the PNP stage (signals approaching the positive supply rail) or the NPN stage (signals approaching the negative supply rail) are forced into cutoff. The thresholds at which the transconductance changes occur are approximately within 1 V of either supply rail, and the behavior is similar to that of the input bias currents.

In light of the many quirks of true rail-to-rail op amp input stages, applications that do require true rail-to-rail inputs should be carefully evaluated, and an amplifier chosen to ensure that its input offset voltage, input bias current, common-mode rejection, and noise (voltage and current) are suitable.

### Don't Forget Input Overvoltage Considerations

In order to achieve the performance levels required, it is sometimes not possible to provide complete overdrive protection within IC op amps. Although most op amps have some type of input protection, care must still be taken to prevent possible damage against both CM and differential voltage stress.

This is most likely to occur, for example, when the input signal comes from an external sensor. Rather than present a cursory discussion of this topic here, the reader is instead referred to Chapter 7, Section 7-4 for a detailed examination of this important issue.

## *Output Stages*

The earliest IC op amp output stages were NPN emitter followers with NPN current sources or resistive pull-downs, as shown in Figure 1-31A. Naturally, the slew rates were greater for positive-going than they were for negative-going signals.

While all modern op amps have push-pull output stages of some sort, many are still asymmetrical, and have a greater slew rate in one direction than the other. Asymmetry tends to introduce distortion on ac signals and generally results from the use of IC processes with faster NPN than PNP transistors. It may also result in an ability of the output to approach one supply more closely than the other in terms of saturation voltage.

In many applications, the output is required to swing only to one rail, usually the negative rail (i.e., ground in single-supply systems). A pull-down resistor to the negative rail will allow the output to approach that rail (provided the load impedance is high enough, or is also grounded to that rail), but only slowly. Using an FET current source instead of a resistor can speed things up, but this adds complexity, as shown in Figure 1-31B.

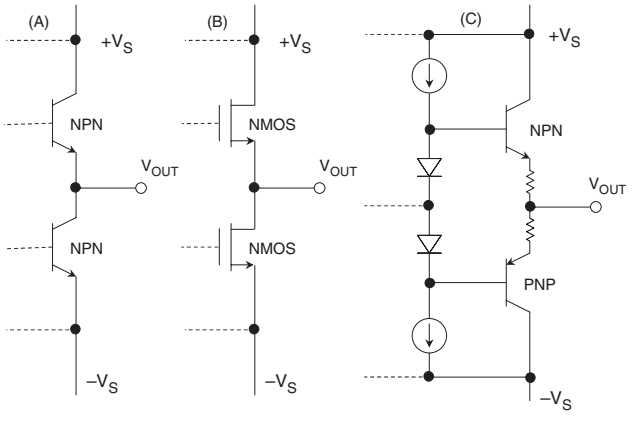



**Figure 1-31: Some traditional op amp output stages**

With modern complementary bipolar (CB) processes, well matched high speed PNP and NPN transistors are readily available. The complementary emitter follower output stage shown in Figure 1-31C has many advantages, but the most outstanding one is the low output impedance. However, the output voltage of this stage can only swing within about one $V_{BE}$ drop of either rail. Therefore an output swing of 1 V to 4 V is typical of such a stage, when operated on a single 5 V supply.

The complementary common-emitter/common-source output stages shown in Figure 1-32A and B allow the op amp output voltage to swing much closer to the rails, but these stages have much higher open-loop output impedance than do the emitter follower-based stages of Figure 1-31C.

In practice, however, the amplifier's high open-loop gain and the applied feedback can still produce an application with low output impedance (particularly at frequencies below 10 Hz). What should be carefully evaluated with this type of output stage is the loop gain within the application, with the load in place. Typically, the op amp will be specified for a minimum gain with a load resistance of 10 kΩ (or more). Care should be taken that the application loading doesn't drop lower than the rated load, or gain accuracy may be lost.

It should also be noted these output stages can cause the op amp to be more sensitive to capacitive loading than the emitter-follower type. Again, this will be noted on the device data sheet, which will indicate a maximum of capacitive loading before overshoot or instability will be noted.

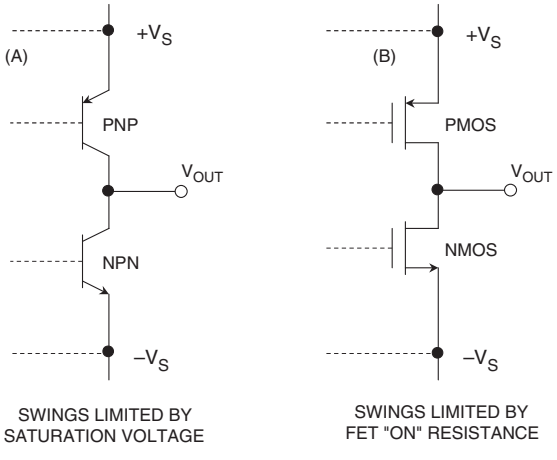



**Figure 1-32: "Almost" rail-to-rail output structures**

The complementary common emitter output stage using BJTs (Figure 1-32A) cannot swing completely to the rails, but only to within the transistor saturation voltage ($V_{CESAT}$) of the rails. For small amounts of load current (less than 100 μA), the saturation voltage may be as low as 5 mV to 10 mV, but for higher load currents, the saturation voltage can increase to several hundred mV (for example, 500 mV at 50 mA).

On the other hand, an output stage constructed of CMOS FETs (Figure 1-32B) can provide nearly true rail-to-rail performance, but only under no-load conditions. If the op amp output must source or sink substantial current, the output voltage swing will be reduced by the I × R drop across the FETs internal "on" resistance. Typically this resistance will be on the order of 100 Ω for precision amplifiers, but it can be less than 10 Ω for high current drive CMOS amplifiers.

For the above basic reasons, it should be apparent that there is no such thing as a *true* rail-to-rail output stage, hence the caption of Figure 1-32 ("Almost" Rail-to-Rail Output Structures). The best any op amp output stage can do is an almost rail-to-rail swing, when it is lightly loaded.

Op amps built on foundry CMOS processes have a primary advantage of low cost. Also, it is relatively straightforward to design rail-to-rail input and output stages with these CMOS devices, which will operate on low supply voltages.

Figure 1-33 shows a simplified schematic of the AD8531/AD8532/AD8534 (single/dual/quad) op amp, which is typical of these design types. The AD8531/AD8532/AD8534 operates on a single 2.7 V to 6.0 V supply and can drive 250 mA. Input offset voltage is 25 mV maximum at 25°C, and voltage noise $45\ \text{nV}/\sqrt{\text{Hz}}$.

This type of op amp is simple and cost effective, and the lack of high dc precision is often no disadvantage. To the contrary, the high output drive available can be an overriding plus, particularly in AC-coupled applications.

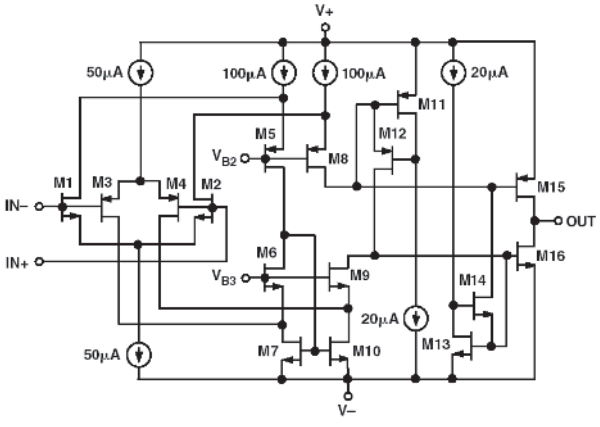



**Figure 1-33: AD8531/AD8532/AD8534 CMOS rail-to-rail op amp simplified schematic**

## Output Stage Surge Protection

Most low speed, high precision op amps generally have output stages which are protected against short circuits to ground or to either supply. Their output current is limited to a little more than 10 mA. This has the additional advantage of minimizing self-heating of the chip (and thus minimizing dc errors due to chip temperature differentials).

If an op amp is required to deliver both high precision and a large output current, it is advisable to use a separate output stage (within the loop) to minimize self-heating of the precision op amp. A simple buffer amplifier such as the BUF04, or a section of a nonprecision op amp can be used.

Note that high speed op amps cannot have output currents limited to low values, as it would affect their slew rate and load drive ability. Thus most high speed op amps will source/sink between 50 mA–100 mA. Although many high speed op amps have internal protection for *momentary* shorts, their junction temperatures can be exceeded with sustained shorts. The user needs to be wary, and consult the specific device ratings.

## Offset Voltage Trim Processes

The AD860x CMOS op amp family exploits the advantages of digital technology to minimize the offset voltage normally associated with CMOS amplifiers. Offset voltage trimming is done after the devices are packaged. A digital code is entered into the device to adjust the offset voltage to less than 1 mV, depending upon the grade. Wafer testing is not required, and the patented ADI technique called DigiTrim™ requires no extra pins to accomplish the function. These devices have rail-to-rail inputs and outputs (similar to Figure 1-33), and the NMOS and PMOS parallel input stages are trimmed separately using DigiTrim to minimize the offset voltage in both pairs. A functional diagram of the AD8602 DigiTrim op amp is shown in Figure 1-34.

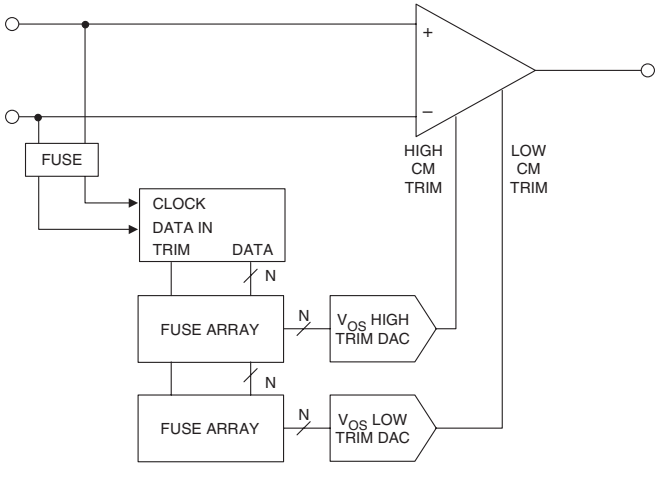



**Figure 1-34: AD8602 (1/2) CMOS op amp showing DigiTrim**

DigiTrim adjusts the offset voltage by programming digitally weighted current sources. The trim information is entered through existing pins using a special digital sequence. The adjustment values can be temporarily programmed, evaluated, and readjusted for optimum accuracy before permanent adjustment is performed. After the trim is completed, the trim circuit is locked out to prevent the possibility of any accidental re-trimming by the end user.

The physical trimming, achieved by blowing polysilicon fuses, is very reliable. No extra pads or pins are required, and no special test equipment is needed to perform the trimming. The trims can be done after packaging so that assembly-related shifts can be eliminated. No testing is required at the wafer level because of high die yields

The first devices to use this new technique are the Analog Devices' AD8601/02/04 (single, dual, quad) rail-to-rail CMOS amplifiers. The offset is trimmed for both high and low common-mode conditions so that the offset voltage is under 500 µV over the full common-mode input voltage range. The bandwidth of the op amps is 8 MHz, slew rate is 5 V/µs, and supply current is only 640 µA per amplifier.

At this point it is useful to review the other popular trim methods. Analog Devices pioneered the use of thin film resistors and laser wafer trimming for precision amplifiers, references, data converters, and other linear ICs (see Reference 5). Up to 16-bit accuracy can be achieved with trimming, and the thin film resistors themselves are very stable with temperature and can add to the thermal stability and accuracy of

a device, even without trimming. Thin film deposition and patterning are processes that must be tightly controlled. The laser trimming systems are also quite expensive. In-package trimming is not possible, so assembly-related shifts cannot be easily compensated. Nevertheless, thin film trimming at the wafer level provides continuous fine trim resolution in precision integrated circuits where high accuracy and stability are required.

*Zener zapping* uses a voltage to create a metallic short circuit across the base-emitter junction of a transistor to remove a circuit element (see References 4 and 6). The base-emitter junction is commonly referred to as a zener, although the mechanism is actually avalanche breakdown of the junction. During the avalanche breakdown across the base-emitter junction, the very high current densities and localized heating generate rapid metal migration between the base and emitter connections, leading to a metallic short across the junction. With proper biasing (current, voltage, and time), this short will have a very low resistance value. If a series of these base-emitter junctions are arranged in parallel with a string of resistors, zapping selected junctions will short out portions of the resistor string, thereby adjusting the total resistance value.

It is possible to perform zener zap trimming in the packaged IC to compensate for assembly-related shifts in the offset voltage. However, trimming in the package requires extra package pins. Alternately, trimming at the wafer level requires additional probe pads. Probe pads do not scale effectively as the process features shrink. Thus, the die area required for trimming is relatively constant, regardless of the process geometries. Some form of bipolar transistor is required for the trim structures, therefore a purely MOS-based process may not have zener zap capability. The nature of the trims is discrete since each zap removes a predefined resistance value. Increasing trim resolution requires additional transistors and pads or pins, which rapidly increase the total die area and/or package cost. This technique is most cost-effective for fairly large geometry processes where the trim structures and probe pads make up a relatively small percentage of the overall die area.

It was in the process of creating the industry standard OP07 in 1975 that Precision Monolithics Incorporated pioneered zener zap trimming (Reference 6). The OP07 and other similar parts must be able to operate from over ±15 V supplies. As a result, they utilize relatively large device geometries to support the high voltage requirements, and extra probe pads don't significantly increase die area.

*Link trimming* is the cutting of metal or poly-silicon links to remove a connection. In link trimming, either a laser or a high current is used to destroy a "shorted" connection across a parallel resistive element. Removing the connection increases the effective resistance of the combined element(s). Laser cutting is similar to laser trimming of thin films. The high local heat from the laser beam causes material changes that lead to a nonconductive area, effectively cutting a metal or conductive polysilicon connector.

The high-current link trim method works as an inverse to zener zapping—the conductive connection is destroyed, rather than created by a zener-zap.

Link trim structures tend to be somewhat more compact than laser trimmed resistor structures. No special processes are required in general, although the process may have to be tailored to the laser characteristics if laser cutting is used. With the high-current trimming method, testing at the wafer level may not be required if die yields are good. The laser cutting scheme doesn't require extra contact pads, but the trim structures don't scale with the process feature sizes. Laser cutting of links cannot be performed in the package, and requires additional probe pads on the die. In addition, it can require extra package pins for in-package high-current trims. Like zener zapping, link trimming is discrete. Resolution improvements require additional structures, increasing area and cost.

*EEPROM trimming* utilizes special, nonvolatile digital memory to store trim data. The stored data bits control adjustment currents through on-chip D/A converters. Memory cells and D/A converters scale with

the process feature size. In-package trimming and even trimming in the customer's system is possible so that assembly-related shifts can be trimmed out. Testing at the wafer level is not required if yields are reasonable. No special hardware is required for the trimming beyond the normal mixed-signal tester system, although test software development may be more complicated.

Since the trims can be overwritten, it is possible to periodically reprogram the system to account for long-term drifts or to modify system characteristics for new requirements. The number of reprogram cycles possible depends on the process, and is finite. Most EEPROM processes provide enough rewrite cycles to handle routine recalibration.

This trim method does require special processing. Stored trim data can be lost under certain conditions, especially at high operating temperatures. At least one extra digital contact pad/package pin is required to input the trim data to the on-chip memory.

This technique is only available on MOS-based processes due to the very thin oxide requirements. The biggest drawback is that the on-chip D/A converters are large—often larger than the amplifier circuits they are adjusting. For this reason, EEPROM trimming is mostly used for data converter or system-level products where the trim D/A converters represent a much smaller percentage of the overall die area.

Figure 1-35 summarizes the key features of each ADI trim method. It can be seen from that all trim methods have their respective places in producing high performance linear integrated circuits.

| PROCESS | TRIMMED AT: | SPECIAL PROCESSING | RESOLUTION |
|---|---|---|---|
| DigiTrim™ | Wafer or Final Test | None | Discrete |
| Laser Trim | Wafer | Thin Film Resistor | Continuous |
| Zener Zap Trim | Wafer | None | Discrete |
| Link Trim | Wafer | Thin Film or Poly Resistor | Discrete |
| EEPROM Trim | Wafer or Final Test | EEPROM | Discrete |

**Figure 1-35: Summary of ADI trim processes**

## *Op Amp Process Technologies*

The wide variety of op amp processes is shown in Figure 1-36. The early 1960s op amps used standard NPN-based bipolar processes. The PNP transistors of these processes were extremely slow and were used primarily for current sources and level-shifting.

The ability to produce matching high speed PNP transistors on a bipolar process added great flexibility to op amp circuit designs. The first p-epi complementary bipolar (CB) process was introduced by ADI in the mid-1980s. The $f_t$s of the PNP and NPN transistors were approximately 700 MHz and 900 MHz, respectively, and had 30 V breakdowns. Since its original introduction in 1985, several additional CB processes have been developed at ADI designed for higher speeds and lower breakdowns. For example, a current 5 V CB process has 9 GHZ PNPs and 16 GHz NPNs. These CB processes are used in today's precision op amps, as well as those requiring wide bandwidths.

- BIPOLAR (NPN-BASED): This is Where it All Started
- COMPLEMENTARY BIPOLAR (CB): Rail-to-Rail, Precision, High Speed
- BIPOLAR + JFET (BiFET): High Input Impedance, High Speed
- COMPLEMENTARY BIPOLAR + JFET (CBFET): High Input Impedance, Rail-to-Rail Output, High Speed
- COMPLEMENTARY MOSFET (CMOS): Low Cost Op Amps (ADI DigiTrim Minimizes Offset Voltage and Drift in CMOS Op Amps)
- BIPOLAR (NPN) + CMOS (BiCMOS): Bipolar Input Stage adds Linearity, Low Power, Rail-to-Rail Output
- COMPLEMENTARY BIPOLAR + CMOS (CBCMOS): Rail-to-Rail Inputs, Rail-to-Rail Outputs, Good Linearity, Low Power, Higher Cost

**Figure 1-36: Op amp process technology summary**

The JFETs available on the Analog Devices complementary bipolar processes allow high input impedance op amps to be designed suitable for such applications as photodiode or electrometer preamplifiers. These processes are sometimes designated as *CBFET*.

CMOS op amps, generally have higher offset voltages and offset voltage drift than trimmed bipolar or BiFET op amps, however the Analog Devices DigiTrim process described above yields low offset voltage, while keeping costs low. Voltage noise for CMOS op amps tends to be larger, but the input bias current is very low. They offer low power and cost (foundry CMOS processes are typically used).

The addition of bipolar or complementary devices to a CMOS process (BiMOS or CBCMOS) adds greater flexibility, better linearity, and lower power as well as additional cost. The bipolar devices are typically used for the input stage to provide good gain and linearity, and CMOS devices for the rail-to-rail output stage.

In summary, there is no single IC process that is optimum for all op amps. Process selection and the resulting op amp design depends on the targeted applications and ultimately should be transparent to the customer.