CMPE283 – Virtualization
Midterm Exam

Name:_____

This exam is governed by the rules posted in the class Canvas discussions forum.

Select the best answer for each question. Questions 1-10 are worth 5 points each. Questions 11-12 are worth 10 points each.

1. _____ True/False : Prior to the introduction of Intel VMX/AMD SVM, it was not possible to fully virtualize a guest OS on the x86 platform.

2. _____ Which of the following is a feature provided by a VMM?

A. Scheduling VCPUs on PCPUs
B. Scheduling processes on CPUs
C. Handling system calls from processes
D. All of the above
E. None of the above

3. _____ Which of the following terms describes a possible treatment of floating point registers during a process context switch?

A. MOV to CR3
B. Lazy switch
C. Page fault
D. FPU
E. None of the above

4. _____ Which of the following best describes the size of the virtual address space on 32-bit Intel CPUs?

A. Always 32 bits
B. Always more than 32 bits
C. Sometimes more than 32 bits, depending on the CPU
D. None of the above

5. _____ When operating in 64 bit (long) mode, the depth of the processor's paging structures (page directory/page table) is:

A. 2 levels deep
B. 3 levels deep
C. 4 levels deep
D. There is not enough information provided to answer the question accurately

6. _____ True/False: A legacy system BIOS is typically responsible for selecting a boot device from amongst the available boot devices (perhaps with input from the end user).

7. _____ True/False: The x86 architecture provides for four privilege levels of operation.

8. _____ Which of the following contains mappings between interrupt vector numbers and interrupt handler routines?

A. IDT
B. LDT
C. GDT
D. SDT
E. None of the above

9. _____ Which of the following will occur if “exit on HLT” is disabled and a guest OS executes the HLT instruction, when running on a multiprocessor machine?

A. The VCPU will become unresponsive until a virtual interrupt is delivered
B. The PCPU will become unresponsive until a physical interrupt is delivered
C. The hypervisor will be unable to schedule other VCPUs on the PCPU that is halted
D. All of A,B, and C
E. None of A,B, or C

10. _____ Which world switch consumes more CPU processing time during register read/write to/from the VMCS?

A. VM Entry
B. VM Exit
C. Both VM Entries and VM Exits take equal time

11. What considerations should the hypervisor author make when determinining which VMX controls to enable?

12. Describe the processor and VMM's behavior when a guest VM executes “CPUID”.