Integrated Circuit Technology

Final Process Project

NMOS Fabrication process

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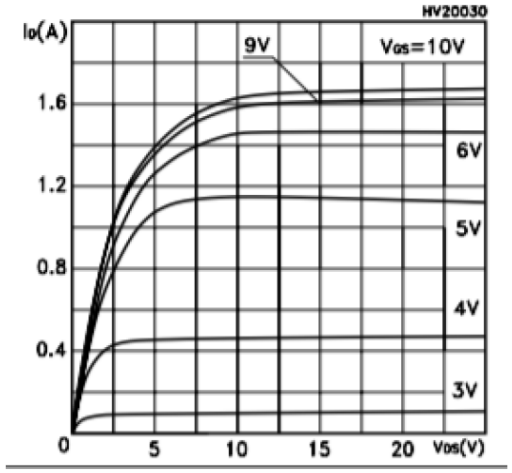
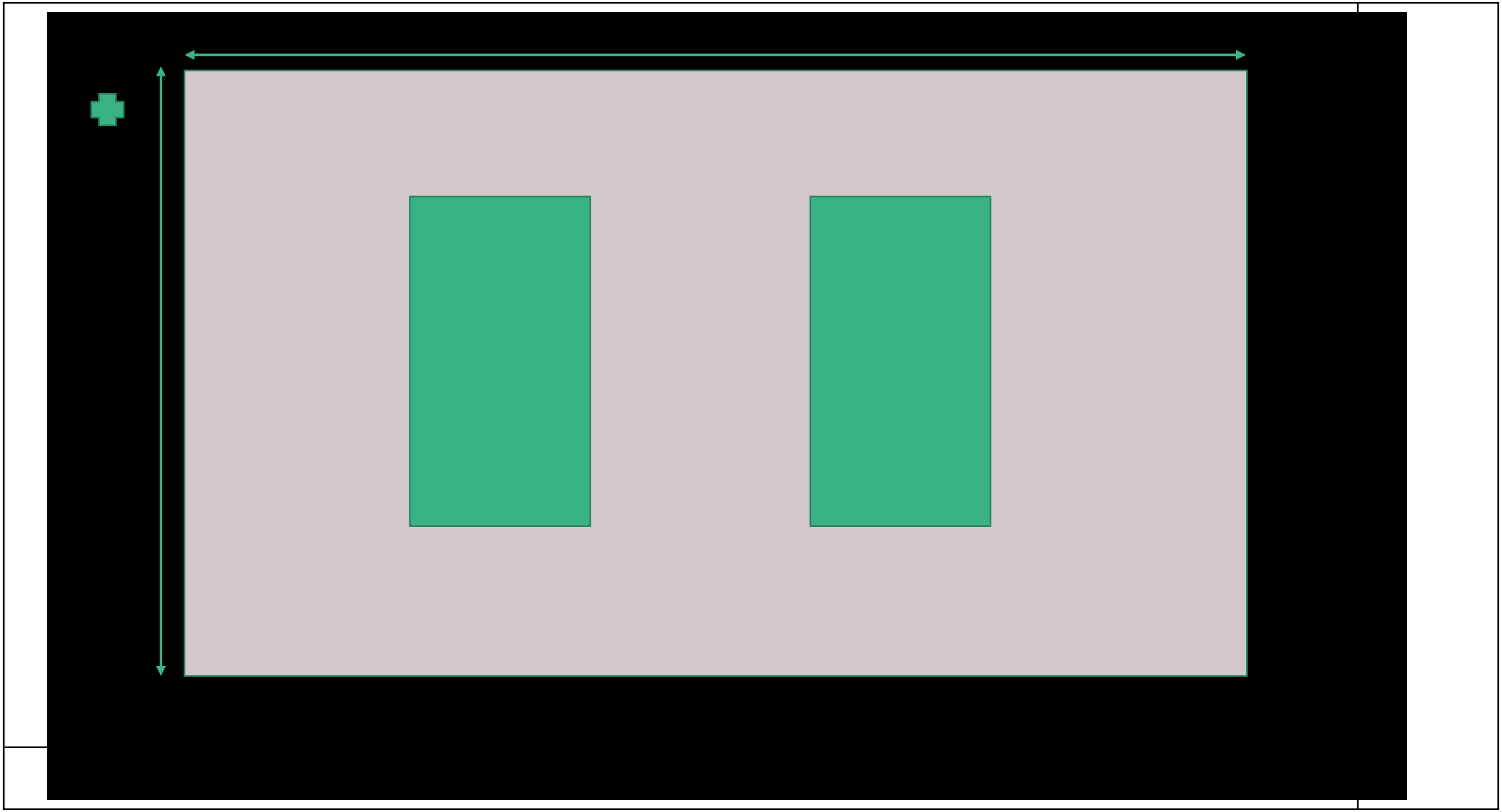
W/L calculations

- From the graph presented below the w/l has been calculated… Given Kp = 0.08 sec, Vth = 2.1 V
- Consider Id = 1.62, Vgs = 10V
- W/L = 0.3244
- Channel length is 80 um and width is ~26um

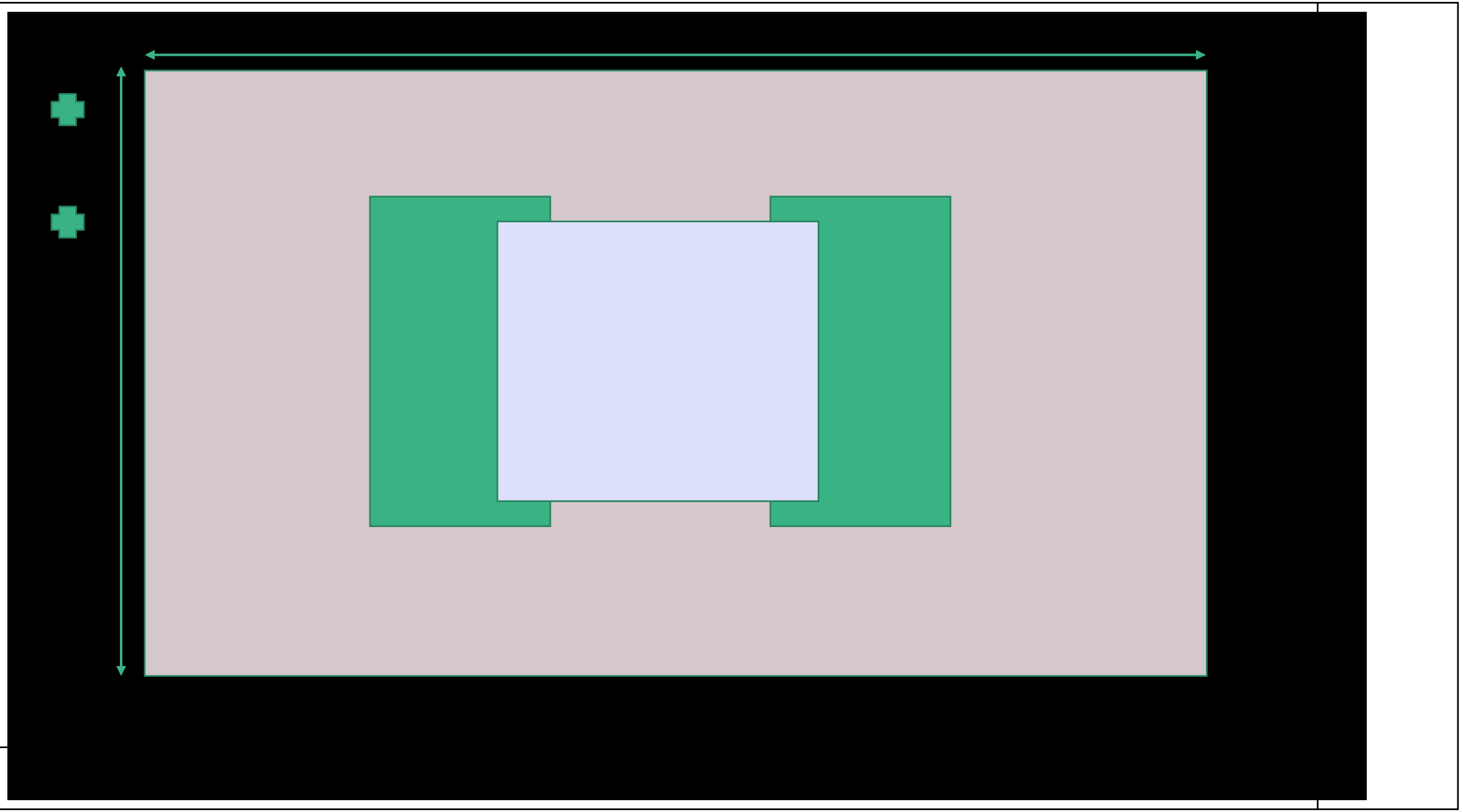


$$I_D = Kp \cdot \frac{W}{L}(V_{GS} - V_{th})^2 \ [A]$$

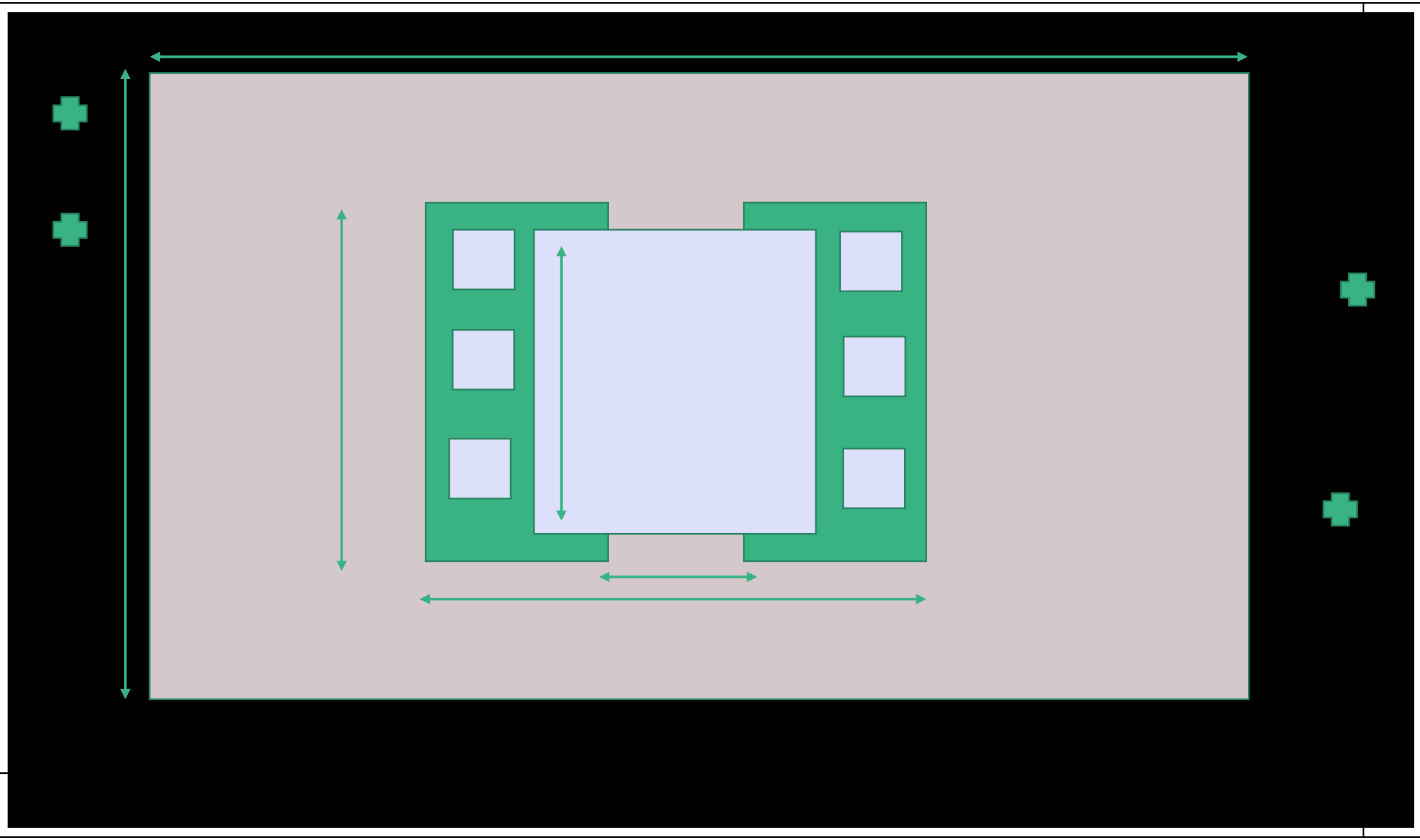
Gate measurements from the W/L calculations



Mask for Drain and Source



Gate level Mask



Metal contacts – Aluminum metal