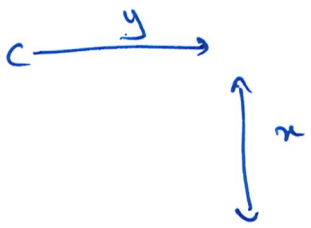
Q1 (a) Maximum no of transistors on a 1cm x 1cm



$x = 42 + 2 + 42 = 200nm$

$y = 42 + 2 + L + L + 42 = 400nm$

Now;

Area : $x \times y = 400 \times 200 = 80000nm^2$

$= 8 \times 10^{-10} cm^2$

for a 1cm x 1cm ~~trans~~block, no of transistors would be

$$\frac{1cm^2}{8 \times 10^{-10} cm^2} = 1.25 \times 10^9 \text{ transistors.}$$

(b) Given $d = 2nm$. (thickness of Gate oxide layer)

C_L of one transistor

$$C_L = \frac{\varepsilon}{d} \cdot (W \times L)$$

$$\Rightarrow C_L = \frac{3.9 \times 8.85 \times 10^{-14}}{2 \times 10^{-7} cm} \cdot (100nm \times 100nm)$$

$$= \frac{3.9 \times 8.85 \times 10^{-14}}{2 \times 10^{-7} cm} \times (10^{-5} cm)^2$$

$C_L = 1.7258 \times 10^{-16}$ Farad.

(c) Dissipated power is given by {for a single transistor}

Given $f_{clk} = 100\,MHz$

$= C_L \times V_{DD}^2 \times f_{clk}$

$= (1.7258 \times 10^{-16}) \times (5V)^2 \times 100 \times 10^6\ Hz$

$= 4.3144 \times 10^{-7}$

Now, total dissipated power in a 1cm x 1cm block is given by

$= (4.3144 \times 10^{-7}) \times (1.25 \times 10^9)$

=> total dissipated power = 539.2969 watts.

(d) Given $R_\theta = 0.5\,C/W$; $T_A = 25^\circ C$

the temperature of chip is given by

$T_j = T_A + (\text{Dissipated power} \times R_\theta)$

$= 25^\circ C + (539.2969(W) \times 0.5\,(C/W))$

$T_j = 294.6484^\circ C$

(e) The on-chip temperature for a 1cm x 1cm is way too high. this reduces the life span of the chip.

(f) to reduce the temp of chip to less than 150°C the oxide thickness can be increased in this case to reduce the temp of chip.