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ALU - Arithmetic and Logic Unit designed as part of the Paplinski's "WORD SERIAL MULTIPLIER"

The function of the ALU is to perform operations like addition and subtraction, The F - output from the ALU is loaded into the A-register through arithmetic shift right operation

Least significant bit f0 is shifted into the Q register, The inputs to the ALU A and B are taken from the D register and A register respectively, again the output from the ALU with F = F/2 is performed and fed

Cursor = 60ns
Baseline = 0
Cursor-Baseline = 60ns

Baseline = 0

TimeA = 60ns