padmanabhuni - U88648766 || USF EE

D-register designed as part of the Paplinski's "WORD SERIAL MULTIPLIER"

D register is the Multiplicant register here, which operates when the clock is high -> clk - '1', this is a memory register which is used by the ALU

We have clk, op (operation), DD as inputs and D as the output, D_s, Dop are the internal signals, D_s will feed the output to the D register when the Dop is '1' finally we give 5 different test vectors to test